CS5253B-8

3.0 A LDO 5-Pin 2.5 V Fixed Linear Regulator for Remote Sense Applications

This new very low dropout linear regulator reduces total power dissipation in the application. To achieve very low dropout, the internal pass transistor is powered separately from the control circuitry. Furthermore, with the control and power inputs tied together, this device can be used in single supply configuration and still offer a better dropout voltage than conventional PNP–NPN based LDO regulators. In this mode the dropout is determined by the minimum control voltage.

The CS5253B–8 is offered in a five–terminal D^2PAK package, which allows for the implementation of a remote–sense pin permitting very accurate regulation of output voltage directly at the load, where it counts, rather than at the regulator. This remote sensing feature virtually eliminates output voltage variations due to load changes and resistive voltage drops. Typical load regulation measured at the sense pin is less than 1.0 mV for an output voltage of 2.5 V with a load step of 10 mA to 3.0 A.

The CS5253B–8 has a very fast transient loop response.

Internal protection circuitry provides for “bust–proof” operation, similar to three–terminal regulators. This circuitry, which includes overcurrent, short circuit, and overtemperature protection will self protect the regulator under all fault conditions.

The CS5253B–8 is ideal for generating a 2.5 V supply to power graphics controllers used on VGA cards. Its remote sense and low value capacitance requirements make this a low cost high performance solution. The CS5253B–8 is optimized from the CS5253–1 to allow a lower value of output capacitor to be used at the expense of a slower transient response.

Features

- V_{OUT} Fixed @ 2.5 V ± 1.5%
- V_{POWER} Dropout < 0.40 V @ 3.0 A
- $V_{CONTROL}$ Dropout < 1.05 V @ 3.0 A
- 1.5% Trimmed Reference
- Fast Transient Response
- Remote Voltage Sensing
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Drop–In Replacement for EZ1582
- Backwards Compatible with 3–Pin Regulators
- Very Low Dropout Reduces Total Power Consumption

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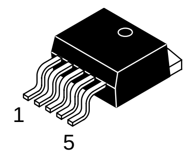
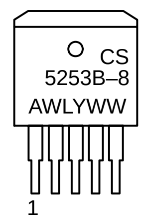


D^2PAK
5–PIN
DP SUFFIX
CASE 936F

Tab = V_{OUT}
Pin 1. V_{SENSE}
2. GND
3. V_{OUT}
4. $V_{CONTROL}$
5. V_{POWER}

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS5253B–8GDP5	D^2PAK*	50 Units/Rail
CS5253B–8GDPR5	D^2PAK*	750 Tape & Reel

*5–Pin.

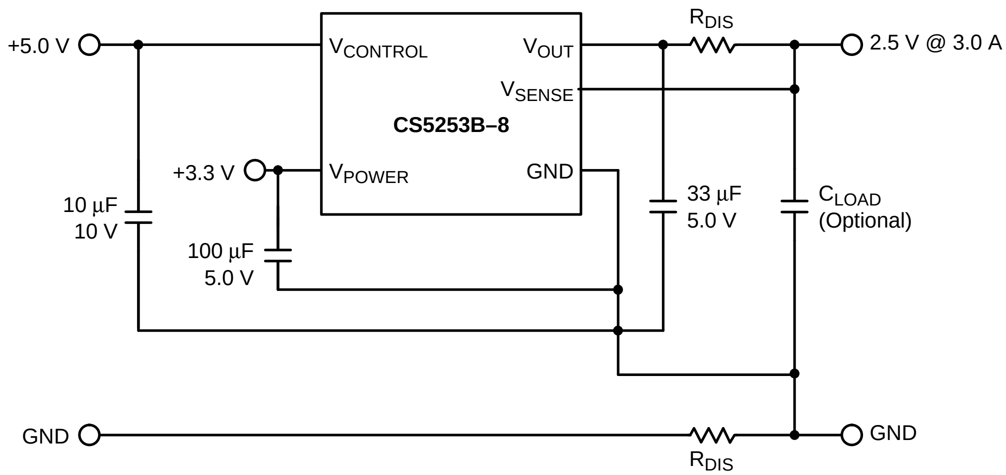


Figure 1. Application Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
V_{POWER} Input Voltage	6.0	V
$V_{CONTROL}$ Input Voltage	13	V
Operating Junction Temperature Range, T_J	0 to 150	°C
Storage Temperature Range	–65 to +150	°C
ESD Damage Threshold	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; 0°C ≤ T_J ≤ 150°C; V_{SENSE} = V_{OUT} and GND = 0 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
CS5253B–8					
Output Voltage	$V_{CONTROL}$ = 3.9 V to 12 V, V_{POWER} = 3.13 V to 5.5 V, I_{OUT} = 10 mA to 3.0 A	2.463 (–1.5%)	2.5	2.538 (+1.5%)	V
Line Regulation	$V_{CONTROL}$ = 3.9 V to 12 V, V_{POWER} = 3.13 V to 5.5 V, I_{OUT} = 10 mA	–	0.02	0.2	%
Load Regulation	$V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, I_{OUT} = 10 mA to 3.0 A, with Remote Sense	–	0.04	0.3	%
Minimum Load Current (Note 2)	$V_{CONTROL}$ = 5.0 V, V_{POWER} = 3.3 V, ΔV_{OUT} = +1.0%	–	0	0	mA
Control Pin Current (Note 3)	$V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, I_{OUT} = 100 mA $V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, I_{OUT} = 3.0 A	– –	6.0 35	10 120	mA mA
Ground Pin Current	$V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, I_{OUT} = 10 mA	–	7	10	mA
Current Limit	$V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, ΔV_{OUT} = –4.0%	3.1	4.0	–	A
Short Circuit Current	$V_{CONTROL}$ = 3.9 V, V_{POWER} = 3.13 V, V_{OUT} = 0 V	2.0	3.5	–	A

2. The minimum load current is the minimum current required to maintain regulation.
3. The $V_{CONTROL}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:100 ratio. The minimum value is equal to the quiescent current of the device.

ELECTRICAL CHARACTERISTICS (continued) (0°C ≤ T_A ≤ 70°C; 0°C ≤ T_J ≤ 150°C; V_{SENSE} = V_{OUT} and GND = 0 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
CS5253B–8					
Ripple Rejection (Note 4)	$V_{CONTROL}$ = V_{POWER} = 3.9 V, V_{RIPPLE} = 1.0 $V_{P–P}$ @ 120 Hz, I_{OUT} = 3.0 A	60	80	–	dB
Thermal Regulation	30 ms Pulse, T_A = 25°C	–	0.002	–	%/W
$V_{CONTROL}$ Dropout Voltage (Minimum $V_{CONTROL}$ – V_{OUT}) (Note 5)	V_{POWER} = 3.13 V, I_{OUT} = 100 mA V_{POWER} = 3.13 V, I_{OUT} = 1.0 A V_{POWER} = 3.13 V, I_{OUT} = 3.0 A	– – –	0.90 1.00 1.05	1.15 1.15 1.30	V V V
V_{POWER} Dropout Voltage (Minimum V_{POWER} – V_{OUT}) (Note 5)	$V_{CONTROL}$ = 3.9 V, I_{OUT} = 100 mA $V_{CONTROL}$ = 3.9 V, I_{OUT} = 1.0 A $V_{CONTROL}$ = 3.9 V, I_{OUT} = 3.0 A	– – –	0.05 0.15 0.40	0.15 0.25 0.60	V V V
RMS Output Noise	Freq = 10 Hz to 10 kHz, T_A = 25°C	–	0.003	–	$\%V_{OUT}$
Temperature Stability	–	0.5	–	–	%
Thermal Shutdown (Note 6)	–	150	180	210	°C
Thermal Shutdown Hysteresis	–	–	25	–	°C
$V_{CONTROL}$ Supply Only Output Current	$V_{CONTROL}$ = 13 V, V_{POWER} Not Connected, GND = V_{OUT} = V_{SENSE} = 0 V	–	–	50	mA
V_{POWER} Supply Only Output Current	V_{POWER} = 6.0 V, $V_{CONTROL}$ Not Connected, GND = V_{OUT} = V_{SENSE} = 0 V	–	0.1	1.0	mA

4. This parameter is guaranteed by design and is not 100% production tested.
5. Dropout is defined as either the minimum control voltage ($V_{CONTROL}$) or minimum power voltage (V_{POWER}) to output voltage differential required to maintain 1.5% regulation at a particular load current.
6. This parameter is guaranteed by design, but not parametrically tested in production. However, a 100% thermal shutdown functional test is performed on each part.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # D²PAK	PIN SYMBOL	FUNCTION
1	V_{SENSE}	This Kelvin sense pin allows for remote sensing of the output voltage at the load for improved regulation. It is internally connected to the positive input of the voltage sensing error amplifier.
2	GND	This pin is connected to system ground.
3	V_{OUT}	This pin is connected to the emitter of the power pass transistor and provides a regulated voltage capable of sourcing 3.0 A of current.
4	$V_{CONTROL}$	This is the supply voltage for the regulator control circuitry. For the device to regulate, this voltage should be between 0.9 V and 1.3 V (depending on the output current) greater than the output voltage. The control pin current will be about 1.0% of the output current.
5	V_{POWER}	This is the power input voltage. This pin is physically connected to the collector of the power pass transistor. For the device to regulate, this voltage should be between 0.1 V and 0.6 V greater than the output voltage depending on the output current. The output load current of 3.0 A is supplied through this pin.

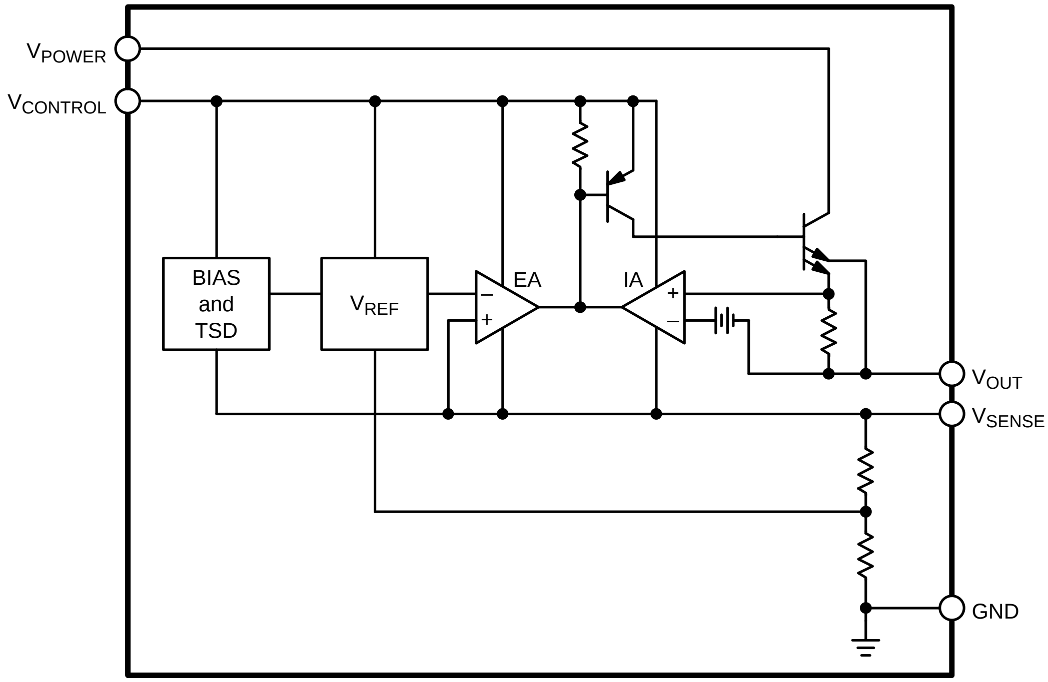


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

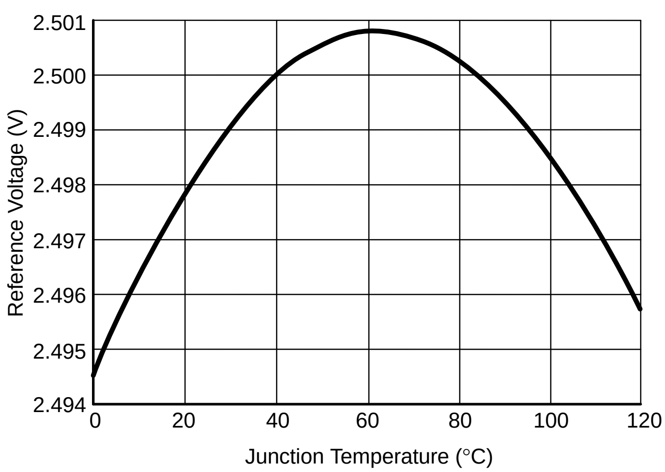


Figure 3. Output Voltage vs Junction Temperature

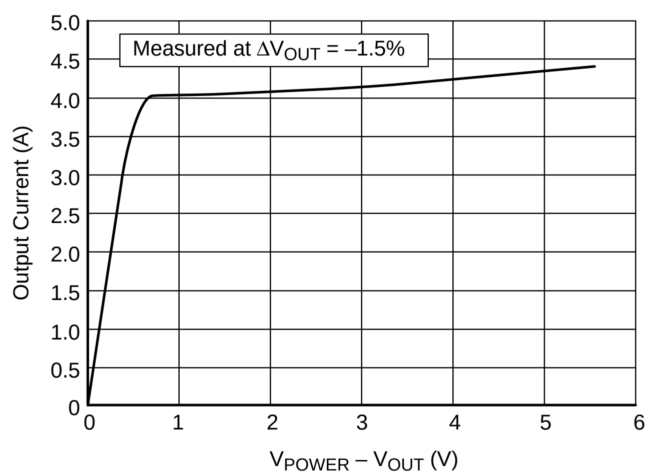


Figure 4. Output Current vs $V_{POWER} - V_{OUT}$

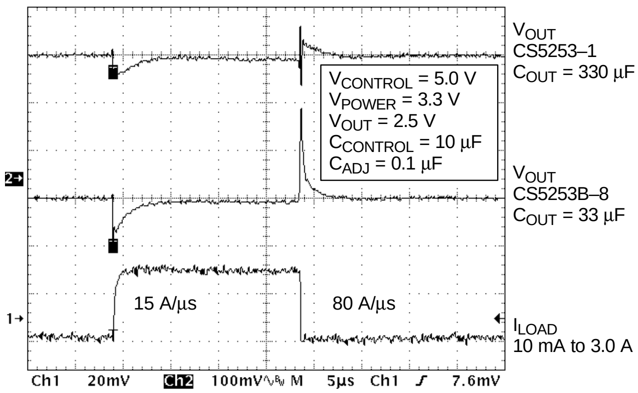


Figure 5. Transient Response Comparison between CS5253–1 and CS5253B–8

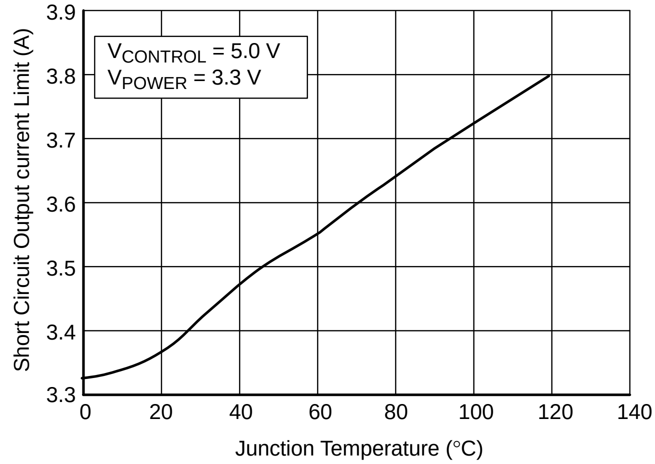


Figure 6. Short Circuit Output Current vs Junction Temperature

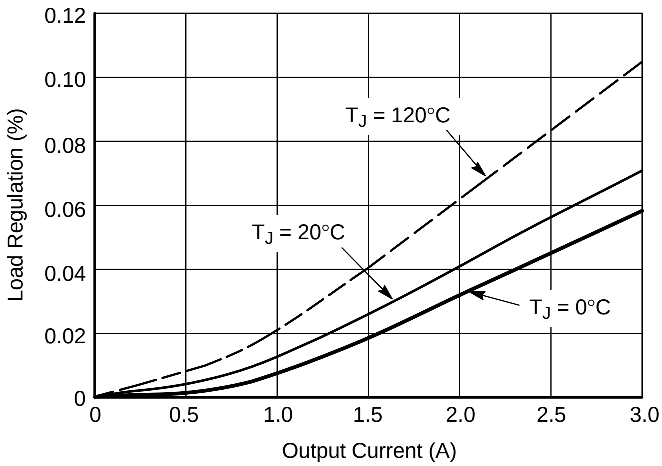


Figure 7. Load Regulation vs Output Current

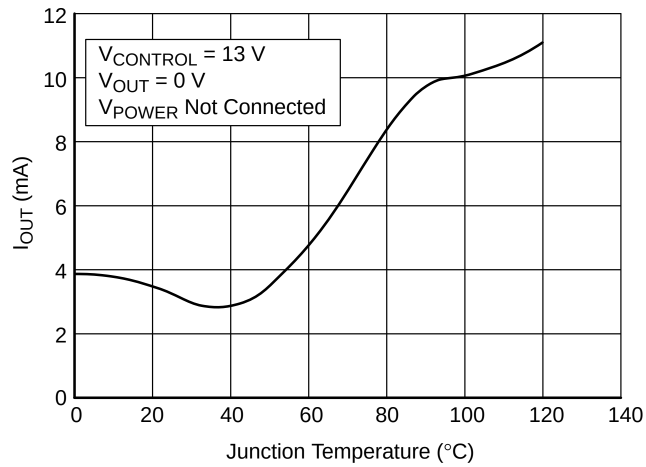


Figure 8. $V_{CONTROL}$ Only Output Current vs Junction Temperature

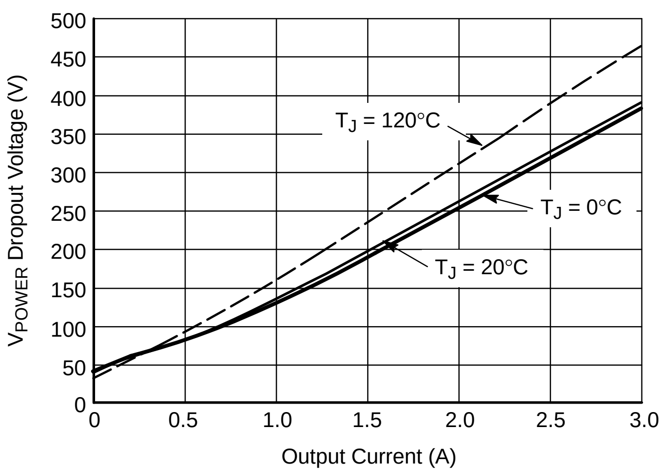


Figure 9. V_{POWER} Dropout Voltage vs Output Current

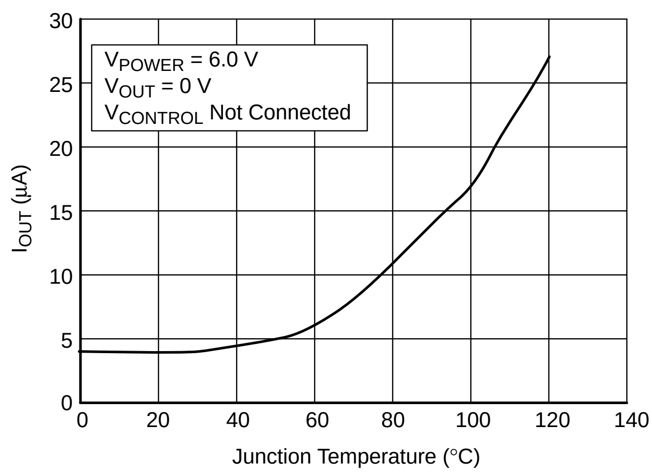


Figure 10. V_{POWER} Only Output Current vs Junction Temperature

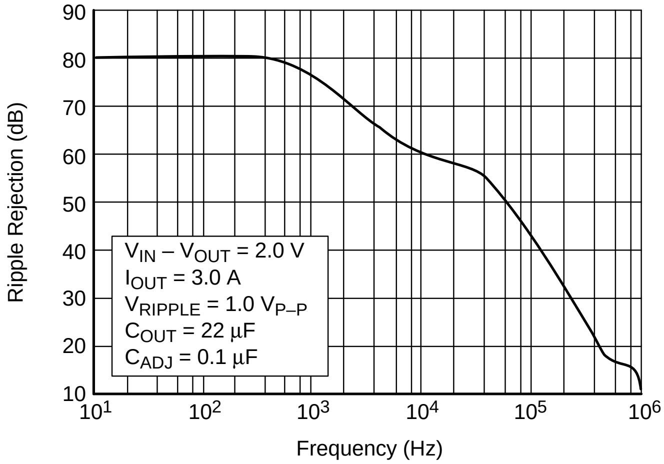


Figure 11. Ripple Rejection vs Frequency

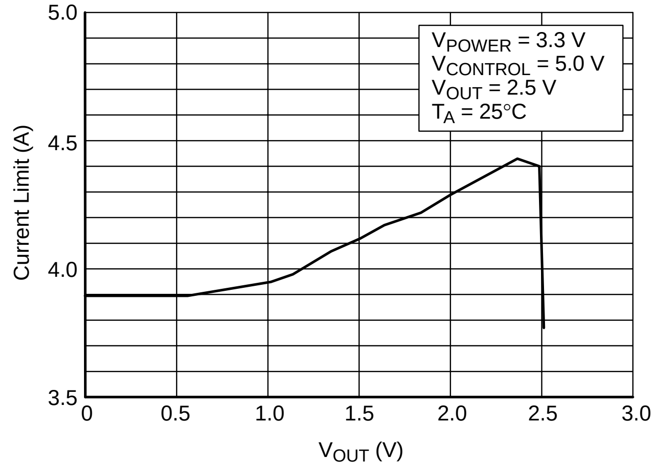


Figure 12. Current Limit vs V_{OUT}

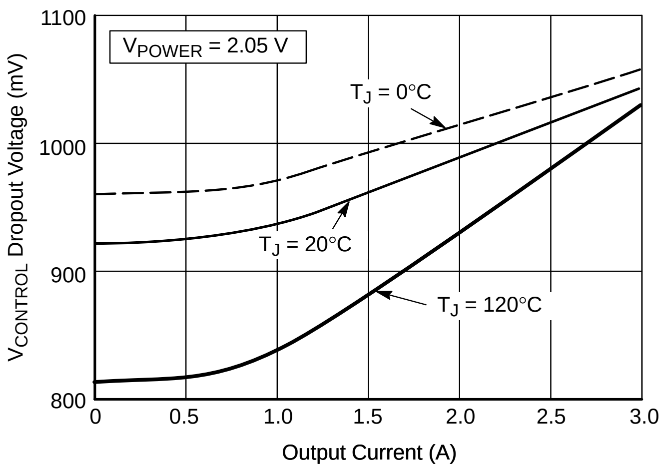


Figure 13. $V_{CONTROL}$ Dropout Voltage vs Output Current

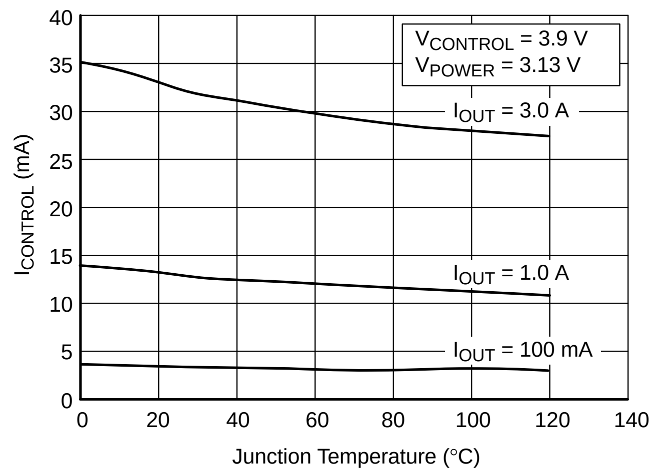


Figure 14. $V_{CONTROL}$ Supply Current vs Junction Temperature

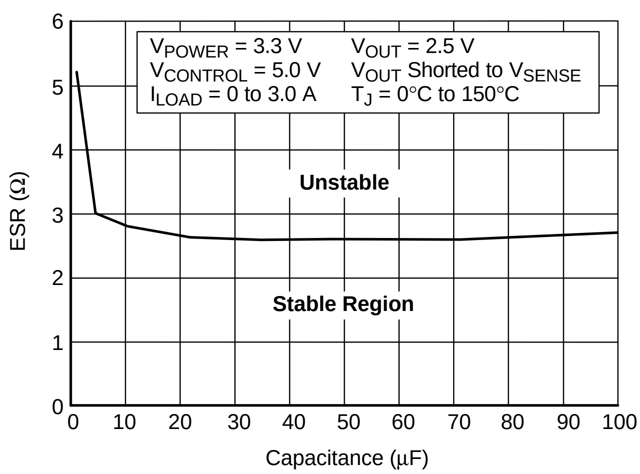


Figure 15. Stability vs ESR

APPLICATIONS NOTES

THEORY OF OPERATION

The CS5253B–8 linear regulator is fixed at 2.5 V at currents up to 3.0 A. The regulator is protected against short circuits, and includes a thermal shutdown circuit with hysteresis. The output, which is current limited, consists of a PNP–NPN transistor pair and requires an output capacitor for stability.

V_{POWER} Function

The CS5253B–8 utilizes a two supply approach to maximize efficiency. The collector of the power device is brought out to the V_{POWER} pin to minimize internal power dissipation under high current loads. $V_{CONTROL}$ provides for the control circuitry and the drive for the output NPN transistor. $V_{CONTROL}$ should be at least 1.0 V greater than the output voltage. Special care has been taken to ensure that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be limited to about three milliamperes until the power input voltage comes up. If the power input voltage comes up first, the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.

The CS5253B–8 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage.

Output Voltage Sensing

The CS5253B–8 five terminal linear regulator includes a dedicated V_{SENSE} function. This allows for true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation. Regulation will be optimized at the point where the sense pin is tied to the output.

DESIGN GUIDELINES

Remote Sense

Remote sense operation can be easily obtained with the CS5253B–8 but some care must be paid to the layout and positioning of the filter capacitors around the part. The ground side of the input capacitors on the +5.0 V and +3.3 V lines and the local V_{OUT}–to–ground output capacitor on the IC must be tied close to the ground pin of the regulator. This will establish the stability of the part. The IC ground may then be connected to ground remotely at the load, giving the ground portion remote sense operation.

The V_{SENSE} line can then be tied remotely at the positive load connection, giving the feedback remote sense operation. The remote sense lines should be Kelvin connected so as to eliminate the effect of load current voltage drop. An optional bypass capacitor may be used at the load to reduce the effect of load variations and spikes.

Current Limit

The internal current limit circuit limits the output current under excessive load conditions.

Short Circuit Protection

The device includes short circuit protection circuitry that clamps the output current at approximately 500mA less than its current limit value. This provides for a current foldback function, which reduces power dissipation under a direct shorted load.

Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to activate above a die junction temperature of approximately 150°C and to shut down the regulator output. This circuitry has 25°C of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

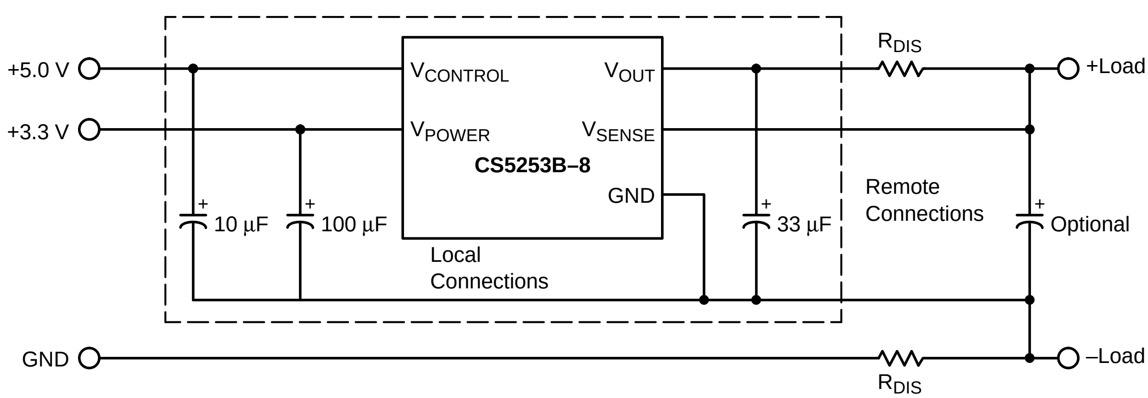


Figure 16. Remote Sense

Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5253B–8 usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to V_{OUT} on the CS5253B–8, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound in necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit

The thermal characteristics of an IC depend on the following four factors: junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$T_{J(max)} = T_{A(max)} + PD_{(max)} \times R_{\Theta JA}$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$PD_{(max)} = (V_{IN(max)} - V_{OUT(min)}) I_{OUT(max)} + V_{IN(max)} \times I_{IN(max)}$$

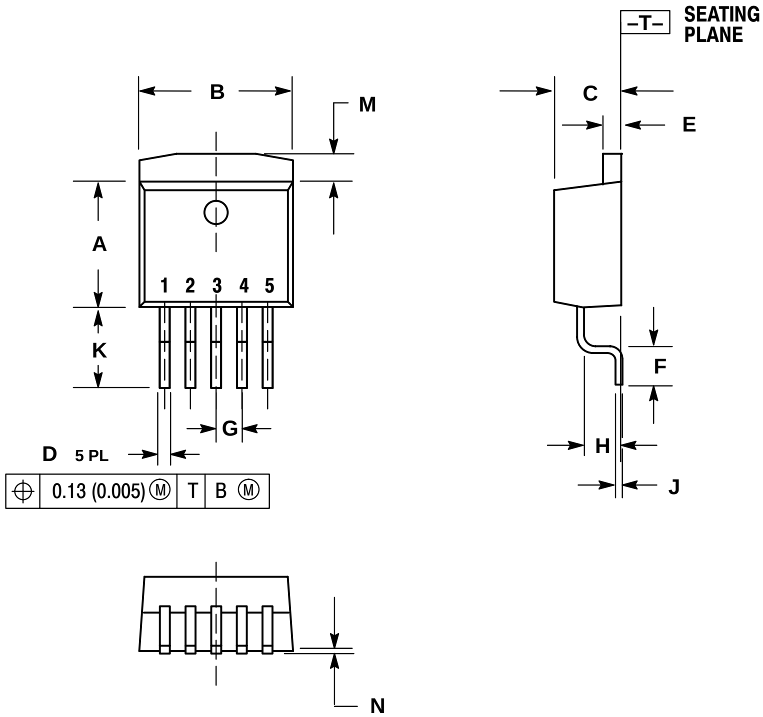
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance which is measured in degrees per watt. Like series electrical resistances, these thermal resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $R_{\Theta JA}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ($R_{\Theta JC}$), case to heat sink ($R_{\Theta CS}$), and heat sink to ambient air ($R_{\Theta SA}$). The equation is:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA}$$

The value for $R_{\Theta JC}$ is 2.5°C/watt for the CS5253B–8 in the D2PAK package. For a high current regulator such as the CS5253B–8 the majority of heat is generated in the power transistor section. The value for $R_{\Theta SA}$ depends on the heat sink type, while the $R_{\Theta CS}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta JA}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see our application note “Thermal Management,” document number AND8036/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

PACKAGE DIMENSIONS

D^2PAK
5–PIN
DP SUFFIX
CASE 936F–01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.035	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.067 BSC		1.70 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

PACKAGE THERMAL DATA

Parameter		D^2PAK, 5–Pin	Unit
$R_{\Theta JC}$	Typical	2.5	°C/W
$R_{\Theta JA}$	Typical	10–50*	°C/W

*Depending on thermal properties of substrate. $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$.

Notes

Notes

PUBLICATION ORDERING INFORMATION

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