T-46-23-14

CY7C198
CY7C199

CYPRESS SEMICONDUCTOR

32,768 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 25 ns
- Low active power
  - 880 mW
- Low standby power
  - 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

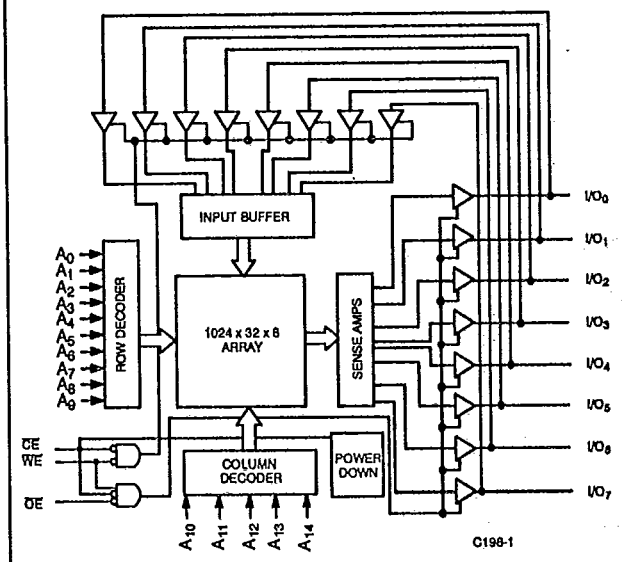
Functional Description

The CY7C198 and CY7C199 are high-performance CMOS static RAMs organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by 75% when deselected. The CY7C199 is in the space-saving 300-mil-wide DIP package and leadless chip carrier. The CY7C198 is in the standard 600-mil-wide package.

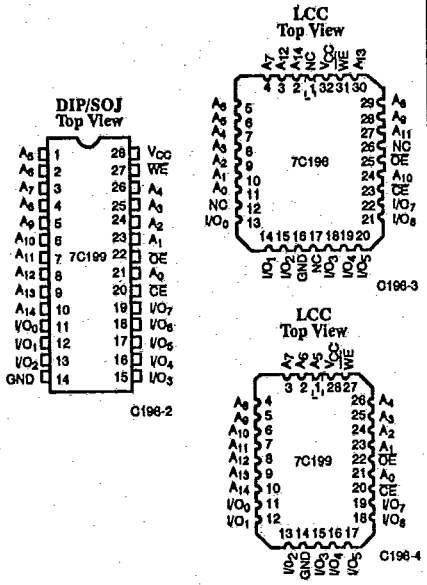
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C198–12 7C199–12	7C198–15 7C199–15	7C198–20 7C199–20	7C198–25 7C199–25	7C198–35 7C199–35	7C198–45 7C199–45	7C198–55 7C199–55
Maximum Access Time (ns)		12	15	20	25	35	45	55
Maximum Operating Current (mA)	Commercial	160	160	160	160	150	150	150
	Military		180	180	160	160	160	160
Maximum Standby Current (mA)		40	40	40	35	35	35	35

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C198−12 7C199−12 Min.	7C198−12 7C199−12 Max.	7C198−15 7C199−15 Min.	7C198−15 7C199−15 Max.	7C198−20 7C199−20 Min.	7C198−20 7C199−20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC}$, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		160		160		160	mA
			Mil				180		180	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$ $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, $f = 0$			20		20		20	mA

Shaded area contains advanced information.

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

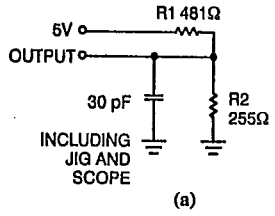
Parameters	Description	Test Conditions		7C198–25 7C199–25 Min.	7C198–25 7C199–25 Max.	7C198–35, 45, 55 7C199–35, 45, 55 Min.	7C198–35, 45, 55 7C199–35, 45, 55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		160		150	mA
			Mil		160		160	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$			35		35	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f=0			20		20	mA

Capacitance[4]

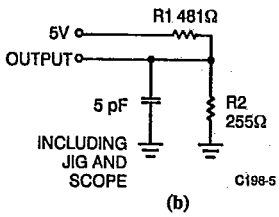
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

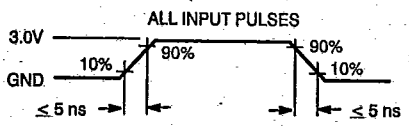


(a)



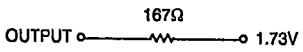
(b)

C198-5



C198-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 5]

Parameters	Description	7C198–12 7C199–12		7C198–15 7C199–15		7C198–20 7C199–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[8, 9]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		ns
t_{AW}	Address Set-Up to Write End	9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	9		10		15		ns
t_{SD}	Data Set-Up to Write End	7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns

Shaded area contains advanced information.

Notes:

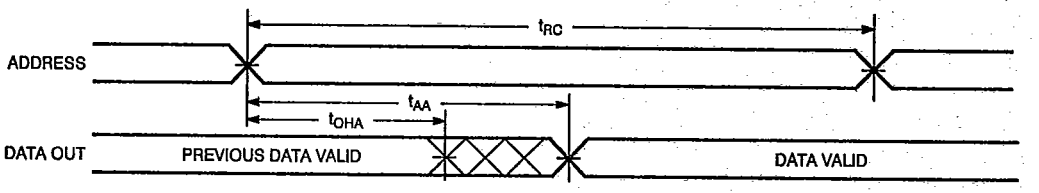
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[2, 5] (continued)

Parameters	Description	7C198–25 7C199–25		7C198–35 7C199–35		7C198–45 7C199–45		7C198–55 7C199–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		13		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6,7]		13		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25		25	ns
WRITE CYCLE[8, 9]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		50		ns
t_{AW}	Address Set-Up to Write End	20		30		40		50		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		40		ns
t_{SD}	Data Set-Up to Write End	15		17		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		13		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns

Switching Waveforms

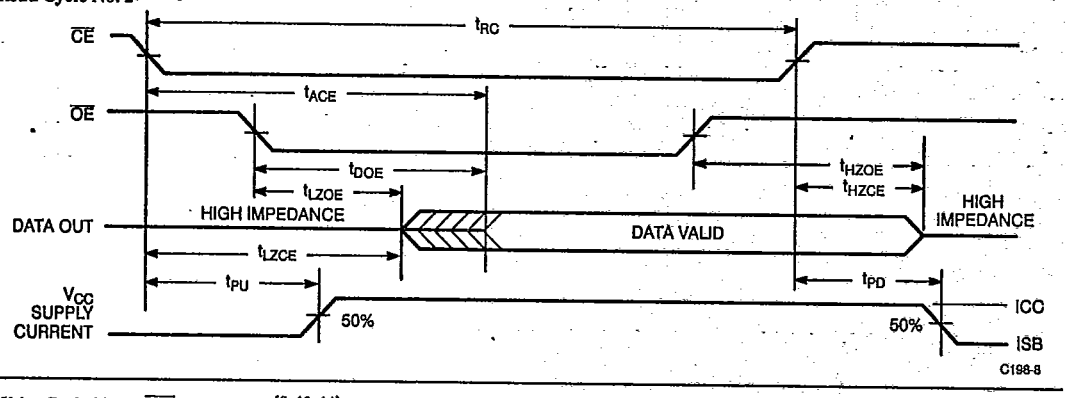
Read Cycle No. 1[10, 11]



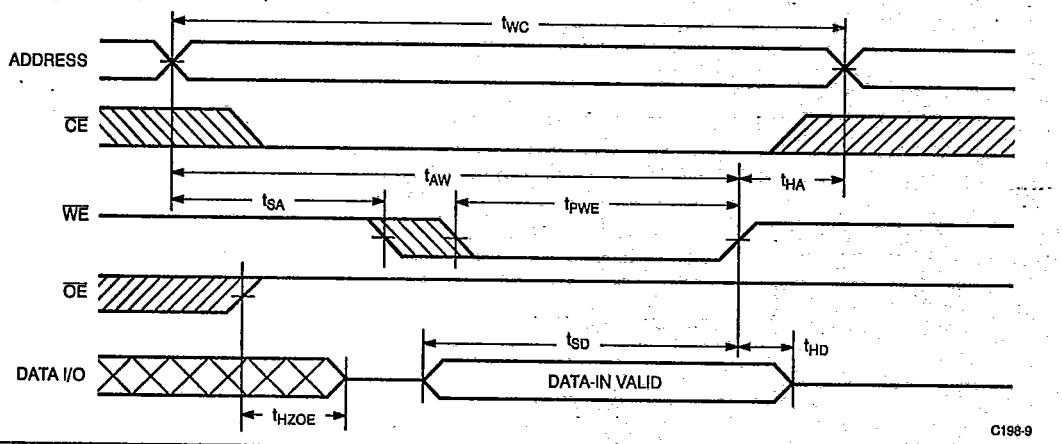
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

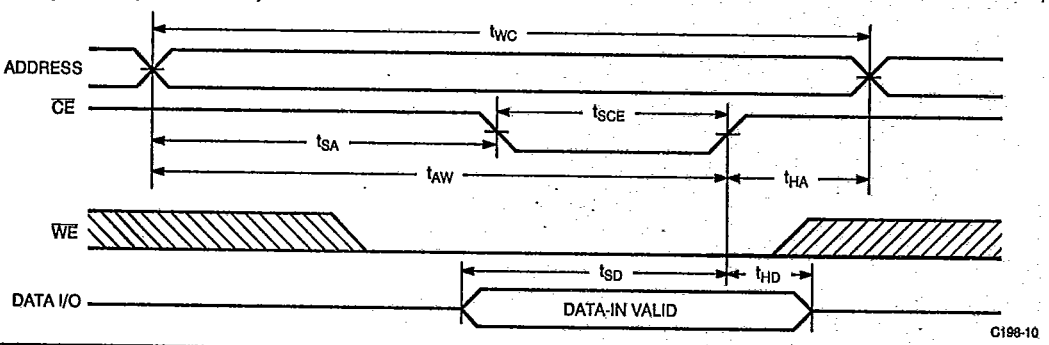
Read Cycle No. 2[11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 13, 14]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 14]

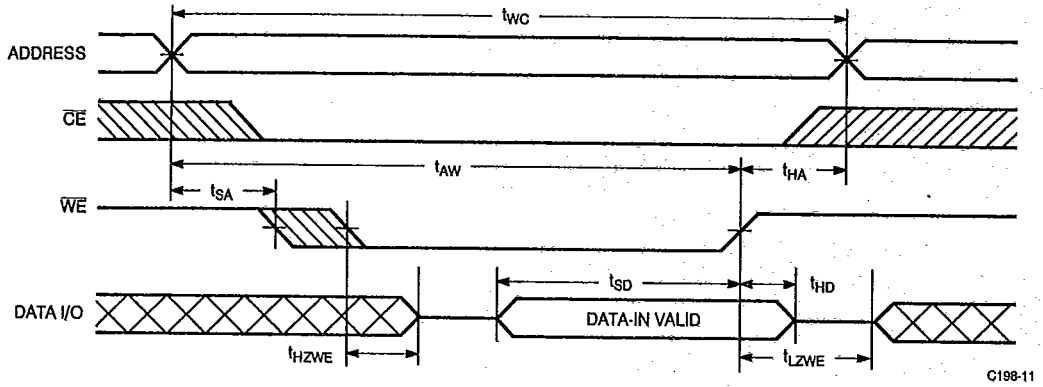


Notes:

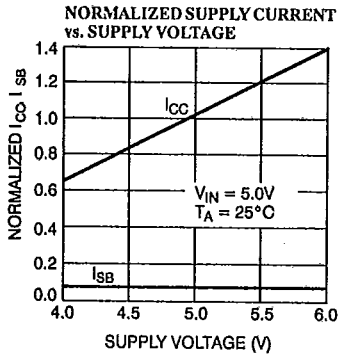
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

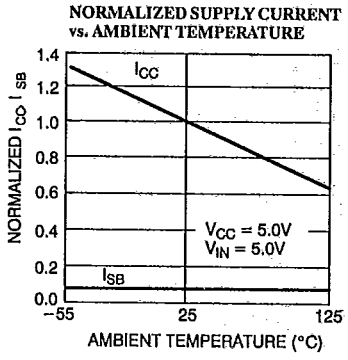
Switching Waveforms (continued)

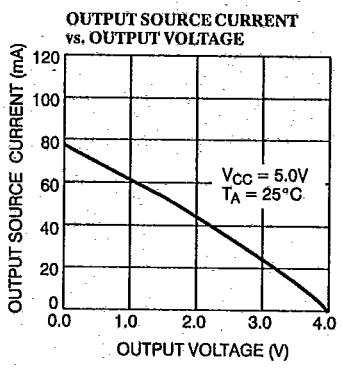
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]

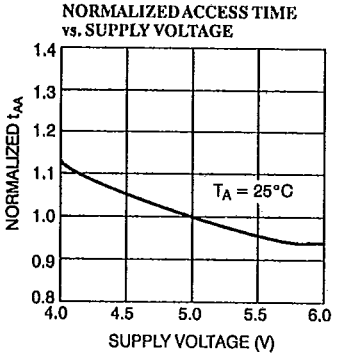


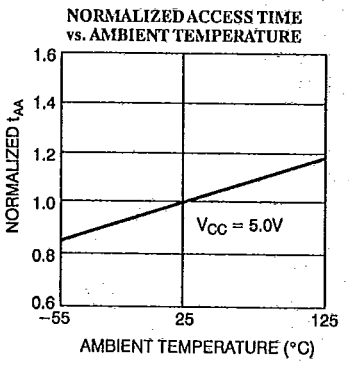
Typical DC and AC Characteristics

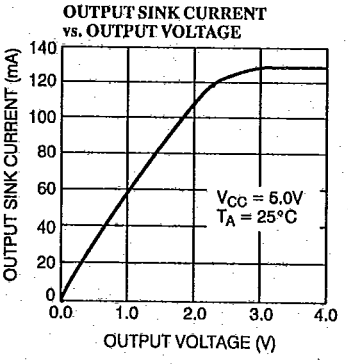






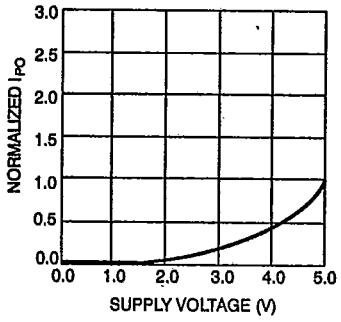




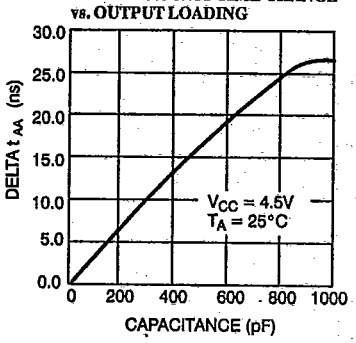


Typical DC and AC Characteristics (continued)

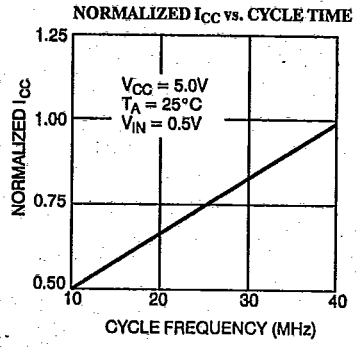
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C198–12DC	D16	Commercial
	CY7C198–12LC	L55	
	CY7C198–12PC	P15	
15	CY7C198–15DC	D16	Commercial
	CY7C198–15LC	L55	
	CY7C198–15PC	P15	
	CY7C198–15DMB	D16	Military
	CY7C198–15LMB	L55	
20	CY7C198–20DC	D16	Commercial
	CY7C198–20LC	L55	
	CY7C198–20PC	P15	
	CY7C198–20DMB	D16	Military
	CY7C198–20LMB	L55	
25	CY7C198–25DC	D16	Commercial
	CY7C198–25LC	L55	
	CY7C198–25PC	P15	
35	CY7C198–35DC	D16	Commercial
	CY7C198–35LC	L55	
	CY7C198–35PC	P15	
	CY7C198–35DMB	D16	Military
	CY7C198–35LMB	L55	
45	CY7C198–45DC	D16	Commercial
	CY7C198–45LC	L55	
	CY7C198–45PC	P15	
	CY7C198–45DMB	D16	Military
	CY7C198–45LMB	L55	
55	CY7C198–55DC	D16	Commercial
	CY7C198–55LC	L55	
	CY7C198–55PC	P15	
	CY7C198–55DMB	D16	Military
	CY7C198–55LMB	L55	

Shaded area contains advanced information.

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C199–12DC	D22	Commercial
	CY7C199–12LC	L54	
	CY7C199–12PC	P21	
	CY7C199–12VC	V21	
15	CY7C199–15DC	D22	Commercial
	CY7C199–15LC	L54	
	CY7C199–15PC	P21	
	CY7C199–15VC	V21	
	CY7C199–15DMB	D22	Military
	CY7C199–15KMB	K74	
	CY7C199–15LMB	L54	
20	CY7C199–20DC	D22	Commercial
	CY7C199–20LC	L54	
	CY7C199–20PC	P21	
	CY7C199–20VC	V21	
	CY7C199–20DMB	D22	Military
	CY7C199–20KMB	K74	
	CY7C199–20LMB	L54	
25	CY7C199–25DC	D22	Commercial
	CY7C199–25LC	L54	
	CY7C199–25PC	P21	
	CY7C199–25VC	V21	
25	CY7C199–25DMB	D22	Military
	CY7C199–25KMB	K74	
	CY7C199–25L54	L54	
35	CY7C199–35DC	D22	Commercial
	CY7C199–35LC	L54	
	CY7C199–35PC	P21	
	CY7C199–35VC	V21	
	CY7C199–35DMB	D22	Military
	CY7C199–35KMB	K74	
	CY7C199–35LMB	L54	
45	CY7C199–45DC	D22	Commercial
	CY7C199–45LC	L54	
	CY7C199–45PC	P21	
	CY7C199–45VC	V21	
	CY7C199–45DMB	D22	Military
	CY7C199–45KMB	K74	
	CY7C199–45LMB	L54	
55	CY7C199–55DC	D22	Commercial
	CY7C199–55LC	L54	
	CY7C199–55PC	P21	
	CY7C199–55VC	V21	
	CY7C199–55DMB	D22	Military
	CY7C199–55KMB	K74	
	CY7C199–55LMB	L54	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38–00077–I