

MOS FIELD EFFECT TRANSISTOR

2SK3433

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3433 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Super low on-state resistance:

RDS(on)1 = $26 \text{ m}\Omega$ MAX. (VGS = 10 V, ID = 20 A)

- ★ RDS(on)2 = 41 m Ω MAX. (Vgs = 4.0 V, ID = 20 A)
 - Low Ciss: Ciss = 1500 pF TYP.
 - Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	Drain to Source Voltage	V _{DSS}	60	V
* *+	Gate to Source Voltage	Vgss	±20	V
	Drain Current (DC)	I _{D(DC)}	±40	Α
	Drain Current (pulse) Note1	I _{D(pulse)}	±160	Α
*	Total Power Dissipation (Tc = 25°C)	Рт	47	W
	Total Power Dissipation (T _A = 25°C)	Рт	1.5	W
	Channel Temperature	Tch	150	°C
	Storage Temperature	T _{stg}	-55 to +150	°C
*	Single Avalanche Current Note2	las	21	Α
*	Single Avalanche Energy Note2	Eas	44	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V

2 Ctarting T. 25 % D. 25 % V.-. 2

ORDERING INFORMATION

PART NUMBER	PACKAGE	
2SK3433	TO-220AB	
2SK3433-S	TO-262	
2SK3433-Z	TO-220SMD	

(TO-220AB)



(TO-262)



(TO-220SMD)



THERMAL RESISTANCE

*	Channel to Case	Rth(ch-C)	2.66	°C/W
	Channel to Ambient	Rth(ch-A)	83.3	°C/W

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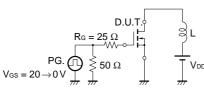
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

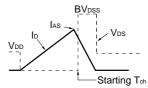


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

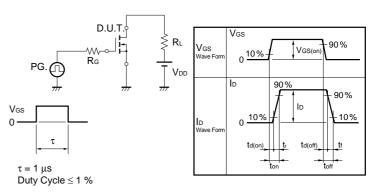
	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain to Source On-state Resistance	RDS(on)1	V _G s = 10 V, I _D = 20 A		22	26	mΩ
*		RDS(on)2	Vgs = 4.0 V, ID = 20 A		29	41	mΩ
	Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
*	Forward Transfer Admittance	y fs	V _{DS} = 10 V, I _D = 20 A	11	22		S
	Drain Leakage Current	loss	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
	Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
	Input Capacitance	Ciss	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		1500		pF
	Output Capacitance	Coss			250		pF
	Reverse Transfer Capacitance	Crss			120		pF
*	Turn-on Delay Time	td(on)	ID = 20 A, VGS(on) = 10 V, VDD = 30 V,		35		ns
*	Rise Time	t r	$R_G = 10 \Omega$		320		ns
*	Turn-off Delay Time	td(off)			89		ns
*	Fall Time	t f			120		ns
	Total Gate Charge	Q _G	ID = 40 A , VDD = 48 V, VGS = 10 V		30		nC
	Gate to Source Charge	Qgs			5		nC
	Gate to Drain Charge	Q _{GD}			8		nC
	Body Diode Forward Voltage	V _{F(S-D)}	IF = 40 A, VGS = 0 V		1.0		V
*	Reverse Recovery Time	trr	IF = 40 A, VGS = 0 V,		44		ns
*	Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		60		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY





TEST CIRCUIT 2 SWITCHING TIME

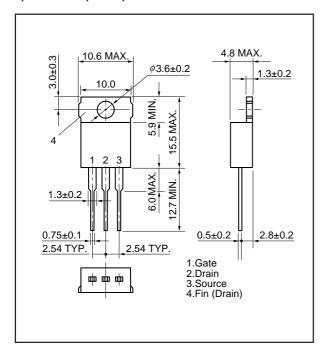


TEST CIRCUIT 3 GATE CHARGE

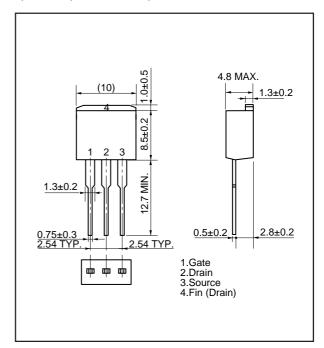


PACKAGE DRAWINGS (Unit: mm)

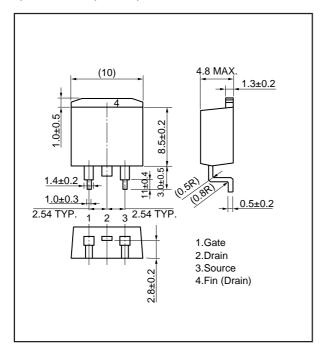
1) TO-220AB (MP-25)



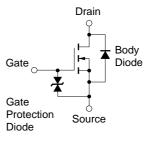
2) TO-262 (MP-25 Fin Cut)



3) TO-220SMD (MP-25Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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