

TC74ACT00P, TC74ACT00F, TC74ACT00FN, TC74ACT00FT

QUAD 2-INPUT NAND GATE

The TC74ACT00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

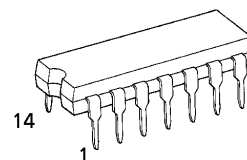
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

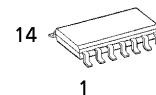
FEATURES:

- High Speed..... $t_{pd} = 4.0\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs... $V_{IL} = 0.8\text{V}(\text{Max.})$
 $V_{IH} = 2.0\text{V}(\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F00

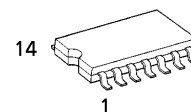
(Note) The JEDEC SOP (FN) is not available in Japan.



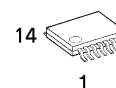
P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

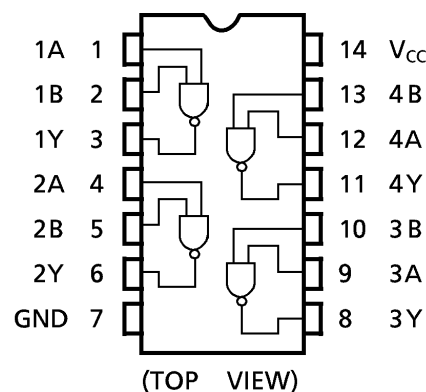


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

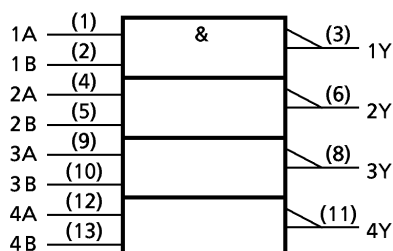


FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	$0 \sim 10$	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		$4.5 \begin{Bmatrix} \\ 5.5 \end{Bmatrix}$	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}		$4.5 \begin{Bmatrix} \\ 5.5 \end{Bmatrix}$	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\mu\text{A}$ $I_{OH} = -24\text{mA}$ $I_{OH} = -75\text{mA}^*$	$4.5 \begin{Bmatrix} 4.5 \\ 5.5 \end{Bmatrix}$	$4.4 \begin{Bmatrix} 3.94 \\ - \end{Bmatrix}$	$4.5 \begin{Bmatrix} - \\ - \end{Bmatrix}$	$- \begin{Bmatrix} - \\ - \end{Bmatrix}$	$4.4 \begin{Bmatrix} 3.80 \\ 3.85 \end{Bmatrix}$	$- \begin{Bmatrix} - \\ - \end{Bmatrix}$	V
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ $I_{OL} = 50\mu\text{A}$ $I_{OL} = 24\text{mA}$ $I_{OL} = 75\text{mA}^*$	$4.5 \begin{Bmatrix} 4.5 \\ 5.5 \end{Bmatrix}$	$- \begin{Bmatrix} - \\ - \end{Bmatrix}$	$0.0 \begin{Bmatrix} - \\ - \end{Bmatrix}$	$0.1 \begin{Bmatrix} 0.36 \\ - \end{Bmatrix}$	$- \begin{Bmatrix} - \\ - \end{Bmatrix}$	$0.1 \begin{Bmatrix} 0.44 \\ 1.65 \end{Bmatrix}$	V
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA
	I_C	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT : V_{CC} or GND	5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH} t _{pHL}		5.0 ± 0.5	—	4.7	7.9	1.0	9.5	ns
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	23	—	—	—	

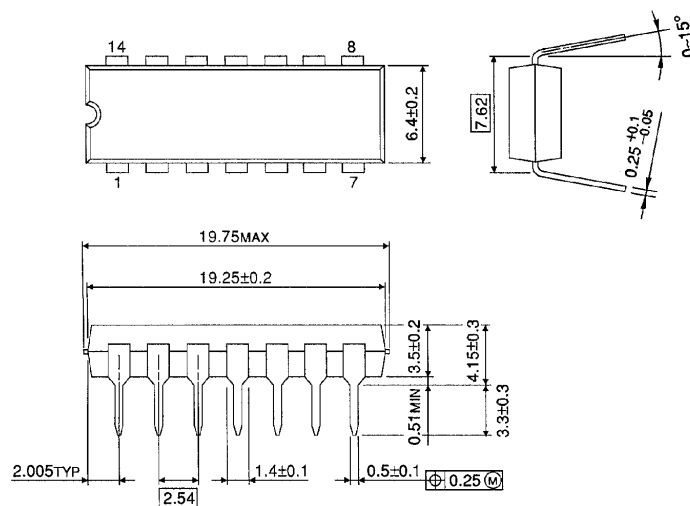
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

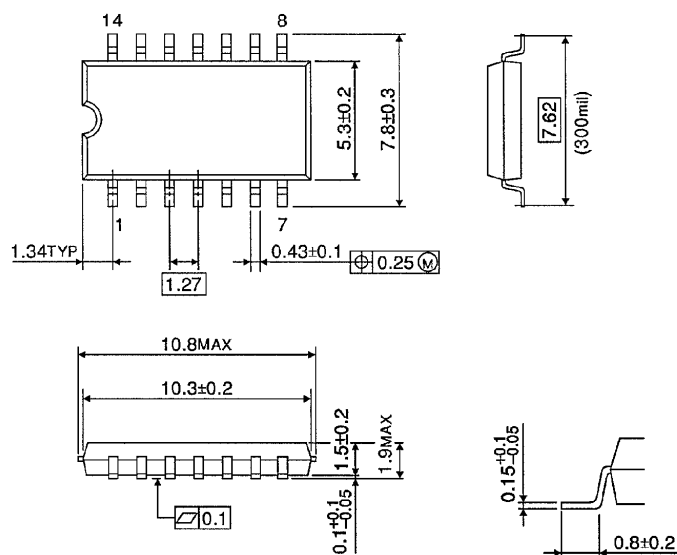
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

Unit in mm

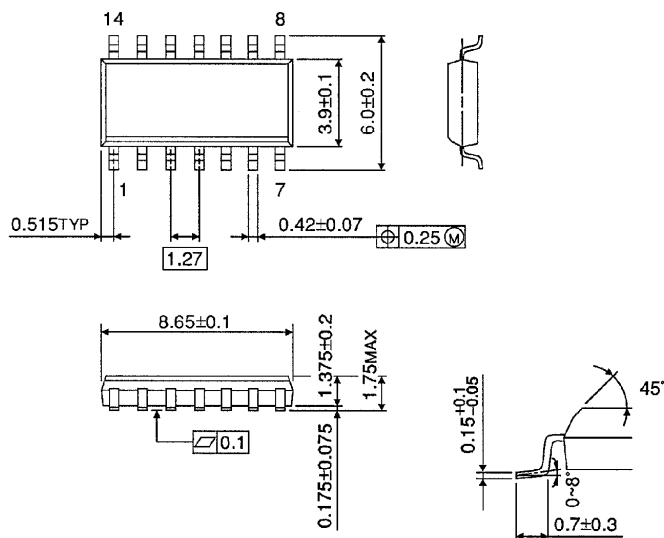


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

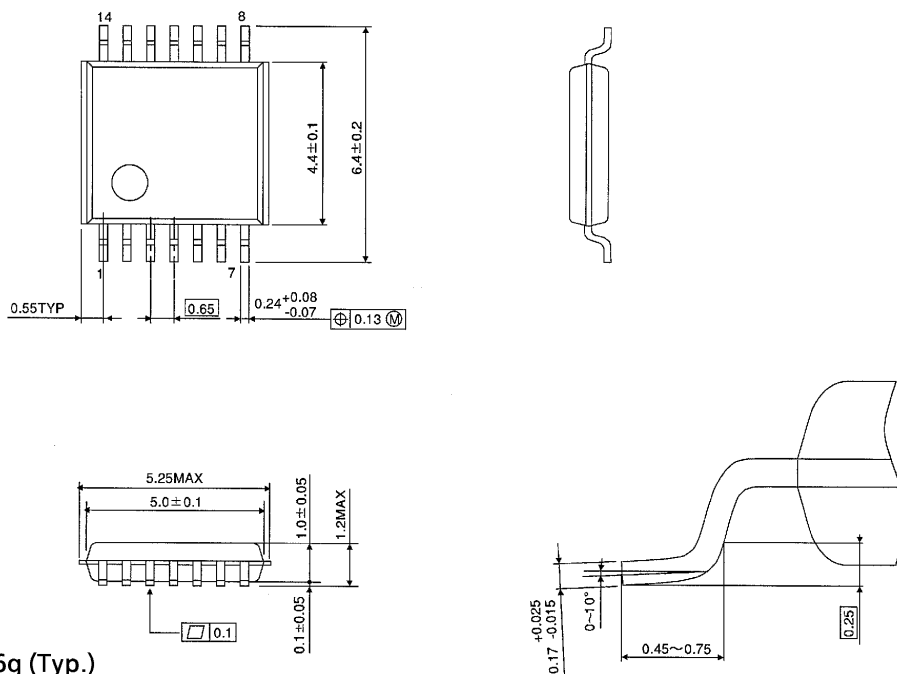
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) OUTLINE DRAWING (TSSOP14-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)