

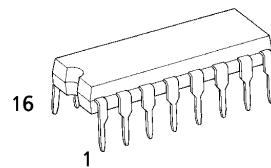
TC74HC174AP, TC74HC174AF, TC74HC174AFN**HEX D-TYPE FLIP FLOP WITH CLEAR**

(Note) The JEDEC SOP (FN) is not available in Japan.

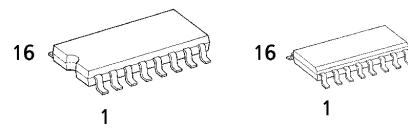
The TC74HC174A is a high speed CMOS D - TYPE FLIP FLOP fabricated with silicon gate C2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the \overline{CLR} input is held low, the Q outputs are in the low logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

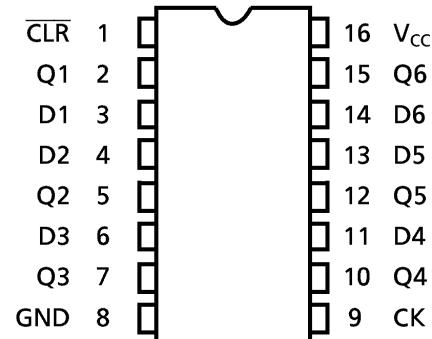
- High Speed..... $f_{MAX} = 71\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Symmetrical Output Impedance..... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS174



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27) FN (SOL16-P-150-1.27)
Weight : 0.18g (Typ.) Weight : 0.13g (Typ.)

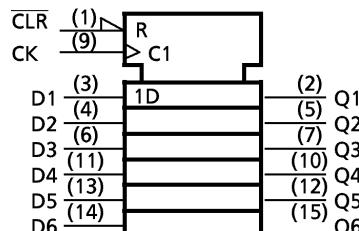
PIN ASSIGNMENT

(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
CLR	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q _n	NO CHANGE

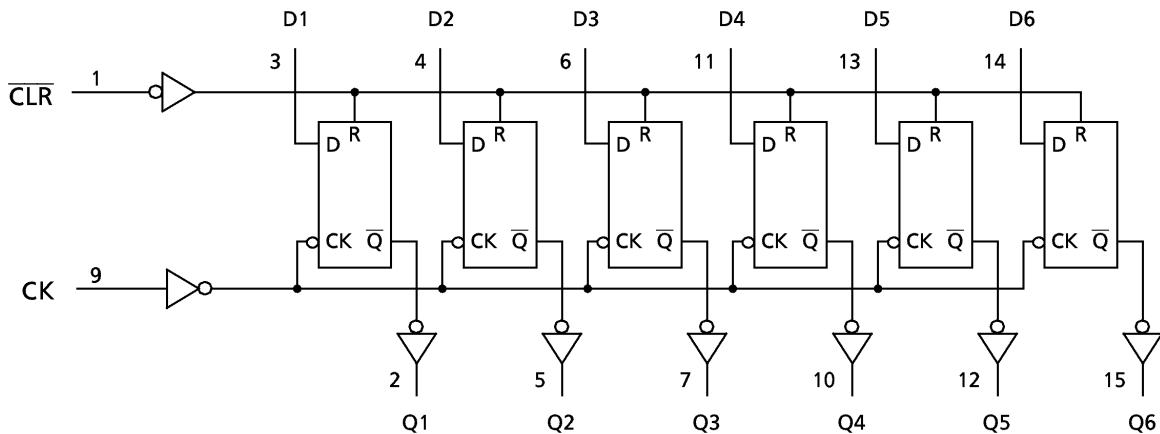
X : Don't Care

IEC LOGIC SYMBOL

961001EBA2

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 ($V_{CC} = 2.0\text{V}$) 0~ 500 ($V_{CC} = 4.5\text{V}$) 0~ 400 ($V_{CC} = 6.0\text{V}$)	ns

961001EBA2'

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —
			$I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu A$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1
			$I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C		UNIT
				TYP.	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	95 19 16	ns
			2.0 4.5 6.0	— — —	75 15 13	95 19 16	95 19 16	
Minimum Set-up Time	t_s		2.0 4.5 6.0	— — —	75 15 13	95 19 16	95 19 16	ns
			2.0 4.5 6.0	— — —	0 0 0	0 0 0	0 0 0	
Minimum Hold Time	t_h		2.0 4.5 6.0	— — —	25 5 4	30 6 5	30 6 5	MHz
			2.0 4.5 6.0	— — —	6 33 38	4 26 30	4 26 30	
Clock Frequency	f							

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		—	14	26	
Propagation Delay Time (CLR-Q)	t_{pHL}		—	15	26	
Maximum Clock Frequency	f_{MAX}		39	71	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$		$T_a = -40\text{--}85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	27	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		2.0	—	68	150	—	190
			4.5	—	17	30	—	38
			6.0	—	14	26	—	32
Propagation Delay Time (CLR-Q)	t_{pHL}		2.0	—	72	150	—	190
			4.5	—	18	30	—	38
			6.0	—	15	26	—	32
Maximum Clock Frequency	f_{MAX}		2.0	6	15	—	4	MHz
			4.5	33	59	—	26	
			6.0	38	71	—	30	
Input Capacitance	C_{IN}		—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$		—	40	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

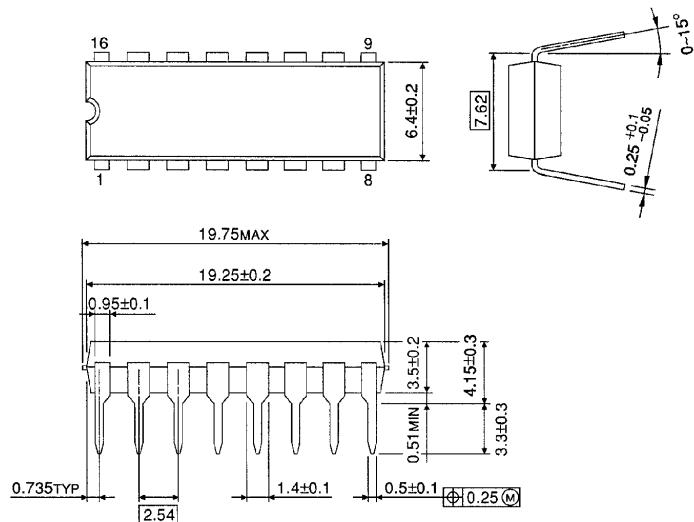
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 28 + 12 \cdot n$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

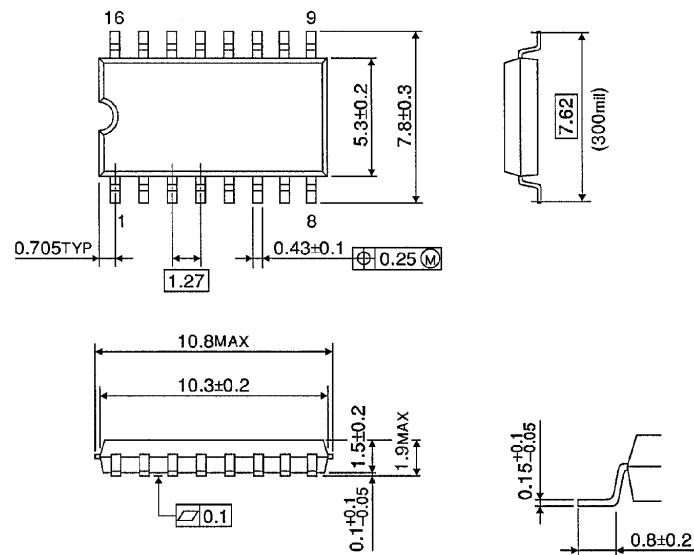
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

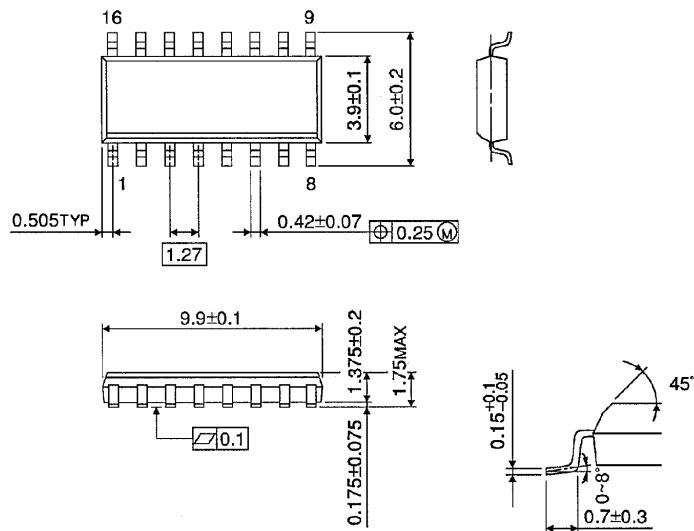


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)