TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95C001

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP95C001F

1. Outline and Features

TMP95C001F is a 16-bit microcontroller of a high-speed 16-bit CPU (TLCS-900/H) core. It has only an indispensable function such as a wait controller, an interrupt controller, and etc.

TMP95C001F is presented in a 64-pin flat package. Its features are as follows.

(1) High-speed 16-bit CPU (TLCS-900/H_CPU)
- Instruction mnemonics upwardly compatible with TLCS-90/900
- 16M-byte linear address space
- General-purpose registers using register bank system
- 16-bit multiplication / division instructions, bit transfer / arithmetic instructions
- Micro DMA: four channels (640 ns / 2 bytes at 25 MHz)

(2) Minimum instruction execution time: 160 ns (at 25 MHz)

(3) Internal RAM : No
Internal ROM : No

(4) External memory expansion
- Expandable to 16 Mbytes (common to programs and data)
- External data bus width selection pin (AM8 / $\overline{16}$)
- Can use both 8- and 16-bit external buses··· dynamic bus sizing

(5) Wait controller : four blocks

(6) Interrupt function
- Interrupt sources : 20
  (Internal interrupt : 13
  External interrupt : 7)

(7) Standby function
Three HALT modes (RUN, IDLE, STOP)

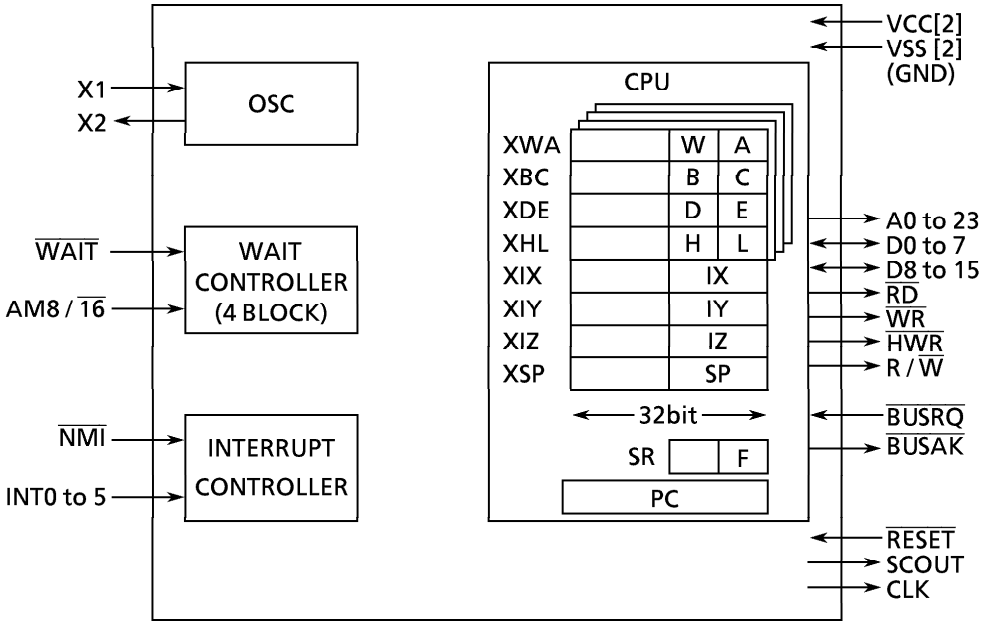


Figure 1 TMP95C001 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for TMP95C001F their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP95C001F.

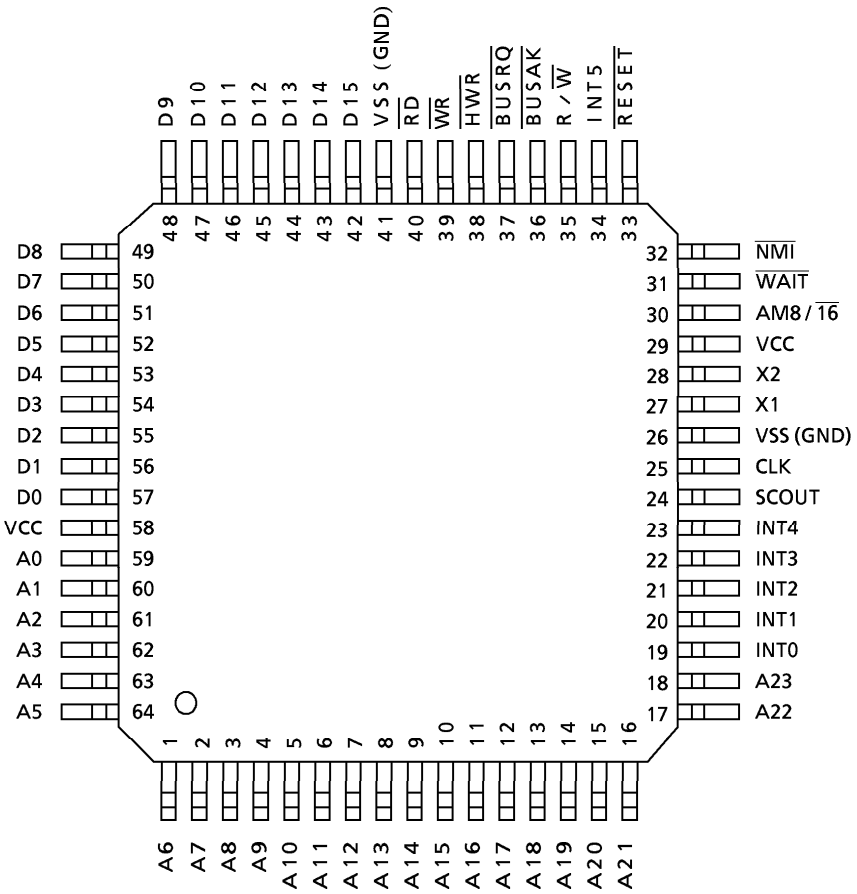
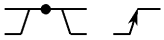
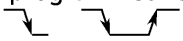


Figure 2.1 Pin Assignment (64-pin QFP)

2.2 Pin Names and Functions

Table 2.2 shows the I/O pin names and their functions.

Table 2.2 Pin Names and Functions

Pin Name	Pin Number	Input / Output	Function
D0 to D15	16	Input / Output	Data : Data bus 0 to 15
A0 to A23	24	Output	Address : Address bus 0 to 23
$\overline{RD}$	1	Output	Read : Strobe signal to read external memory Setting RSRAM mode outputs $\overline{RD}$ even when reading internal areas.
$\overline{WR}$	1	Output	Write : Strobe signal to write data of pins D0 to 7.
$\overline{HWR}$	1	Output	Upper write: Strobe signal for writing data of pins D8 to 15.
$\overline{BUSRQ}$	1	Input	Input Bus request: Signal to request external bus release.
$\overline{BUSAK}$	1	Output	Bus acknowledge: Signal to indicate external bus is released after receiving $\overline{BUSRQ}$.
R / $\overline{W}$	1	Output	Read/write: "1" indicates read or dummy cycle; "0" indicates write cycle.
SCOUT	1	Output	System clock output: Outputs system clock (external clock divided by 2).
$\overline{WAIT}$	1	Input	Wait: CPU bus wait request pin. (enabled in 1 + N or 0 + N WAIT mode).
INT0	1	Input	Interrupt request pin 0: Can be programmed for level or rising-edge detection. 
INT1 to 4	4	Input	Interrupt request pin 1 to 4: Rising-edge interrupt request pin
INT5	1	Input	Interrupt request pin 5: Can be programmed for level or rising-edge detection. 
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Can be programmed for falling-edge or falling-rising-edge detection. 
CLK	1	Output	Clock output: Outputs external input clock X1 divided by 4. Pulled up during reset.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width selection pin. Set to 0 when using fixed 16-bit external bus or dual 8/16-bit external bus. Set to 1 with 8-bit external bus fixed.
$\overline{RESET}$	1	Input	Reset: Initializes TMP95C001. (with pull-up)
X1 / X2	2	Input / Output	Oscillator connecting pins
VCC	2		Power supply pin (All Vcc pins should be connected with the power supply pin.)
VSS (GND)	2		Ground pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Connect all VCC pins to power supply and all VSS pins to GND.

3. Operation

The following is a block-by-block description of the functions and basic operation of TMP95C001.

Note that the description concludes with cautions and restrictions for each block in 7, Usage Cautions and Restrictions.

3.1 CPU

TMP95C001 contains an advanced, high-speed 16-bit CPU (the TLCS-900/H_CPU). The CPU is described in the TLCS-900 CPU section in the previous chapter.

The following describes the CPU functions unique to TMP95C001 that are not described in "TLCS-900 CPU".

3.1.1 Reset Operation

Figure 3.1 (1) shows reset timing.

At TMP95C001 reset, the power supply voltage must be within the operating range and internal oscillation must be stable. Set the $\overline{\text{RESET}}$ input to 0 for at least ten system clocks (= 10 states: 0.8 μs for a 25-MHz clock).

When the reset is accepted, the CPU:

- Sets the program counter (PC) to the reset vector stored at addresses FFFF00H to FFFF02H.
  PC (7 : 0) ← value at address FFFF00H
  PC (15 : 8) ← value at address FFFF01H
  PC (23 : 16) ← value at address FFFF02H
- Sets the stack pointer (XSP) to 100H
- Sets bits IFF2 to 0 of the status register (SR) to 111 (this sets the interrupt level mask register to level 7).
- Sets the MAX bit of the status register (SR) to 1 (this sets maximum mode). (Note: This product does not support minimum mode. Do not set the MAX bit to 0.)
- Clears bits RFP2 to 0 of the status register (SR) to 000 (this sets the register banks to 0).

After reset is released, the CPU begins execution from the instruction at the location specified in the PC. Other than the changes described above, reset does not alter any internal CPU registers.

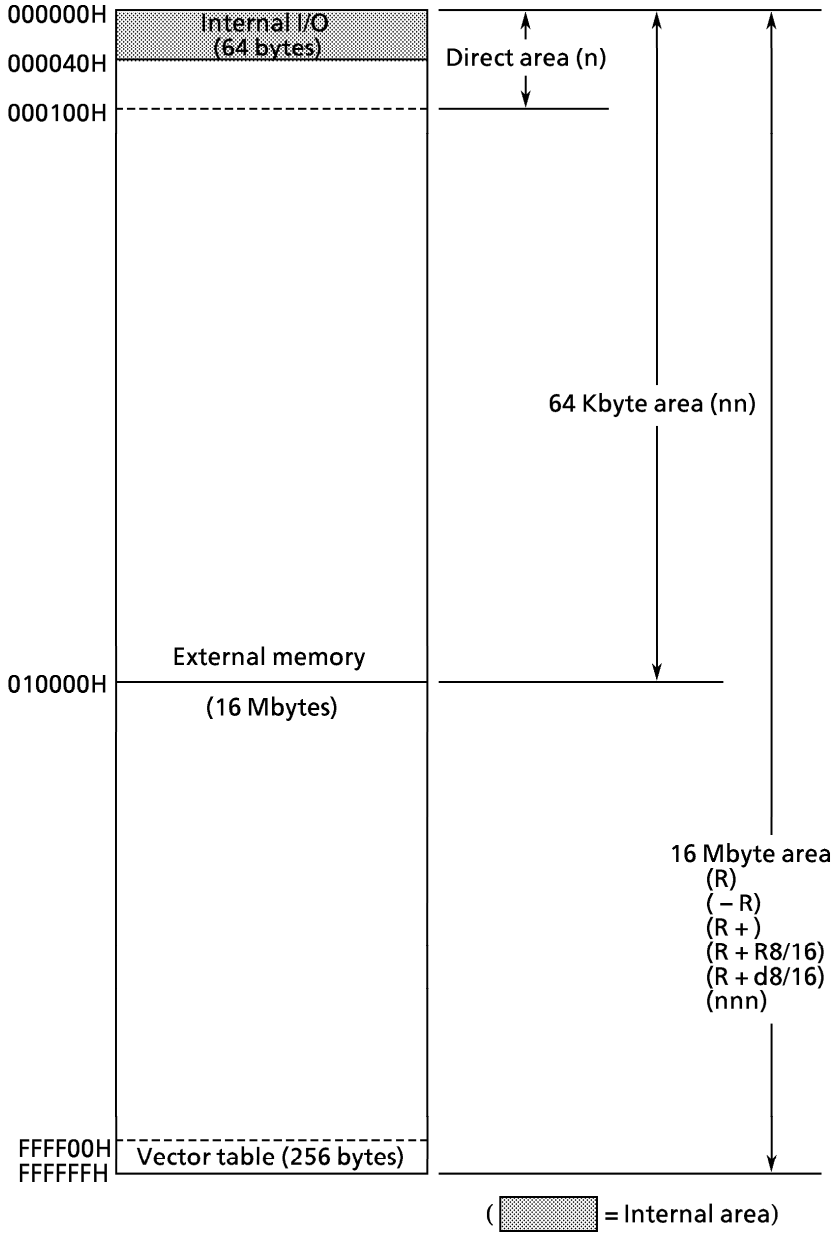
When reset is accepted, processing of the internal I/O and other pins are as follows:

- Initializes the internal I/O registers as per specifications.
- Pulls up the clock pin to 1.

3.2 Memory Map

TMP95C001 uses an address area of 64 bytes as an internal I/O area. This is allocated at addresses 000000H to 00003FH. The CPU can also access this internal I/O using a short instruction code according to "direct addressing mode".

Figure 3.2 shows an accessing area in the respective addressing modes for the memory map and the CPU.



Note : After reset, the stack pointer (XSP) is set to 100H.

Figure 3.2 TMP95C001 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5 to 6.5	V
Input voltage	V_{IN}	− 0.5 to Vcc + 0.5	V
Output current (total)	ΣI_{OL}	+ 120	mA
Output current (total)	ΣI_{OH}	− 120	mA
Power dissipation (Ta = 70°C)	P_D	400	mW
Soldering temperature (10 s)	T_{SOLDER}	+ 260	°C
Storage temperature	T_{STG}	− 65 to 150	°C
Operating temperature	T_{OPR}	− 20 to 70	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

(Typ values are for Ta = + 25°C and Vcc = + 5 V)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) INT1 to 5, BUSRQ, WAIT RESET, NMI, INT0 AM8/16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}		−0.3 −0.3 −0.3 −0.3 −0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2Vcc	V V V V V
Input High Voltage (D0 to 15) INT1 to 5, BUSRQ, WAIT RESET, NMI, INT0 AM8/16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}		2.2 0.7 Vcc 0.75 Vcc Vcc − 0.3 0.8Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH} V_{OH1} V_{OH2}	I_{OH} = − 400 μA I_{OH} = − 100 μA I_{OH} = − 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I_{DAR}	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ	−1.0	− 3.5	mA
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc − 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = − 20 to 70°C) STOP (Ta = 0 to 50°C)	I_{CC}	fc = 25 MHz 0.2 ≦ Vin ≦ Vcc − 0.2 0.2 ≦ Vin ≦ Vcc − 0.2	20 (Typ) 3.5 (Typ) 0.5 (Typ)	30 10 50 10	mA mA μA μA
Power Down Voltage (at STOP)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistance	R_{RST}		50	250	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0	V_{TH}		0.4	1.0 (Typ)	V

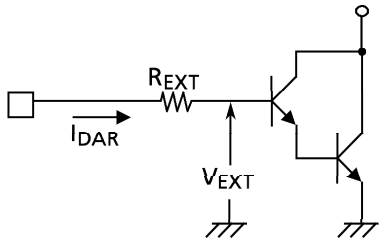
Note: I_{DAR} is guaranteed for total of up to 8 ports.

(2) Vcc = + 3 V ± 10%, Ta = – 20~ + 70°C (fc = 4 to 12.5 MHz)

(Typ values are for Ta = + 25°C and Vcc = + 3 V)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) INT1 to 5, BUSRQ, WAIT RESET, NMI, INT0 AM8/16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}		–0.3 –0.3 –0.3 –0.3 –0.3	0.6 0.3 Vcc 0.25 Vcc 0.3 0.2Vcc	V V V V V
Input High Voltage (D0 to 15) INT1 to 5, BUSRQ, WAIT RESET, NMI, INT0 AM8/16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}		2.0 0.7 Vcc 0.75 Vcc Vcc – 0.3 0.8Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH}	I_{OH} = – 400 μA	2.4		V
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc – 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE STOP (Ta = – 20 to 70°C) STOP (Ta = 0 to 50°C)	I cc	fc = 12.5 MHz 0.2 ≦ Vin ≦ Vcc – 0.2 0.2 ≦ Vin ≦ Vcc – 0.2	5.0 (Typ) 0.9 (Typ) 0.5 (Typ)	9.0 1.8 50 10	mA mA μA μA
Power Down Voltage (at STOP)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
RESET Pull Up Resistance	R_{RST}		80	500	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0	V_{TH}		0.4	1.0 (Typ)	V

(Reference) Definition of I_{DAR}



4.3 AC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = – 20 to + 70℃

(fc = 8 MHz to 25 MHz)

No.	Parameter	Symbol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	40	125	50		40		ns
2	Clock pulse width	t_{CLK}	2x – 40		60		40		ns
3	A0 to A23 valid→ clock hold	t_{AK}	0.5x – 20		5		0		ns
4	Clock valid→ A0 to A23 hold	t_{KA}	1.5x – 60		5		0		ns
5	A0 to A23 valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{AC}	1.0x – 20		30		20		ns
6	$\overline{RD}$/$\overline{WR}$ rise→ A0 to A23 hold	t_{CA}	0.5x – 20		5		0		ns
7	A0 to A23 valid→ D0 to D15 input	t_{AD}		3.5x – 35		140		105	ns
8	$\overline{RD}$ fall→ D0 to D15 input	t_{RD}		2.5x – 40		85		60	ns
9	$\overline{RD}$ Low pulse width	t_{RR}	2.5x – 40		85		60		ns
10	$\overline{RD}$ rise→ D0 to D15 hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ Low pulse width	t_{WW}	2.5x – 40		85		60		ns
12	D0 to D15 valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 40		60		40		ns
13	$\overline{WR}$ rise →D0 to D15 hold	t_{WD}	0.5x – 10		15		10		ns
14	A0 to A23 valid→ $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AW}		3.5x – 90		85		50	ns
	A0 to A23 valid→ $\overline{WAIT}$ input (0 WAIT + n mode)	t_{AW}		1.5x – 40		35		20	ns
15	$\overline{RD}$/$\overline{WR}$ fall→ $\overline{WAIT}$ hold (1 WAIT + n mode)	t_{CW}	2.5x + 0		125		100		ns
	$\overline{RD}$/$\overline{WR}$ fall→ $\overline{WAIT}$ hold (0 WAIT + n mode)	t_{CW}	0.5x + 0		25		20		ns

AC measuring conditions

- Output level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (Note that for D0 to D15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$,and CLK, CL = 100 pF)
- Input level : High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 Vcc / Low 0.2 Vcc (except for D0 to D15)

(2) Vcc = + 3 V ± 10%, Ta = – 20 to + 70℃

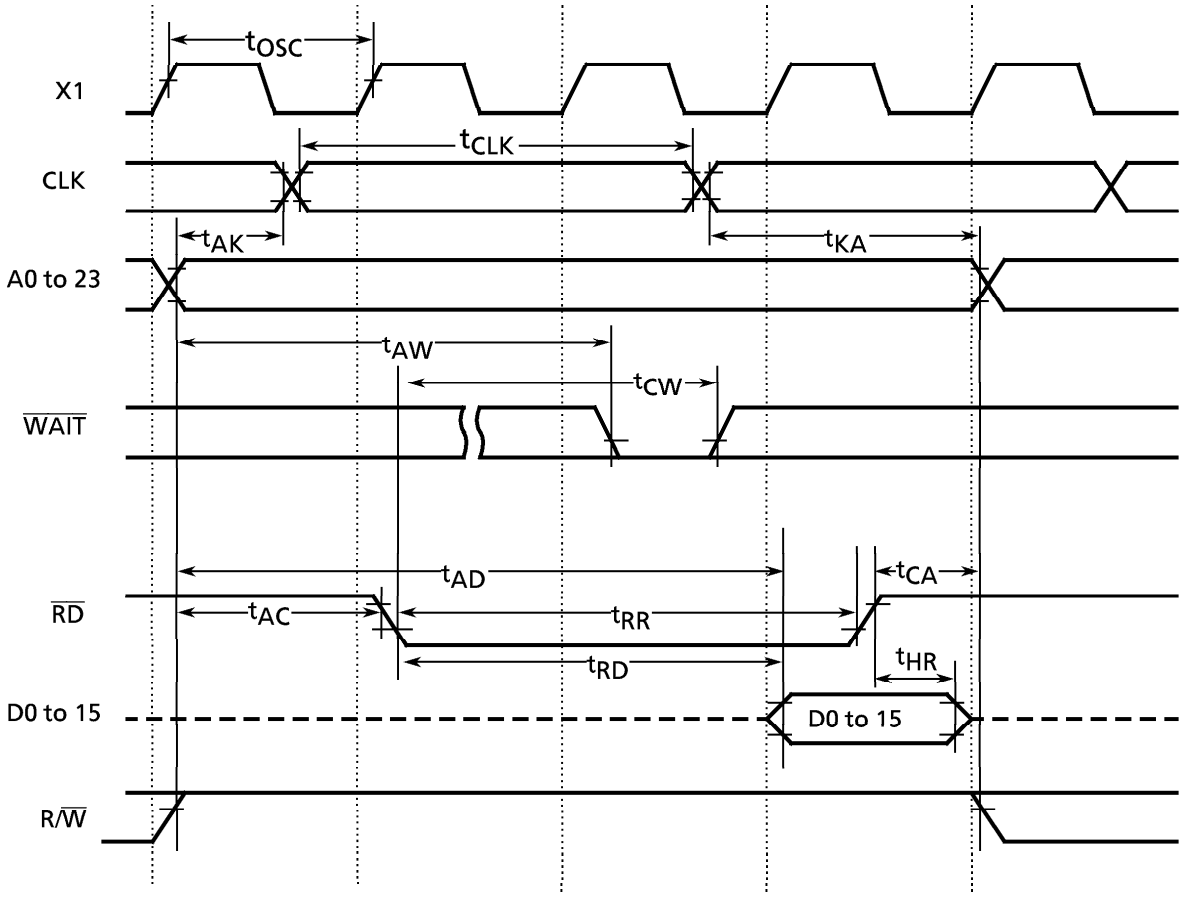
(fc = 4 MHz to 12.5 MHz)

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	80	250	80		ns
2	Clock pulse width	t_{CLK}	2x – 40		120		ns
3	A0 to A23 valid→ clock hold	t_{AK}	0.5x – 40		0		ns
4	Clock valid→ A0 to A23 hold	t_{KA}	1.5x – 80		40		ns
5	A0 to A23 valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{AC}	1.0x – 60		20		ns
6	$\overline{RD}$/$\overline{WR}$ rise→ A0 to A23 hold	t_{CA}	0.5x – 40		0		ns
7	A0 to A23 valid→ D0 to D15 input	t_{AD}		3.5x – 125		155	ns
8	$\overline{RD}$ fall →D0 to D15 input	t_{RD}		2.5x – 115		85	ns
9	$\overline{RD}$ Low pulse width	t_{RR}	2.5x – 40		160		ns
10	$\overline{RD}$ rise→ D0 to D15 hold	t_{HR}	0		0		ns
11	$\overline{WR}$ Low pulse width	t_{WW}	2.5x – 40		160		ns
12	D0 to D15 valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 60		100		ns
13	$\overline{WR}$ rise →D0 to D15 hold	t_{WD}	0.5x – 30		10		ns
14	A0 to A23 valid→ $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AW}		3.5x – 130		150	ns
	A0 to A23 valid→ $\overline{WAIT}$ input (0 WAIT + n mode)	t_{AW}		1.5x – 80		40	ns
15	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ hold (1 WAIT + n mode)	t_{CW}	2.5x + 0		200		ns
	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ hold (0 WAIT + n mode)	t_{CW}	0.5x + 0		40		ns

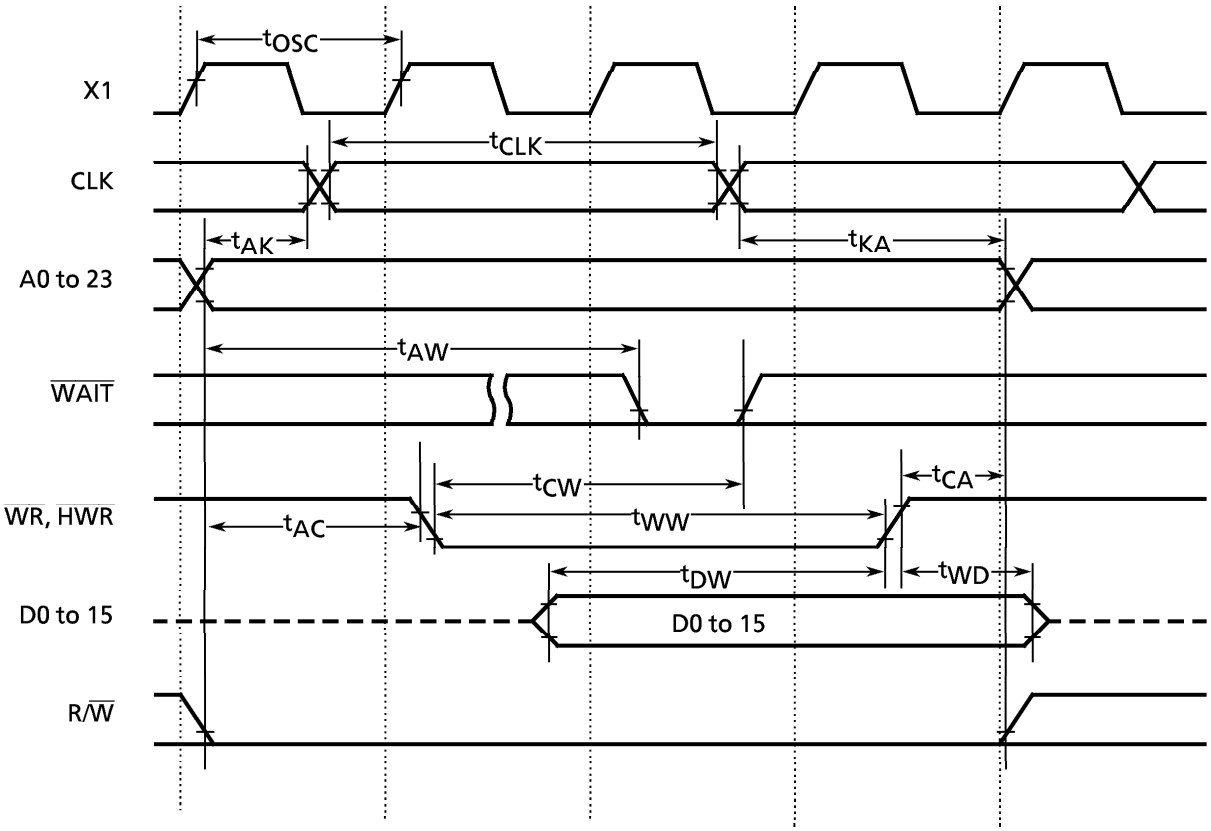
AC measuring conditions

- Output level : High 0.7 × V_{CC} / Low 0.3 × V_{CC} , CL = 50 pF
- Input level : High 0.9 × V_{CC} / Low 0.1 × Vcc

(3) Read cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
tAW
tCW
WAIT
tAD
tCA
RD
tAC
tRR
tRD
tHR
D0 to 15
D0 to 15
R/W

(4) Write cycle



4.4 SCOUT pin AC Electrical Characteristics

Ta = – 20 to + 70°C

Parameter	Symbol	Variable		12.5 MHz		25 MHz	
		Min	Max	Min	Max	Min	Max
High-level pulse width VCC = + 5 V ± 10% (fc = 8 to 25 MHz)	t_{SCH}	1x – 20		60		20	
VCC = + 3 V ± 10% (fc = 4 to 12.5 MHz)		1x – 30		50		–	–
Low-level pulse width VCC = + 5 V ± 10% (fc = 8 to 25 MHz)	t_{SCL}	1x – 20		60		20	
VCC = + 3 V ± 10% (fc = 4 to 12.5 MHz)		1x – 30		50		–	–

AC measuring conditions

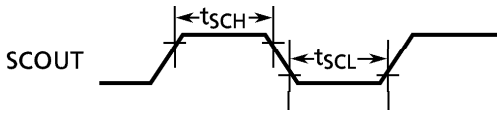
- Output level

  (1) Vcc = + 5 V ± 10%

  High 2.2 V / Low 0.8 V, CL = 30pF

  (2) Vcc = + 3 V ± 10%

  High 0.7 × Vcc / Low 0.3 × Vcc, CL = 30pF

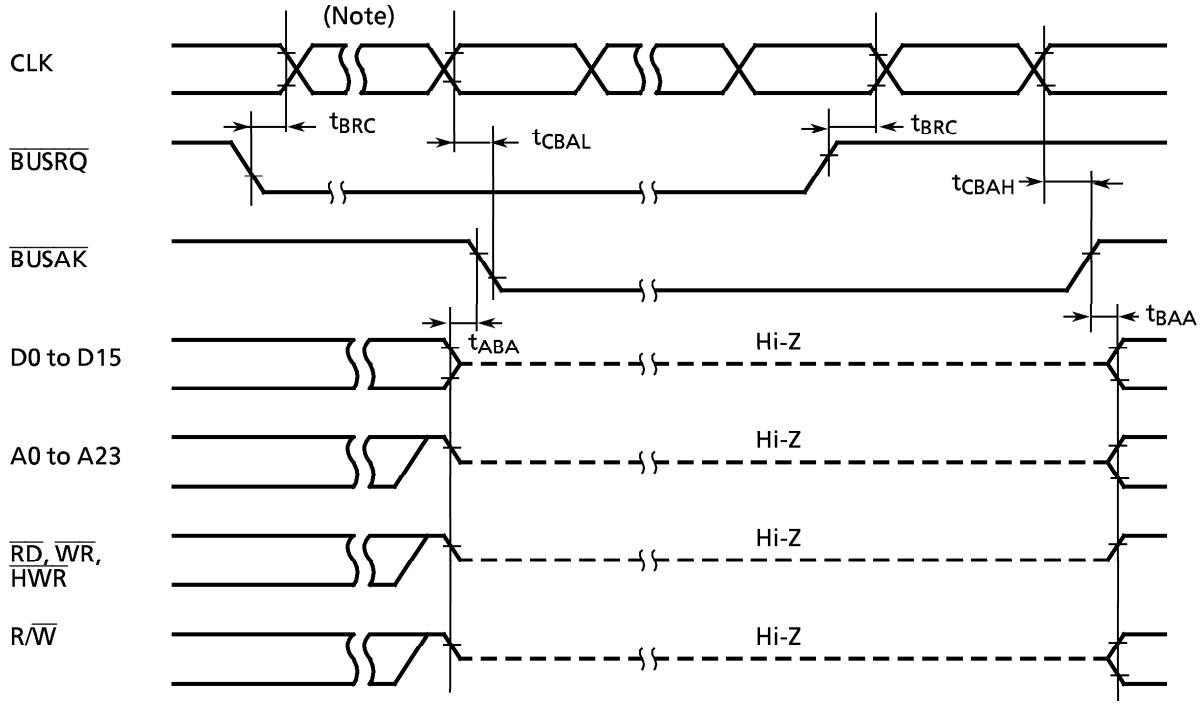


4.5 Interrupt Operation

Vcc = + 5 V ± 10%, Ta = − 20 to + 70℃ (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = − 20 to + 70℃ (fc = 4 to 12.5 MHz)

Parameter	Symbol	Variable		12.5 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$、INT0 low-level pulse width	t_{INTAL}	4x		320		160		ns
$\overline{NMI}$、INT0 high-level pulse width	t_{INTAH}	4x		320		160		ns
INT1 to INT5 low-level pulse width	t_{INTBL}	8x + 100		740		420		ns
INT1 to INT5 high-level pulse width	t_{INTBH}	8x + 100		740		420		ns

4.6 Bus Request/Bus Acknowledge Timing



Vcc = + 5 V ± 10%, Ta = − 20 to + 70℃ (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = − 20 to + 70℃ (fc = 4 to 12.5 MHz)

Parameter	Symbol	Variable		12.5 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time for CLK	t_{BRC}	120		120		120		ns
CLK→$\overline{BUSAK}$ fall	t_{CBAL}		2.0x + 120		280		200	ns
CLK→$\overline{BUSAK}$ rise	t_{CBAH}		0.5x + 40		80		60	ns
Time from output buffer off until $\overline{BUSAK}$ fall	t_{ABA}	0	80	0	80	0	80	ns
Time from $\overline{BUSAK}$ rise until output buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note: When bus release is requested with $\overline{BUSRQ}$ cleared to 0, that request cannot be granted until the previous bus cycle is terminated by a WAIT, and the WAIT is released.