

# SPANSION™ MCP

## Data Sheet



September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

### **Continuity of Specifications**

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

### **Continuity of Ordering Part Numbers**

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

### **For More Information**

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.



3 Stacked MCP (Multi-Chip Package) FLASH & FLASH & FCRAM

CMOS

**64M (×16) FLASH MEMORY &  
32M (×16) FLASH MEMORY &  
32M (×16) Mobile FCRAM™**

**MB84VF5F4F4J1-70**

## ■ FEATURES

- Power supply voltage of 2.7 V to 3.1 V
- High performance
  - 70 ns maximum access time (Flash\_1: 64 Mb Falsh)
  - 70 ns maximum access time (Flash\_2 : 32 Mb Falsh)
  - 65 ns maximum access time (FCRAM : 32 Mb FCRAM)
- Operating Temperature
  - 30 °C to +85 °C
- Package 107-ball FBGA

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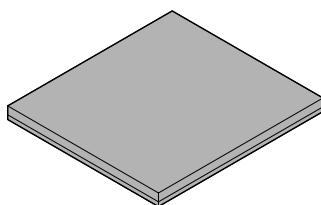
## ■ PRODUCT LINEUP

|                                             | Flash_1                               | Flash_2                               | FCRAM                               |
|---------------------------------------------|---------------------------------------|---------------------------------------|-------------------------------------|
| Supply Voltage (V)                          | V <sub>ccf_1</sub> * = 2.7 V to 3.1 V | V <sub>ccf_2</sub> * = 2.7 V to 3.1 V | V <sub>ccr</sub> * = 2.7 V to 3.1 V |
| Max Address Access Time (ns)                | 70                                    | 70                                    | 65                                  |
| Max $\overline{\text{CE}}$ Access Time (ns) | 70                                    | 70                                    | 65                                  |
| Max $\overline{\text{OE}}$ Access Time (ns) | 30                                    | 30                                    | 40                                  |

\* : All of V<sub>ccf\_1</sub>, V<sub>ccf\_2</sub>, and V<sub>ccr</sub> must be the same level when either part is being accessed.

## ■ PACKAGE

107-ball plastic FBGA



BGA-107P-M01

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## 1. FLASH MEMORY\_1 & \_2

- **Simultaneous Read/Write Operations (Dual Bank)**

- **Flash\_1 FlexBank™ \*1**

Bank A : 8 Mbit (8 KB × 8 and 64 KB × 15)

Bank B : 24 Mbit (64 KB × 48)

Bank C : 24 Mbit (64 KB × 48)

Bank D : 8 Mbit (8 KB × 8 and 64 KB × 15)

- **Flash\_2 FlexBank™**

Bank A : 4 Mbit (8 KB × 8 and 64 KB × 7)

Bank B : 12 Mbit (64 KB × 24)

Bank C : 12 Mbit (64 KB × 24)

Bank D : 4 Mbit (64 KB × 8)

Two virtual Banks are chosen from the combination of four physical banks.

Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.

Read-while-erase

Read-while-program

- **Minimum 100,000 Program/Erase Cycles**

- **Sector Erase Architecture**

Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.

Any combination of sectors can be concurrently erased. It also supports full chip erase.

- **HiddenROM (HiddenROM) Region**

256 byte of HiddenROM, accessible through a new "HiddenROM Enable" command sequence

Factory serialized and protected to provide a secure electronic serial number (ESN)

- **WP/ACC Input Pin**

At  $V_{IL}$ , allows protection of "outermost"  $2 \times 8$  Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status

At  $V_{IH}$ , allows removal of boot sector protection

At  $V_{ACC}$ , increases program performance

- **Embedded Erase™ \*2 Algorithms**

Automatically preprograms and erases the chip or any sector

- **Embedded Program™ \*2 Algorithms**

Automatically writes and verifies data at specified address

- **Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**

- **Ready/Busy Output (RY/ $\overline{BY}$ \_1 or RY/ $\overline{BY}$ \_2)**

Hardware method for detection of program or erase cycle completion

- **Automatic Sleep Mode**

When addresses remain stable, the device automatically switches itself to low power mode.

- **Low  $V_{ccf}$  write inhibit  $\leq 2.5$  V**

- **Program Suspend/Resume**

Suspends the program operation to allow a read in another byte

- **Erase Suspend/Resume**

Suspends the erase operation to allow a read data and/or program in another sector within the same device

- **Please Refer to "MBM29DL64DF" Datasheet in Detailed Function for Flash\_1.**

- **Please Refer to "MBM29DL32BF" Datasheet in Detailed Function for Flash\_2.**

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## 2. FCRAM™ \*3

- **Power Dissipation**

Operating : 25 mA Max

Standby : 100 µA Max

- **Power Down Mode**

Sleep : 10 µA Max

NAP : 60 µA Max

8M Partial : 70 µA Max

- **Power Down Control by CE2r**

- **Byte Write Control:  $\overline{\text{LB}}(\text{DQ}_7\text{-DQ}_0)$ ,  $\overline{\text{UB}}(\text{DQ}_{15}\text{-DQ}_8)$**

- **8 words Address Access Capability**

\*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

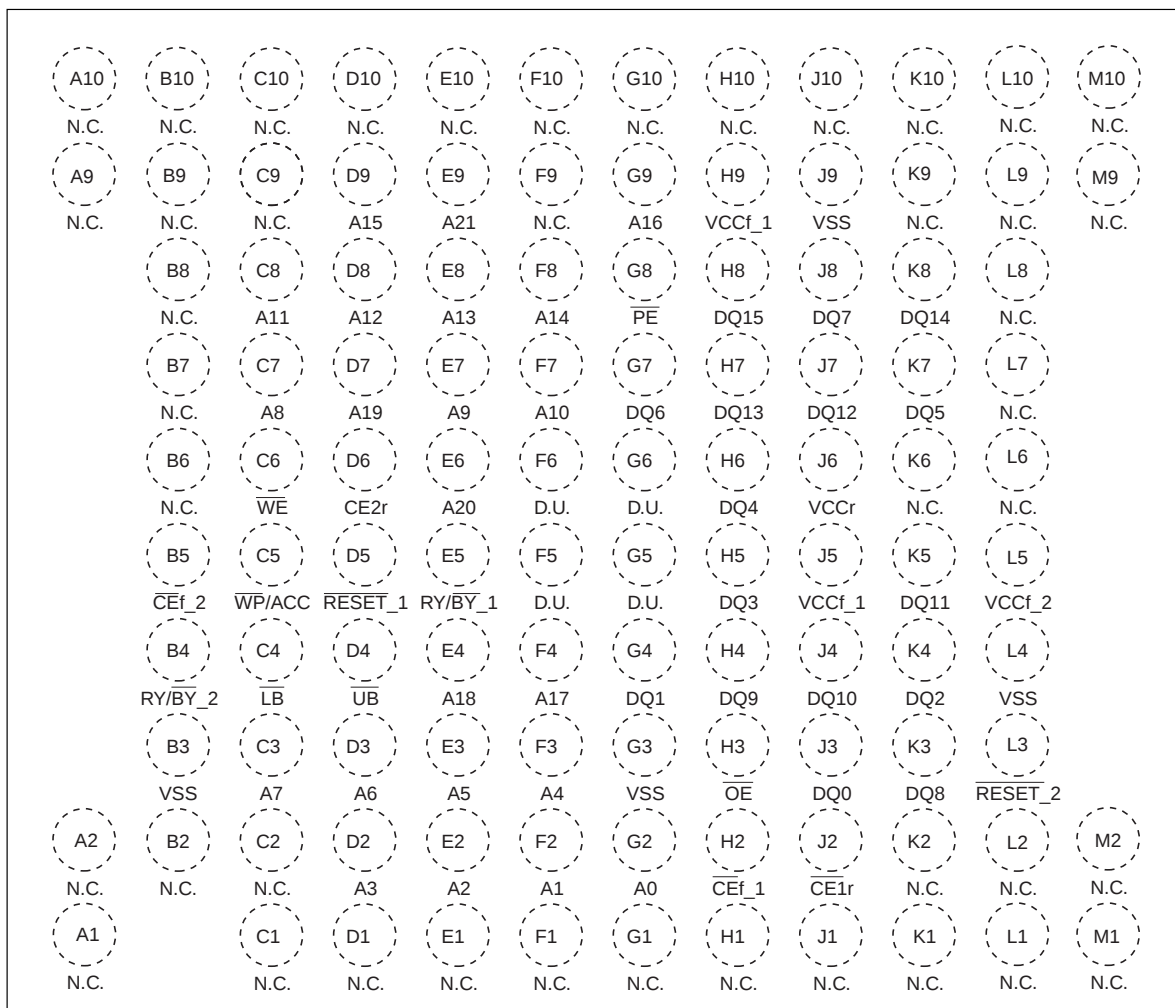
\*2: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

\*3: FCRAM™ is a trademark of Fujitsu Limited, Japan.

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## ■ PIN ASSIGNMENT

(Top View)  
Marking Side



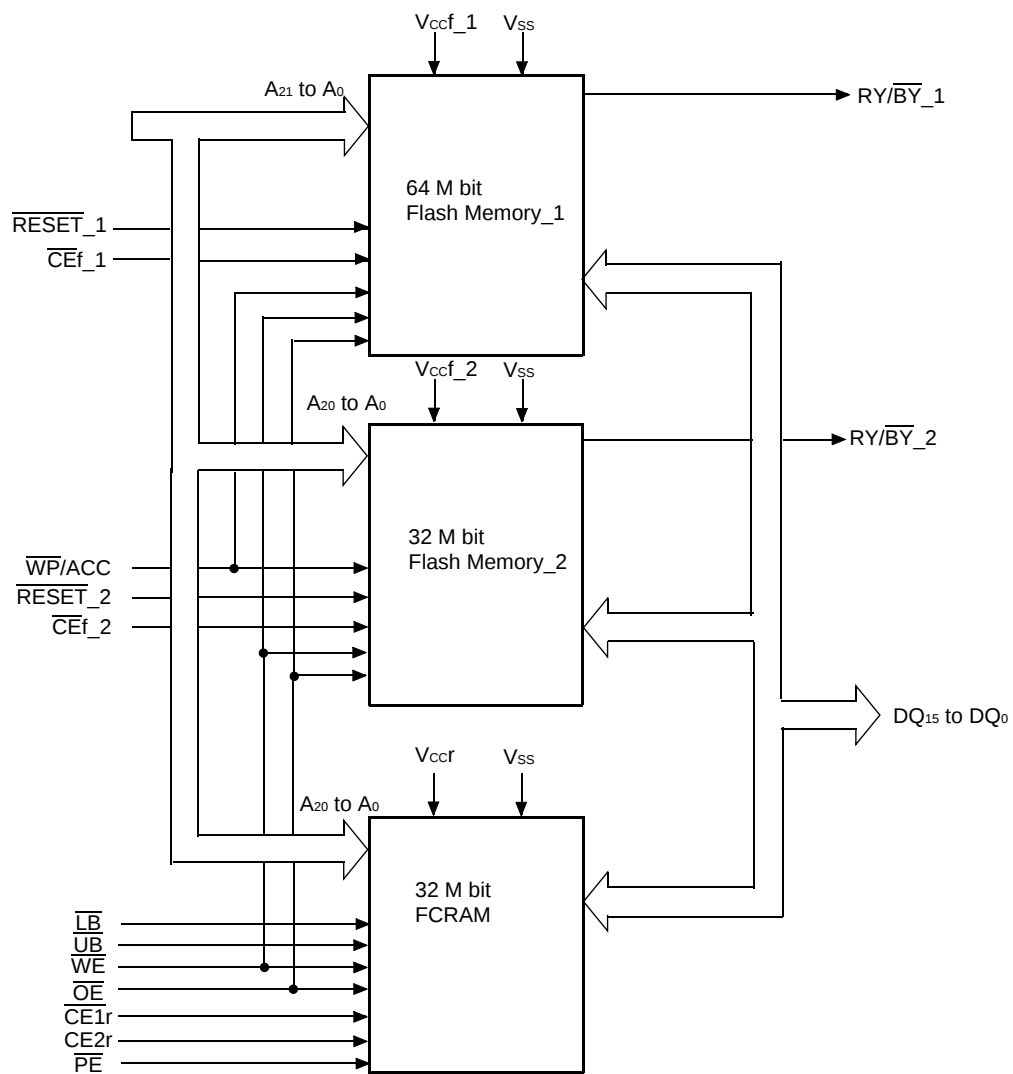
(BGA-107P-M01)

## ■ PIN DESCRIPTION

| Pin name                            | Input/<br>Output | Description                                           |
|-------------------------------------|------------------|-------------------------------------------------------|
| A <sub>20</sub> to A <sub>0</sub>   | I                | Address Inputs (Common)                               |
| A <sub>21</sub>                     | I                | Address Input (Flash_1)                               |
| DQ <sub>15</sub> to DQ <sub>0</sub> | I/O              | Data Inputs/Outputs (Common)                          |
| $\overline{\text{CEf}}_1$           | I                | Chip Enable (Flash_1)                                 |
| $\overline{\text{CEf}}_2$           | I                | Chip Enable (Flash_2)                                 |
| $\overline{\text{CE1r}}$            | I                | Chip Enable (FCRAM)                                   |
| CE2r                                | I                | Chip Enable (FCRAM)                                   |
| $\overline{\text{OE}}$              | I                | Output Enable (Common)                                |
| $\overline{\text{WE}}$              | I                | Write Enable (Common)                                 |
| RY/ $\overline{\text{BY}}$ _1       | O                | Ready/Busy Output (Flash_1) Open Drain Output         |
| RY/ $\overline{\text{BY}}$ _2       | O                | Ready/Busy Output (Flash_2) Open Drain Output         |
| $\overline{\text{UB}}$              | I                | Upper Byte Control (FCRAM)                            |
| $\overline{\text{LB}}$              | I                | Lower Byte Control (FCRAM)                            |
| $\overline{\text{RESET}}_1$         | I                | Hardware Reset Pin/Sector Protection Unlock (Flash_1) |
| $\overline{\text{RESET}}_2$         | I                | Hardware Reset Pin/Sector Protection Unlock (Flash_2) |
| $\overline{\text{WP/ACC}}$          | I                | Write Protect / Acceleration (Flash_1 & Flash_2)      |
| $\overline{\text{PE}}$              | I                | Partial Enable (FCRAM)                                |
| N.C.                                | —                | No Internal Connection                                |
| D.U.                                | —                | Don't Use                                             |
| V <sub>ss</sub>                     | Power            | Device Ground (Common)                                |
| V <sub>ccf_1</sub>                  | Power            | Device Power Supply (Flash_1)                         |
| V <sub>ccf_2</sub>                  | Power            | Device Power Supply (Flash_2)                         |
| V <sub>ccr</sub>                    | Power            | Device Power Supply (FCRAM)                           |

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## ■ BLOCK DIAGRAM



## ■ DEVICE BUS OPERATIONS

| Operation*1, *2                                 | $\overline{CEf\_1}$ | $\overline{CEf\_2}$ | $\overline{CE1r}$ | CE2r | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | $\overline{PE}$ | A <sub>20</sub> to A <sub>0</sub> | DQ <sub>7</sub> to DQ <sub>0</sub> | DQ <sub>15</sub> to DQ <sub>8</sub> | $\overline{RESET\_1}$ | $\overline{RESET\_2}$ | $\overline{WP/ACC}$<br>*12 |
|-------------------------------------------------|---------------------|---------------------|-------------------|------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------------------------|------------------------------------|-------------------------------------|-----------------------|-----------------------|----------------------------|
| Full Standby                                    | H                   | H                   | H                 | H    | X               | X               | X               | X               | H               | X                                 | High-Z                             | High-Z                              | H                     | H                     | X                          |
| Output Disable *3                               | H                   | H                   | L                 | H    | H               | H               | X               | X               | H               | X*10                              | High-Z                             | High-Z                              | H                     | H                     | X                          |
|                                                 | L                   | H                   | H                 |      | H               | H               | X               | X               |                 | X                                 |                                    |                                     |                       |                       |                            |
|                                                 | H                   | L                   | H                 |      | H               | H               | X               | X               |                 | X                                 |                                    |                                     |                       |                       |                            |
| Read from Flash_1 *4                            | L                   | H                   | H                 | H    | L               | H               | X               | X               | H               | Valid                             | D <sub>OUT</sub>                   | D <sub>OUT</sub>                    | H                     | H                     | X                          |
| Read from Flash_2 *4                            | H                   | L                   | H                 | H    | L               | H               | X               | X               | H               | Valid                             | D <sub>OUT</sub>                   | D <sub>OUT</sub>                    | H                     | H                     | X                          |
| Write to Flash_1                                | L                   | H                   | H                 | H    | H               | L               | X               | X               | H               | Valid                             | D <sub>IN</sub>                    | D <sub>IN</sub>                     | H                     | H                     | X                          |
| Write to Flash_2                                | H                   | L                   | H                 | H    | H               | L               | X               | X               | H               | Valid                             | D <sub>IN</sub>                    | D <sub>IN</sub>                     | H                     | H                     | X                          |
| Read from FCRAM *5                              | H                   | H                   | L                 | H    | L               | H               | L*9             | L*9             | H               | Valid                             | D <sub>OUT</sub>                   | D <sub>OUT</sub>                    | H                     | H                     | X                          |
| Write to FCRAM                                  | H                   | H                   | L                 | H    | H               | L               | L               | L               | H               | Valid                             | D <sub>IN</sub>                    | D <sub>IN</sub>                     | H                     | H                     | X                          |
|                                                 |                     |                     |                   |      |                 |                 | H               | L               |                 |                                   | High-Z                             | D <sub>IN</sub>                     |                       |                       |                            |
|                                                 |                     |                     |                   |      |                 |                 | L               | H               |                 |                                   | D <sub>IN</sub>                    | High-Z                              |                       |                       |                            |
| Flash_1 Temporary Sector Group Unprotection *6  | X                   | X                   | X                 | X    | X               | X               | X               | X               | X               | X                                 | X                                  | X                                   | V <sub>ID</sub>       | X                     | X                          |
| Flash_2 Temporary Sector Group Unprotection*6   | X                   | X                   | X                 | X    | X               | X               | X               | X               | X               | X                                 | X                                  | X                                   | X                     | V <sub>ID</sub>       | X                          |
| Flash_1 Hardware Reset                          | X                   | X                   | H                 | H    | X               | X               | X               | X               | X               | X                                 | High-Z                             | High-Z                              | L                     | X                     | X                          |
| Flash_2 Hardware Reset                          | X                   | X                   | H                 | H    | X               | X               | X               | X               | X               | X                                 | High-Z                             | High-Z                              | X                     | L                     | X                          |
| Flash_1 or 2 Boot Block Sector Write Protection | X                   | X                   | X                 | X    | X               | X               | X               | X               | X               | X                                 | X                                  | X                                   | X                     | X                     | L                          |
| FCRAM Power Down Program                        | H                   | H                   | H                 | H    | X               | X               | X               | X               | L               | Valid *11                         | High-Z                             | High-Z                              | H                     | H                     | X                          |
| FCRAM No Read *7                                | H                   | H                   | L                 | H    | L               | H               | H               | H               | H               | Valid                             | High-Z                             | High-Z                              | H                     | H                     | X                          |
| FCRAM Power Down *8                             | X                   | X                   | X                 | L    | X               | X               | X               | X               | X               | X                                 | X                                  | X                                   | X                     | X                     | X                          |

Legend: L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = V<sub>IL</sub> or V<sub>IH</sub>. See DC Characteristics for voltage levels.

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- \*1 : Other operations except for indicated this column are inhibited.
- \*2 : Do not apply for a following state two or more on the same time;  
1)  $\overline{CEf\_1} = V_{IL}$ , 2)  $\overline{CEf\_2} = V_{IL}$ , 3)  $\overline{CE1r} = V_{IL}$  and  $CE2r = V_{IH}$
- \*3 : FCRAM Output Disable condition should not be kept longer than 1 $\mu$ s.
- \*4 :  $\overline{WE}$  can be  $V_{IL}$  if  $\overline{OE}$  is  $V_{IL}$ ,  $\overline{OE}$  at  $V_{IH}$  initiates the write operations.
- \*6 : It is also used for the extended sector group protections.
- \*7 : The FCRAM Power Down Program can be performed one time after compliance of Power-UP timings and it should not be re-programmed after regular Read or Write.
- \*8 : FCRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.  $I_{PDR}$  current and data retention depends on the selection of Power Down Program.
- \*9 : Either or both  $\overline{LB}$  and  $\overline{UB}$  must be Low for FCRAM Read Operation.
- \*10 : Can be either  $V_{IL}$  or  $V_{IH}$  but must be valid before Read or Write.
- \*11 : See "1. FCRAM Power Down Program Key Table" in "■32M FCRAM CHARACTERISTICS for MCP".
- \*12 : Protect " outer most "  $2 \times 8K$  bytes ( 4 words ) on both ends of the boot block sectors.

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter                                                                                                                              | Symbol                                                     | Rating |                          | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|--------|--------------------------|------|
|                                                                                                                                        |                                                            | Min    | Max                      |      |
| Storage Temperature                                                                                                                    | T <sub>stg</sub>                                           | −55    | +125                     | °C   |
| Ambient Temperature with Power Applied                                                                                                 | T <sub>A</sub>                                             | −30    | +85                      | °C   |
| Voltage with Respect to Ground All pins except $\overline{\text{RESET}}_1$ or $\overline{\text{RESET}}_2, \overline{\text{WP/ACC}}$ *1 | V <sub>IN</sub> , V <sub>OUT</sub>                         | −0.3   | V <sub>ccf_1</sub> + 0.3 | V    |
|                                                                                                                                        |                                                            |        | V <sub>ccf_2</sub> + 0.3 | V    |
|                                                                                                                                        |                                                            |        | V <sub>ccr</sub> + 0.3   | V    |
| V <sub>ccf_1</sub> /V <sub>ccf_2</sub> /V <sub>ccr</sub> Supply *1                                                                     | V <sub>ccf_1</sub> , V <sub>ccf_2</sub> , V <sub>ccr</sub> | −0.3   | +3.3                     | V    |
| $\overline{\text{RESET}}_1$ or $\overline{\text{RESET}}_2$ *2                                                                          | V <sub>IN</sub>                                            | −0.5   | +13.0                    | V    |
| $\overline{\text{WP/ACC}}$ *3                                                                                                          | V <sub>IN</sub>                                            | −0.5   | +10.5                    | V    |

\*1 : Minimum DC voltage on input or I/O pins is −0.3 V. During voltage transitions, input or I/O pins may undershoot V<sub>SS</sub> to −1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V<sub>ccf\_1</sub> + 0.3 V or V<sub>ccf\_2</sub> + 0.3 V or V<sub>ccr</sub> + 0.3 V. During voltage transitions, input or I/O pins may overshoot to V<sub>ccf\_1</sub> + 2.0 V or V<sub>ccf\_2</sub> + 2.0 V or V<sub>ccr</sub> + 1.0 V for periods of up to 20 ns.

\*2 : Minimum DC input voltage on  $\overline{\text{RESET}}_1$  or  $\overline{\text{RESET}}_2$  pin is −0.5 V. During voltage transitions  $\overline{\text{RESET}}_1$  or  $\overline{\text{RESET}}_2$  pins may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V<sub>IN</sub>−V<sub>ccf\_1</sub> or V<sub>ccf\_2</sub>) does not exceed +9.0 V. Maximum DC input voltage on  $\overline{\text{RESET}}_1$  or  $\overline{\text{RESET}}_2$  pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

\*3 : Minimum DC input voltage on  $\overline{\text{WP/ACC}}$  pin is −0.5 V. During voltage transitions,  $\overline{\text{WP/ACC}}$  pin may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on  $\overline{\text{WP/ACC}}$  pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V<sub>ccf\_1</sub> or V<sub>ccf\_2</sub> is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter                                                                | Symbol                                                     | Value |      | Unit |
|--------------------------------------------------------------------------|------------------------------------------------------------|-------|------|------|
|                                                                          |                                                            | Min   | Max  |      |
| Ambient Temperature                                                      | T <sub>A</sub>                                             | −30   | +85  | °C   |
| V <sub>ccf_1</sub> /V <sub>ccf_2</sub> /V <sub>ccr</sub> Supply Voltages | V <sub>ccf_1</sub> , V <sub>ccf_2</sub> , V <sub>ccr</sub> | +2.7  | +3.1 | V    |

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

| Parameter                                                      | Symbol              | Conditions                                                                                                                                                                                                                  |                                          | Value |      |      | Unit |
|----------------------------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|-------|------|------|------|
|                                                                |                     |                                                                                                                                                                                                                             |                                          | Min   | Typ  | Max  |      |
| Input Leakage Current                                          | I <sub>LI</sub>     | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>ccf_1</sub> , V <sub>ccr</sub>                                                                                                                                                  |                                          | -1.0  | —    | +1.0 | mA   |
| Output Leakage Current                                         | I <sub>LO</sub>     | V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>ccf_1</sub> , V <sub>ccr</sub>                                                                                                                                                 |                                          | -1.0  | —    | +1.0 | mA   |
| RESET Inputs Leakage Current                                   | I <sub>LIT</sub>    | V <sub>ccf</sub> = V <sub>ccf</sub> Max,<br>RESET = 12.5 V                                                                                                                                                                  |                                          | —     | —    | 35   | μA   |
| Flash_1 V <sub>CC</sub> Active Current (Read) *1               | I <sub>cc1f_1</sub> | CEf_1 = V <sub>IL</sub> ,<br>OE = V <sub>IH</sub>                                                                                                                                                                           | t <sub>CYCLE</sub> = 5 MHz               | —     | —    | 18   | mA   |
|                                                                |                     |                                                                                                                                                                                                                             | t <sub>CYCLE</sub> = 1 MHz               | —     | —    | 4    | mA   |
| Flash_1 V <sub>CC</sub> Active Current (Program/Erase) *2      | I <sub>cc2f_1</sub> | CEf_1 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                              |                                          | —     | —    | 30   | mA   |
| Flash_1 V <sub>CC</sub> Active Current (Read-While-Program) *5 | I <sub>cc3f_1</sub> | CEf_1 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                              |                                          | —     | —    | 48   | mA   |
| Flash_1 V <sub>CC</sub> Active Current (Read-While-Erase) *5   | I <sub>cc4f_1</sub> | CEf_1 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                              |                                          | —     | —    | 48   | mA   |
| Flash_1 V <sub>CC</sub> Active Current (Erase-Suspend-Program) | I <sub>cc5f_1</sub> | CEf_1 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                              |                                          | —     | —    | 30   | mA   |
| Flash_2 V <sub>CC</sub> Active Current (Read) *1               | I <sub>cc1f_2</sub> | CEf_2 = V <sub>IL</sub> ,<br>OE = V <sub>IH</sub>                                                                                                                                                                           | t <sub>CYCLE</sub> = 5 MHz               | —     | —    | 18   | mA   |
|                                                                |                     |                                                                                                                                                                                                                             | t <sub>CYCLE</sub> = 1 MHz               | —     | —    | 4    |      |
| Flash_2 V <sub>CC</sub> Active Current (Program/Erase) *2      | I <sub>cc2f_2</sub> | CE_2 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                               |                                          | —     | —    | 30   | mA   |
| Flash_2 V <sub>CC</sub> Active Current (Read-While-Program) *5 | I <sub>cc3f_2</sub> | CE_2 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                               |                                          | —     | —    | 48   | mA   |
| Flash_2 V <sub>CC</sub> Active Current (Read-While-Erase) *5   | I <sub>cc4f_2</sub> | CE_2 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                               |                                          | —     | —    | 48   | mA   |
| Flash_2 V <sub>CC</sub> Active Current (Erase-Suspend-Program) | I <sub>cc5f_2</sub> | CE_2 = V <sub>IL</sub> , OE = V <sub>IH</sub>                                                                                                                                                                               |                                          | —     | —    | 35   | mA   |
| WP/ACC Acceleration Program Current                            | I <sub>ACC</sub>    | V <sub>ccf</sub> = V <sub>ccf</sub> Max,<br>WP/ACC = V <sub>ACC</sub> Max                                                                                                                                                   |                                          | —     | —    | 20   | mA   |
| FCRAM V <sub>CC</sub> Active Current                           | I <sub>cc1r</sub>   | V <sub>ccr</sub> = V <sub>ccr</sub> Max,<br>CE1r = V <sub>IL</sub> , CE2r = V <sub>IH</sub> ,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> ,<br>I <sub>OUT</sub> = 0mA                                           | t <sub>RC</sub> / t <sub>WC</sub> = Min  | —     | —    | 25   | mA   |
|                                                                |                     |                                                                                                                                                                                                                             | t <sub>RC</sub> / t <sub>WC</sub> = 1 ms | —     | —    | 3    |      |
| Flash V <sub>CC</sub> Standby Current                          | I <sub>SB1f</sub>   | V <sub>ccf</sub> = V <sub>ccf</sub> Max, CEf = V <sub>ccf</sub> ± 0.3 V,<br>RESET = V <sub>ccf</sub> ± 0.3 V,<br>WP/ACC = V <sub>ccf</sub> ± 0.3 V                                                                          |                                          | —     | 1 *7 | 5 *7 | μA   |
| Flash V <sub>CC</sub> Standby Current (RESET)                  | I <sub>SB2f</sub>   | V <sub>ccf</sub> = V <sub>ccf</sub> Max, RESET = V <sub>SS</sub> ± 0.3 V,<br>WP/ACC = V <sub>ccf</sub> ± 0.3 V                                                                                                              |                                          | —     | 1 *7 | 5 *7 | μA   |
| Flash V <sub>CC</sub> Current (Automatic Sleep Mode) *3        | I <sub>SB3f</sub>   | V <sub>ccf</sub> = V <sub>ccf</sub> Max, CEf = V <sub>SS</sub> ± 0.3 V,<br>RESET = V <sub>ccf</sub> ± 0.3 V,<br>WP/ACC = V <sub>ccf</sub> ± 0.3 V,<br>V <sub>IN</sub> = V <sub>ccf</sub> ± 0.3 V or V <sub>SS</sub> ± 0.3 V |                                          | —     | 1 *7 | 5 *7 | μA   |

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(Continued)

| Parameter                                                                                             | Symbol     | Conditions                                                                                                                                            |            | Value         |     |                   | Unit    |
|-------------------------------------------------------------------------------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------------|-----|-------------------|---------|
|                                                                                                       |            |                                                                                                                                                       |            | Min           | Typ | Max               |         |
| FCRAM $V_{CC}$ Standby Current                                                                        | $I_{SB1F}$ | $V_{CCF} = V_{CCF} \text{ Max}, \overline{CE1r} \geq V_{CCF} - 0.2V,$<br>$CE2r \geq V_{CCF} - 0.2V,$<br>$V_{IN} \leq 0.2V \text{ or } V_{CCF} - 0.2V$ |            | —             | —   | 100               | $\mu A$ |
| FCRAM $V_{CC}$ Power Down Current                                                                     | $I_{PDSF}$ | $V_{CCF} = V_{CCF} \text{ Max},$<br>$CE1r \geq V_{CCF} - 0.2V,$<br>$CE2r \leq 0.2V,$<br>$V_{IN} \text{ Cycle time} = t_{RC} \text{ Min}$              | Sleep      | —             | —   | 10                | $\mu A$ |
|                                                                                                       | $I_{PDNF}$ |                                                                                                                                                       | NAP        | —             | —   | 60                | $\mu A$ |
|                                                                                                       | $I_{PD8F}$ |                                                                                                                                                       | 8M Partial | —             | —   | 70                | $\mu A$ |
| Input Low Level                                                                                       | $V_{IL}$   | —                                                                                                                                                     |            | -0.3          | —   | 0.5               | V       |
| Input High Level                                                                                      | $V_{IH}$   | —                                                                                                                                                     |            | 2.2           | —   | $V_{CC+0.3}^{*6}$ | V       |
| Voltage for Sector Protection, and Temporary Sector Unprotection ( $\overline{RESET}$ ) <sup>*4</sup> | $V_{ID}$   | —                                                                                                                                                     |            | 11.5          | —   | 12.5              | V       |
| Voltage for $\overline{WP}/ACC$ Sector Protection/Unprotection and Program Acceleration <sup>*4</sup> | $V_{ACC}$  | —                                                                                                                                                     |            | 8.5           | 9.0 | 9.5               | V       |
| Output Low Voltage Level                                                                              | $V_{OLf}$  | $V_{CCF} = V_{CCF} \text{ Min}, I_{OL} = 4.0 \text{ mA}$                                                                                              | Flash      | —             | —   | 0.45              | V       |
|                                                                                                       | $V_{OLr}$  | $V_{CCF} = V_{CCF} \text{ Min}, I_{OL} = 1.0 \text{ mA}$                                                                                              | FCRAM      | —             | —   | 0.4               | V       |
| Output High Voltage Level                                                                             | $V_{OHf}$  | $V_{CCF} = V_{CCF} \text{ Min}, I_{OH} = -0.1 \text{ mA}$                                                                                             | Flash      | $V_{CCF}-0.4$ | —   | —                 | V       |
|                                                                                                       | $V_{OHR}$  | $V_{CCF} = V_{CCF} \text{ Min}, I_{OH} = -0.5 \text{ mA}$                                                                                             | FCRAM      | 2.2           | —   | —                 | V       |
| Flash Low $V_{CCF}$ Lock-Out Voltage                                                                  | $V_{LKO}$  | —                                                                                                                                                     |            | 2.3           | 2.4 | 2.5               | V       |

Legend: Flash means Flash\_1 or Flash\_2,  $V_{CCF}$  means  $V_{CCF\_1}$  or  $V_{CCF\_2}$ ,  $V_{SSf}$  means  $V_{SSf\_1}$  or  $V_{SSf\_2}$ ,  $\overline{CEf}$  means  $\overline{CEf\_1}$  or  $\overline{CEf\_2}$ ,  $\overline{RESET}$  means  $\overline{RESET\_1}$  or  $\overline{RESET\_2}$

\*1: The  $I_{CC}$  current listed includes both the DC operating current and the frequency dependent component.

\*2:  $I_{CC}$  active while Embedded Algorithm (program or erase) is in progress.

\*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

\*4: Applicable for only  $V_{CCF}$  applying.

\*5: Embedded Algorithm (program or erase) is in progress. (@5 MHz)

\*6:  $V_{CC}$  indicates lower of  $V_{CCF\_1}$  or  $V_{CCF\_2}$  or  $V_{CCr}$ .

\*7: Actual Standby Current is twice of what is indicated in the table, due to two Flash memory chips embedment within one device.

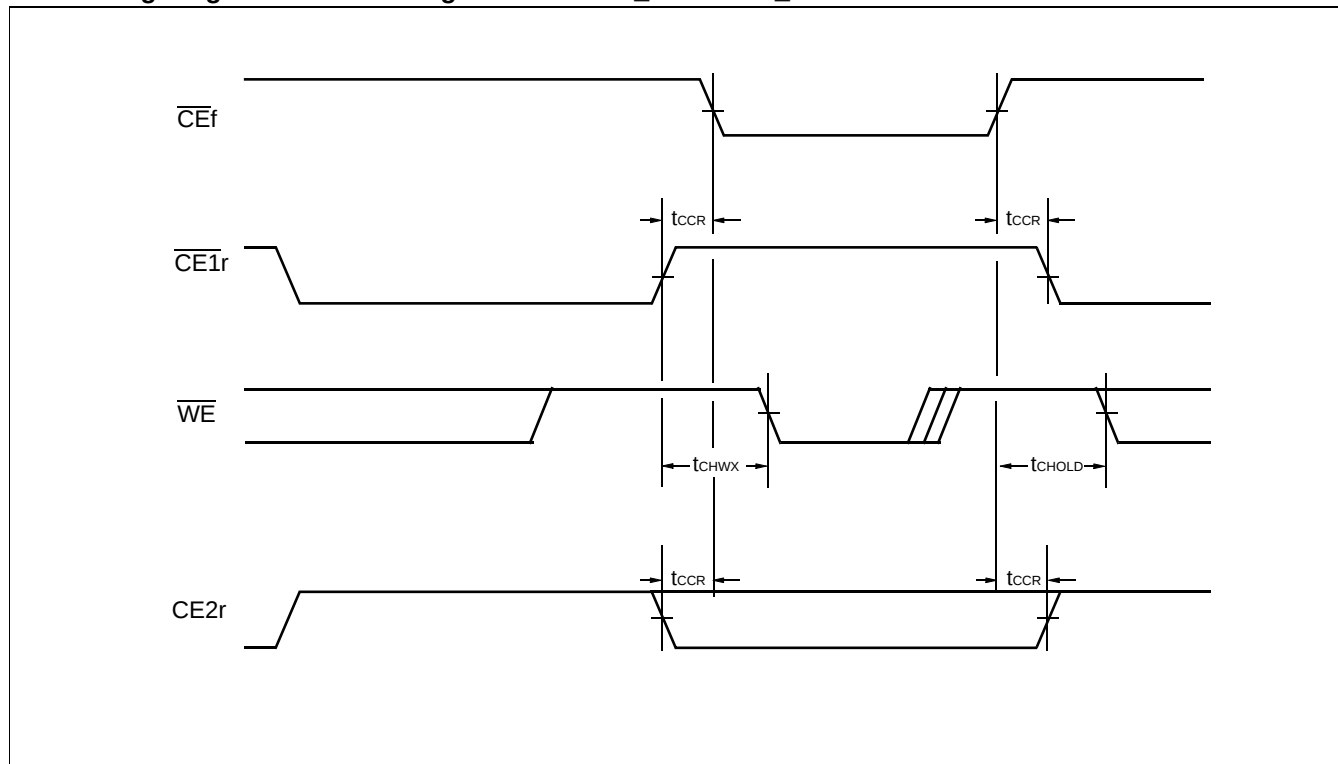
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## 2. AC Characteristics

### • $\overline{\text{CE}}$ Timing

| Parameter                                                                                | Symbol |                    | Condition | Value |     | Unit |
|------------------------------------------------------------------------------------------|--------|--------------------|-----------|-------|-----|------|
|                                                                                          | JEDEC  | Standard           |           | Min   | Max |      |
| $\overline{\text{CE}}$ Recover Time                                                      | —      | $t_{\text{CCR}}$   | —         | 0     | —   | ns   |
| $\overline{\text{CE}}$ Hold Time                                                         | —      | $t_{\text{CHOLD}}$ | —         | 3     | —   | ns   |
| $\overline{\text{CE1r}}$ , High to $\overline{\text{WE}}$ Invalid time for Standby Entry | —      | $t_{\text{CHWX}}$  | —         | 10    | —   | ns   |

### • Timing Diagram for alternating RAM to Flash\_1 or Flash\_2



### • Flash\_1 Characteristics

Please refer to “■64M FLASH MEMORY CHARACTERISTICS for MCP” part. In this part, Flash means Flash\_1,  $V_{\text{ccf}}$  means  $V_{\text{ccf\_1}}$ ,  $V_{\text{ssf}}$  means  $V_{\text{ssf\_1}}$ ,  $\overline{\text{CEf}}$  means  $\overline{\text{CEf\_1}}$ ,  $\overline{\text{RESET}}$  means  $\overline{\text{RESET\_1}}$

### • Flash\_2 Characteristics

Please refer to “■32M FLASH MEMORY CHARACTERISTICS for MCP” part. In this part, Flash means Flash\_2,  $V_{\text{ccf}}$  means  $V_{\text{ccf\_2}}$ ,  $V_{\text{ssf}}$  means  $V_{\text{ssf\_2}}$ ,  $\overline{\text{CEf}}$  means  $\overline{\text{CEf\_2}}$ ,  $\overline{\text{RESET}}$  means  $\overline{\text{RESET\_2}}$

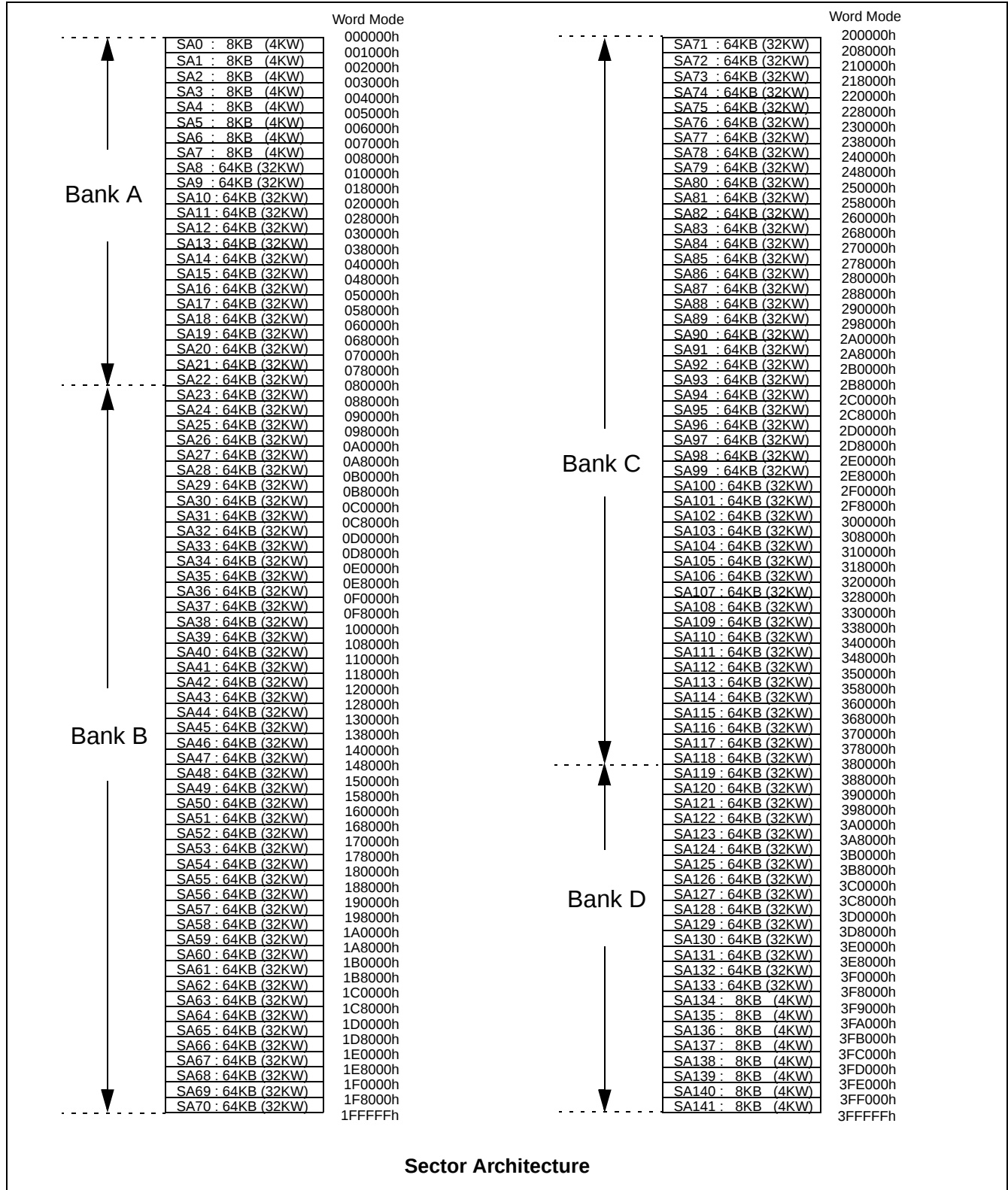
### • FCRAM Characteristics

Please refer to “■32M FCRAM CHARACTERISTICS for MCP” part.

## ■ 64M FLASH MEMORY CHARACTERISTICS for MCP

### 1. Flexible Sector-erase Architecture on Flash Memory

- Sixteen 4K words, and one hundred twenty-six 32K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



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**FlexBank™ Architecture Table**

| Bank Splits | Bank 1  |             | Bank 2  |                          |
|-------------|---------|-------------|---------|--------------------------|
|             | Volume  | Combination | Volume  | Combination              |
| 1           | 8 Mbit  | Bank A      | 56 Mbit | Remainder (Bank B, C, D) |
| 2           | 24 Mbit | Bank B      | 40 Mbit | Remainder (Bank A, C, D) |
| 3           | 24 Mbit | Bank C      | 40 Mbit | Remainder (Bank A, B, D) |
| 4           | 8 Mbit  | Bank D      | 56 Mbit | Remainder (Bank A, B, C) |

**Example of Virtual Banks Combination Table**

| Bank Splits | Bank 1  |                       |                                                     | Bank 2  |                                      |                                                     |
|-------------|---------|-----------------------|-----------------------------------------------------|---------|--------------------------------------|-----------------------------------------------------|
|             | Volume  | Combination           | Sector Size                                         | Volume  | Combination                          | Sector Size                                         |
| 1           | 8 Mbit  | Bank A                | 8 × 8 Kbyte/4 Kword<br>+<br>15 × 64 Kbyte/32 Kword  | 56 Mbit | Bank B<br>+<br>Bank C<br>+<br>Bank D | 8 × 8 Kbyte/4 Kword<br>+<br>111 × 64 Kbyte/32 Kword |
| 2           | 16 Mbit | Bank A<br>+<br>Bank D | 16 × 8 Kbyte/4 Kword<br>+<br>30 × 64 Kbyte/32 Kword | 48 Mbit | Bank B<br>+<br>Bank C                | 96 × 64 Kbyte/32 Kword                              |
| 3           | 24 Mbit | Bank B                | 48 × 64 Kbyte/32 Kword                              | 40 Mbit | Bank A<br>+<br>Bank C<br>+<br>Bank D | 16 × 8 Kbyte/4 Kword<br>+<br>78 × 64 Kbyte/32 Kword |
| 4           | 32 Mbit | Bank A<br>+<br>Bank B | 8 × 8 Kbyte/4 Kword<br>+<br>63 × 64 Kbyte/32 Kword  | 32 Mbit | Bank C<br>+<br>Bank D                | 8 × 8 Kbyte/4 Kword<br>+<br>63 × 64 Kbyte/32 Kword  |

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

**Simultaneous Operation Table**

| Case | Bank 1 Status   | Bank 2 Status   |
|------|-----------------|-----------------|
| 1    | Read mode       | Read mode       |
| 2    | Read mode       | Autoselect mode |
| 3    | Read mode       | Program mode    |
| 4    | Read mode       | Erase mode *    |
| 5    | Autoselect mode | Read mode       |
| 6    | Program mode    | Read mode       |
| 7    | Erase mode *    | Read mode       |

\* : By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

Sector Address Table

| Bank   | Sector | Sector Address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Address Range      |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|
|        |        | Bank Address    |                 |                 |                 |                 |                 |                 |                 |                 |                 | Word Mode          |
|        |        | A <sub>21</sub> | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> |                    |
| Bank A | SA0    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 000000h to 000FFFh |
|        | SA1    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 001000h to 001FFFh |
|        | SA2    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 002000h to 002FFFh |
|        | SA3    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 003000h to 003FFFh |
|        | SA4    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               | 004000h to 004FFFh |
|        | SA5    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | 005000h to 005FFFh |
|        | SA6    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 0               | 006000h to 006FFFh |
|        | SA7    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 1               | 007000h to 007FFFh |
|        | SA8    | 0               | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | 008000h to 00FFFFh |
|        | SA9    | 0               | 0               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | 010000h to 017FFFh |
|        | SA10   | 0               | 0               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | 018000h to 01FFFFh |
|        | SA11   | 0               | 0               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | 020000h to 027FFFh |
|        | SA12   | 0               | 0               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | 028000h to 02FFFFh |
|        | SA13   | 0               | 0               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | 030000h to 037FFFh |
|        | SA14   | 0               | 0               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | 038000h to 03FFFFh |
|        | SA15   | 0               | 0               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | 040000h to 047FFFh |
|        | SA16   | 0               | 0               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | 048000h to 04FFFFh |
|        | SA17   | 0               | 0               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | 050000h to 057FFFh |
|        | SA18   | 0               | 0               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | 058000h to 05FFFFh |
|        | SA19   | 0               | 0               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | 060000h to 067FFFh |
|        | SA20   | 0               | 0               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | 068000h to 06FFFFh |
|        | SA21   | 0               | 0               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | 070000h to 077FFFh |
|        | SA22   | 0               | 0               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | 078000h to 07FFFFh |

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| Bank   | Sector | Sector Address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Address Range      |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|
|        |        | Bank Address    |                 |                 |                 |                 |                 |                 |                 |                 |                 | Word Mode          |
|        |        | A <sub>21</sub> | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> |                    |
| Bank B | SA23   | 0               | 0               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | 080000h to 087FFFh |
|        | SA24   | 0               | 0               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | 088000h to 08FFFFh |
|        | SA25   | 0               | 0               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | 090000h to 097FFFh |
|        | SA26   | 0               | 0               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | 098000h to 09FFFFh |
|        | SA27   | 0               | 0               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | 0A0000h to 0A7FFFh |
|        | SA28   | 0               | 0               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | 0A8000h to 0AFFFFh |
|        | SA29   | 0               | 0               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | 0B0000h to 0B7FFFh |
|        | SA30   | 0               | 0               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | 0B8000h to 0BFFFFh |
|        | SA31   | 0               | 0               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | 0C0000h to 0C7FFFh |
|        | SA32   | 0               | 0               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | 0C8000h to 0CFFFFh |
|        | SA33   | 0               | 0               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | 0D0000h to 0D7FFFh |
|        | SA34   | 0               | 0               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | 0D8000h to 0DFFFFh |
|        | SA35   | 0               | 0               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | 0E0000h to 0E7FFFh |
|        | SA36   | 0               | 0               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | 0E8000h to 0EFFFFh |
|        | SA37   | 0               | 0               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | 0F0000h to 0F7FFFh |
|        | SA38   | 0               | 0               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | 0F8000h to 0FFFFFh |
|        | SA39   | 0               | 1               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | 100000h to 107FFFh |
|        | SA40   | 0               | 1               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | 108000h to 10FFFFh |
|        | SA41   | 0               | 1               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | 110000h to 117FFFh |
|        | SA42   | 0               | 1               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | 118000h to 11FFFFh |
|        | SA43   | 0               | 1               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | 120000h to 127FFFh |
|        | SA44   | 0               | 1               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | 128000h to 12FFFFh |
|        | SA45   | 0               | 1               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | 130000h to 137FFFh |
|        | SA46   | 0               | 1               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | 138000h to 13FFFFh |
|        | SA47   | 0               | 1               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | 140000h to 147FFFh |
|        | SA48   | 0               | 1               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | 148000h to 14FFFFh |
|        | SA49   | 0               | 1               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | 150000h to 157FFFh |
|        | SA50   | 0               | 1               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | 158000h to 15FFFFh |
|        | SA51   | 0               | 1               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | 160000h to 167FFFh |
|        | SA52   | 0               | 1               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | 168000h to 16FFFFh |
|        | SA53   | 0               | 1               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | 170000h to 177FFFh |
|        | SA54   | 0               | 1               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | 178000h to 17FFFFh |
|        | SA55   | 0               | 1               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | 180000h to 187FFFh |
|        | SA56   | 0               | 1               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | 188000h to 18FFFFh |
|        | SA57   | 0               | 1               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | 190000h to 197FFFh |
|        | SA58   | 0               | 1               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | 198000h to 19FFFFh |
|        | SA59   | 0               | 1               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | 1A0000h to 1A7FFFh |
|        | SA60   | 0               | 1               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | 1A8000h to 1AFFFFh |
|        | SA61   | 0               | 1               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | 1B0000h to 1B7FFFh |
|        | SA62   | 0               | 1               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | 1B8000h to 1BFFFFh |
|        | SA63   | 0               | 1               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | 1C0000h to 1C7FFFh |
|        | SA64   | 0               | 1               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | 1C8000h to 1CFFFFh |
|        | SA65   | 0               | 1               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | 1D0000h to 1D7FFFh |
|        | SA66   | 0               | 1               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | 1D8000h to 1DFFFFh |
|        | SA67   | 0               | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | 1E0000h to 1E7FFFh |
|        | SA68   | 0               | 1               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | 1E8000h to 1EFFFFh |
|        | SA69   | 0               | 1               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | 1F0000h to 1F7FFFh |
|        | SA70   | 0               | 1               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | 1F8000h to 1FFFFFh |

(Continued)

| Bank   | Sector | Sector Address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Address Range      |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|
|        |        | Bank Address    |                 |                 |                 |                 |                 |                 |                 |                 |                 | Word Mode          |
|        |        | A <sub>21</sub> | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> |                    |
| Bank C | SA71   | 1               | 0               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | 200000h to 207FFFh |
|        | SA72   | 1               | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | 208000h to 20FFFFh |
|        | SA73   | 1               | 0               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | 210000h to 217FFFh |
|        | SA74   | 1               | 0               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | 218000h to 21FFFFh |
|        | SA75   | 1               | 0               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | 220000h to 227FFFh |
|        | SA76   | 1               | 0               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | 228000h to 22FFFFh |
|        | SA77   | 1               | 0               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | 230000h to 237FFFh |
|        | SA78   | 1               | 0               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | 238000h to 23FFFFh |
|        | SA79   | 1               | 0               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | 240000h to 247FFFh |
|        | SA80   | 1               | 0               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | 248000h to 24FFFFh |
|        | SA81   | 1               | 0               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | 250000h to 257FFFh |
|        | SA82   | 1               | 0               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | 258000h to 25FFFFh |
|        | SA83   | 1               | 0               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | 260000h to 267FFFh |
|        | SA84   | 1               | 0               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | 268000h to 26FFFFh |
|        | SA85   | 1               | 0               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | 270000h to 277FFFh |
|        | SA86   | 1               | 0               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | 278000h to 27FFFFh |
|        | SA87   | 1               | 0               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | 280000h to 287FFFh |
|        | SA88   | 1               | 0               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | 288000h to 28FFFFh |
|        | SA89   | 1               | 0               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | 290000h to 297FFFh |
|        | SA90   | 1               | 0               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | 298000h to 29FFFFh |
|        | SA91   | 1               | 0               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | 2A0000h to 2A7FFFh |
|        | SA92   | 1               | 0               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | 2A8000h to 2AFFFFh |
|        | SA93   | 1               | 0               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | 2B0000h to 2B7FFFh |
|        | SA94   | 1               | 0               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | 2B8000h to 2BFFFFh |
|        | SA95   | 1               | 0               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | 2C0000h to 2C7FFFh |
|        | SA96   | 1               | 0               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | 2C8000h to 2CFFFFh |
|        | SA97   | 1               | 0               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | 2D0000h to 2D7FFFh |
|        | SA98   | 1               | 0               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | 2D8000h to 2DFFFFh |
|        | SA99   | 1               | 0               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | 2E0000h to 2E7FFFh |
|        | SA100  | 1               | 0               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | 2E8000h to 2EFFFFh |
|        | SA101  | 1               | 0               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | 2F0000h to 2F7FFFh |
|        | SA102  | 1               | 0               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | 2F8000h to 2FFFFh  |
|        | SA103  | 1               | 1               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | 300000h to 307FFFh |
|        | SA104  | 1               | 1               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | 308000h to 30FFFFh |
|        | SA105  | 1               | 1               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | 310000h to 317FFFh |
|        | SA106  | 1               | 1               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | 318000h to 31FFFFh |
|        | SA107  | 1               | 1               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | 320000h to 327FFFh |
|        | SA108  | 1               | 1               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | 328000h to 32FFFFh |
|        | SA109  | 1               | 1               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | 330000h to 337FFFh |
|        | SA110  | 1               | 1               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | 338000h to 33FFFFh |
|        | SA111  | 1               | 1               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | 340000h to 347FFFh |
|        | SA112  | 1               | 1               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | 348000h to 34FFFFh |
|        | SA113  | 1               | 1               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | 350000h to 357FFFh |
|        | SA114  | 1               | 1               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | 358000h to 35FFFFh |
|        | SA115  | 1               | 1               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | 360000h to 367FFFh |
|        | SA116  | 1               | 1               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | 368000h to 36FFFFh |
|        | SA117  | 1               | 1               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | 370000h to 377FFFh |
|        | SA118  | 1               | 1               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | 378000h to 37FFFFh |

(Continued)

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(Continued)

| Bank   | Sector | Sector Address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Address Range       |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------------------|
|        |        | Bank Address    |                 |                 |                 |                 |                 |                 |                 |                 |                 | Word Mode           |
|        |        | A <sub>21</sub> | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> |                     |
| Bank D | SA119  | 1               | 1               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | 380000h to 387FFFh  |
|        | SA120  | 1               | 1               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | 388000h to 38FFFFh  |
|        | SA121  | 1               | 1               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | 390000h to 397FFFh  |
|        | SA122  | 1               | 1               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | 398000h to 39FFFFh  |
|        | SA123  | 1               | 1               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | 3A0000h to 3A7FFFh  |
|        | SA124  | 1               | 1               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | 3A8000h to 3AFFFFh  |
|        | SA125  | 1               | 1               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | 3B0000h to 3B7FFFh  |
|        | SA126  | 1               | 1               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | 3B8000h to 3BFFFFh  |
|        | SA127  | 1               | 1               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | 3C0000h to 3C7FFFh  |
|        | SA128  | 1               | 1               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | 3C8000h to 3CFFFFh  |
|        | SA129  | 1               | 1               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | 3D0000h to 3D7FFFh  |
|        | SA130  | 1               | 1               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | 3D8000h to 3DFFFFh  |
|        | SA131  | 1               | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | 3E0000h to 3E7FFFh  |
|        | SA132  | 1               | 1               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | 3E8000h to 3EFFFFh  |
|        | SA133  | 1               | 1               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | 3F0000h to 3F7FFFh  |
|        | SA134  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 0               | 3F8000h to 3F8FFFh  |
|        | SA135  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 1               | 3F9000h to 3F9FFFh  |
|        | SA136  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 0               | 3FA000h to 3FAFFFh  |
|        | SA137  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 1               | 3FB000h to 3FBFFFh  |
|        | SA138  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 3FC000h to 3FCFFFh  |
|        | SA139  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 3FD000h to 3FDFFFh  |
|        | SA140  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 3FE000h to 3FEFFFh  |
|        | SA141  | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 3FF000h to 3FFFFFFh |

Sector Group Addresses Table

| Sector Group | A <sub>21</sub> | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | Sectors        |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|
| SGA0         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | SA0            |
| SGA1         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | SA1            |
| SGA2         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | SA2            |
| SGA3         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | SA3            |
| SGA4         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               | SA4            |
| SGA5         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | SA5            |
| SGA6         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 0               | SA6            |
| SGA7         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 1               | SA7            |
| SGA8         | 0               | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | SA8 to SA10    |
|              |                 |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |                |
|              |                 |                 |                 |                 |                 | 1               | 1               |                 |                 |                 |                |
| SGA9         | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA11 to SA14   |
| SGA10        | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA15 to SA18   |
| SGA11        | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA19 to SA22   |
| SGA12        | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA23 to SA26   |
| SGA13        | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA27 to SA30   |
| SGA14        | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA31 to SA34   |
| SGA15        | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | X               | SA35 to SA38   |
| SGA16        | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | X               | SA39 to SA42   |
| SGA17        | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA43 to SA46   |
| SGA18        | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA47 to SA50   |
| SGA19        | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA51 to SA54   |
| SGA20        | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA55 to SA58   |
| SGA21        | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA59 to SA62   |
| SGA22        | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA63 to SA66   |
| SGA23        | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | X               | SA67 to SA70   |
| SGA24        | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | X               | SA71 to SA74   |
| SGA25        | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA75 to SA78   |
| SGA26        | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA79 to SA82   |
| SGA27        | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA83 to SA86   |
| SGA28        | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA87 to SA90   |
| SGA29        | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA91 to SA94   |
| SGA30        | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA95 to SA98   |
| SGA31        | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | X               | SA99 to SA102  |
| SGA32        | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | X               | SA103 to SA106 |
| SGA33        | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA107 to SA110 |
| SGA34        | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA111 to SA114 |
| SGA35        | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA115 to SA118 |
| SGA36        | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA119 to SA122 |
| SGA37        | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA123 to SA126 |
| SGA38        | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA127 to SA130 |
| SGA39        | 1               | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | SA131 to SA133 |
|              |                 |                 |                 |                 |                 | 0               | 1               |                 |                 |                 |                |
|              |                 |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |                |
| SGA40        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 0               | SA134          |
| SGA41        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 1               | SA135          |
| SGA42        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 0               | SA136          |
| SGA43        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 1               | SA137          |
| SGA44        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | SA138          |
| SGA45        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | SA139          |
| SGA46        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | SA140          |
| SGA47        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | SA141          |

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**Flash Memory Autoselect Codes Table**

| Type                    | A <sub>21</sub> to A <sub>12</sub> | A <sub>6</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | Code (HEX) |
|-------------------------|------------------------------------|----------------|----------------|----------------|----------------|----------------|------------|
| Manufacture's Code      | BA                                 | L              | L              | L              | L              | L              | 04h        |
| Device Code             | BA                                 | L              | L              | L              | L              | H              | 227Eh      |
| Extended Device Code *2 | BA                                 | L              | H              | H              | H              | L              | 2202h      |
|                         | BA                                 | L              | H              | H              | H              | H              | 2201h      |
| Sector Group Protection | Sector Group Addresses             | L              | L              | L              | H              | L              | 01h*1      |

Legend: L = V<sub>IL</sub>, H = V<sub>IH</sub>. See DC Characteristics for voltage levels.

\*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

\*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

Flash Memory Command Definitions Table

| Command Sequence                               | Bus Write Cycles Req'd | First Bus Write Cycle      |      | Second Bus Write Cycle |                       | Third Bus Write Cycle          |      | Fourth Bus Read/Write Cycle               |                   | Fifth Bus Write Cycle |      | Sixth Bus Write Cycle |      |
|------------------------------------------------|------------------------|----------------------------|------|------------------------|-----------------------|--------------------------------|------|-------------------------------------------|-------------------|-----------------------|------|-----------------------|------|
|                                                |                        | Addr.                      | Data | Addr.                  | Data                  | Addr.                          | Data | Addr.                                     | Data              | Addr.                 | Data | Addr.                 | Data |
| Read/Reset                                     | 1                      | XXXh                       | F0h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Read/Reset                                     | 3                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | F0h  | RA* <sup>5</sup>                          | RD* <sup>9</sup>  | —                     | —    | —                     | —    |
| Autoselect                                     | 3                      | 555h                       | AAh  | 2AAh                   | 55h                   | (BA* <sup>8</sup> )<br>555h    | 90h  | —                                         | —                 | —                     | —    | —                     | —    |
| Program                                        | 4                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | A0h  | PA* <sup>6</sup>                          | PD* <sup>10</sup> | —                     | —    | —                     | —    |
| Program Suspend                                | 1                      | BA* <sup>8</sup>           | B0h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Program Resume                                 | 1                      | BA* <sup>8</sup>           | 30h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Chip Erase                                     | 6                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | 80h  | 555h                                      | AAh               | 2AAh                  | 55h  | 555h                  | 10h  |
| Sector Erase                                   | 6                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | 80h  | 555h                                      | AAh               | 2AAh                  | 55h  | SA* <sup>7</sup>      | 30h  |
| Erase Suspend                                  | 1                      | BA* <sup>8</sup>           | B0h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Erase Resume                                   | 1                      | BA* <sup>8</sup>           | 30h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Extended Sector Group Protection* <sup>2</sup> | 4                      | XXXh                       | 60h  | SPA* <sup>11</sup>     | 60h                   | SPA* <sup>11</sup>             | 40h  | SPA* <sup>11</sup>                        | SD* <sup>12</sup> | —                     | —    | —                     | —    |
| Set to Fast Mode                               | 3                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | 20h  | —                                         | —                 | —                     | —    | —                     | —    |
| Fast Program* <sup>1</sup>                     | 2                      | XXXh                       | A0h  | PA* <sup>6</sup>       | PD* <sup>10</sup>     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Reset from Fast Mode* <sup>1</sup>             | 2                      | BA* <sup>8</sup>           | 90h  | XXXh                   | * <sup>4</sup><br>F0h | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Query                                          | 1                      | (BA* <sup>8</sup> )<br>55h | 98h  | —                      | —                     | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| HiddenROM Entry                                | 3                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | 88h  | —                                         | —                 | —                     | —    | —                     | —    |
| HiddenROM Program* <sup>3</sup>                | 4                      | 555h                       | AAh  | 2AAh                   | 55h                   | 555h                           | A0h  | (HRA* <sup>13</sup> )<br>PA* <sup>6</sup> | PD* <sup>10</sup> | —                     | —    | —                     | —    |
| HiddenROM Exit* <sup>3</sup>                   | 4                      | 555h                       | AAh  | 2AAh                   | 55h                   | (HRBA* <sup>14</sup> )<br>555h | 90h  | XXXh                                      | 00h               | —                     | —    | —                     | —    |

(Continued)

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(Continued)

- \*1 : This command is valid during Fast Mode.
- \*2 : This command is valid while  $\overline{\text{RESET}} = V_{\text{ID}}$ .
- \*3 : This command is valid during HiddenROM mode.
- \*4 : The data "00h" is also acceptable.
- \*5 : RA = Address of the memory location to be read
- \*6 : PA = Address of the memory location to be programmed Addresses are latched on the falling edge of the write pulse.
- \*7 : SA = Address of the sector to be erased. The combination of A<sub>21</sub>, A<sub>20</sub>, A<sub>19</sub>, A<sub>18</sub>, A<sub>17</sub>, A<sub>16</sub>, A<sub>15</sub>, A<sub>14</sub>, A<sub>13</sub>, and A<sub>12</sub> will uniquely select any sector.
- \*8 : BA = Bank Address (A<sub>21</sub>, A<sub>20</sub>, A<sub>19</sub>)
- \*9 : RD = Data read from location RA during read operation.
- \*10 : PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- \*11 : SPA = Sector group address to be protected. Set sector group address and (A<sub>6</sub>, A<sub>3</sub>, A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 0, 0, 1, 0).
- \*12 : SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- \*13 : HRA = Address of the HiddenROM area: 000000h to 00007Fh
- \*14 : HRBA = Bank Address of the HiddenROM area (A<sub>21</sub> = A<sub>20</sub> = A<sub>19</sub> = V<sub>IL</sub>)

Notes : • Address bits A<sub>21</sub> to A<sub>11</sub> = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).

- Bus operations are defined in ■DEVICE BUS OPERATION.
- The system should generate the following address patterns: 555h or 2AAh to addresses A<sub>10</sub> to A<sub>0</sub>
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- The command combinations not described in this table are illegal.

## 2. AC Characteristics

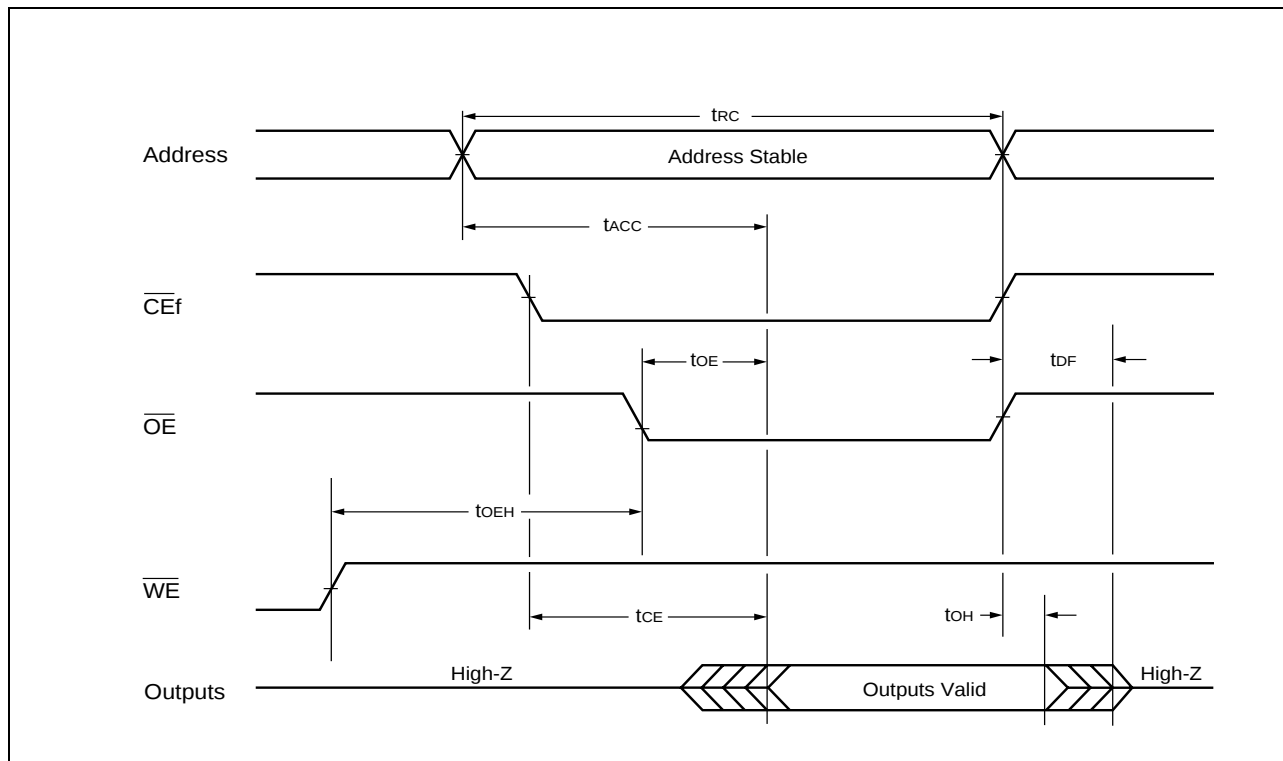
### • Read Only Operations Characteristics (Flash)

| Parameter                                                                                        | Symbol     |             | Condition                                              | Value (Note) |     | Unit    |
|--------------------------------------------------------------------------------------------------|------------|-------------|--------------------------------------------------------|--------------|-----|---------|
|                                                                                                  | JEDEC      | Standard    |                                                        | Min          | Max |         |
| Read Cycle Time                                                                                  | $t_{AVAV}$ | $t_{RC}$    | —                                                      | 70           | —   | ns      |
| Address to Output Delay                                                                          | $t_{AVQV}$ | $t_{ACC}$   | $\overline{CE}f = V_{IL},$<br>$\overline{OE} = V_{IL}$ | —            | 70  | ns      |
| Chip Enable to Output Delay                                                                      | $t_{ELQV}$ | $t_{CEf}$   | $\overline{OE} = V_{IL}$                               | —            | 70  | ns      |
| Output Enable to Output Delay                                                                    | $t_{GLQV}$ | $t_{OE}$    | —                                                      | —            | 30  | ns      |
| Chip Enable to Output High-Z                                                                     | $t_{EHQZ}$ | $t_{DF}$    | —                                                      | —            | 25  | ns      |
| Output Enable to Output High-Z                                                                   | $t_{GHQZ}$ | $t_{DF}$    | —                                                      | —            | 25  | ns      |
| Output Hold Time From Addresses,<br>$\overline{CE}f$ or $\overline{OE}$ , Whichever Occurs First | $t_{AXQX}$ | $t_{OH}$    | —                                                      | 0            | —   | ns      |
| $\overline{RESET}$ Pin Low to Read Mode                                                          | —          | $t_{READY}$ | —                                                      | —            | 20  | $\mu s$ |

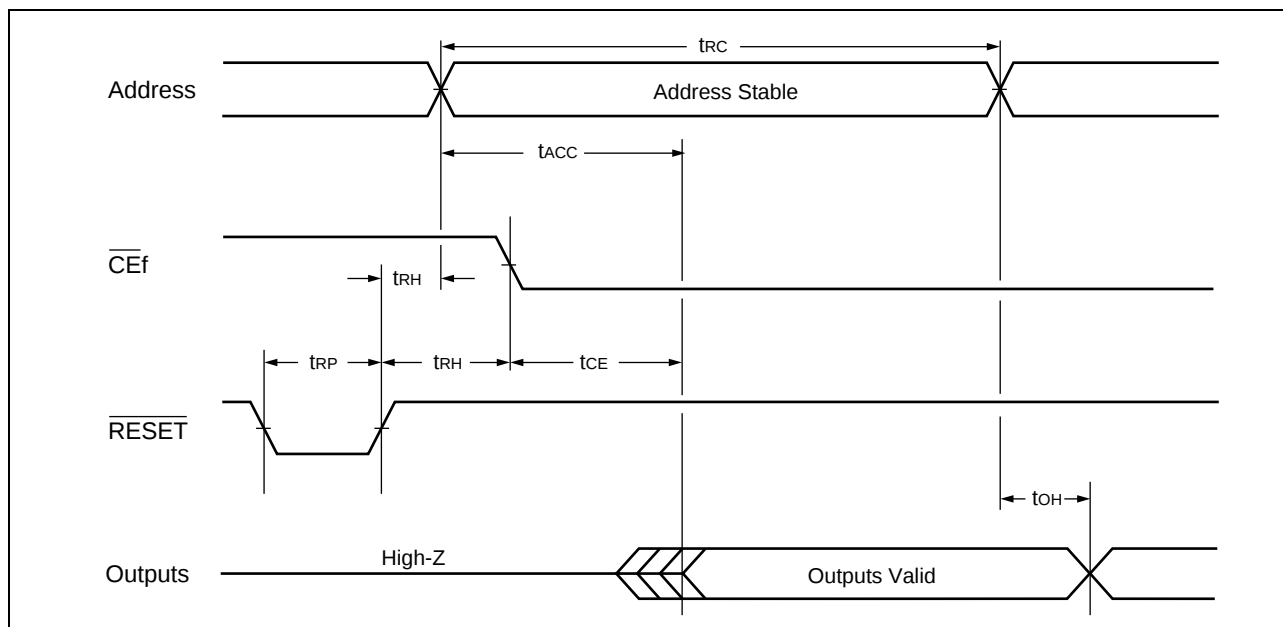
Note: Test Conditions— Output Load:1 TTL gate and 30 pF  
Input rise and fall times: 5 ns  
Input pulse levels: 0.0 V to  $V_{CCf}$   
Timing measurement reference level  
Input:  $0.5 \times V_{CCf}$   
Output:  $0.5 \times V_{CCf}$

# MB84VF5F4F4J1-70

## • Read Operation Timing Diagram (Flash)



## • Hardware Reset/Read Operation Timing Diagram (Flash)



• Write/Erase/Program Operations (Flash)

| Parameter                                                                                 |                                      | Symbol             |                    | Value |     |     | Unit |
|-------------------------------------------------------------------------------------------|--------------------------------------|--------------------|--------------------|-------|-----|-----|------|
|                                                                                           |                                      | JEDEC              | Standard           | Min   | Typ | Max |      |
| Write Cycle Time                                                                          |                                      | t <sub>AVAV</sub>  | t <sub>WC</sub>    | 70    | —   | —   | ns   |
| Address Setup Time                                                                        |                                      | t <sub>AVWL</sub>  | t <sub>AS</sub>    | 0     | —   | —   | ns   |
| Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling                       |                                      | —                  | t <sub>ASO</sub>   | 12    | —   | —   | ns   |
| Address Hold Time                                                                         |                                      | t <sub>WLAX</sub>  | t <sub>AH</sub>    | 30    | —   | —   | ns   |
| Address Hold Time from $\overline{CEf}$ or $\overline{OE}$ High During Toggle Bit Polling |                                      | —                  | t <sub>AHT</sub>   | 0     | —   | —   | ns   |
| Data Setup Time                                                                           |                                      | t <sub>DVWH</sub>  | t <sub>DS</sub>    | 25    | —   | —   | ns   |
| Data Hold Time                                                                            |                                      | t <sub>WHDx</sub>  | t <sub>DH</sub>    | 0     | —   | —   | ns   |
| Output Enable Hold Time                                                                   | Read                                 | —                  | t <sub>OEh</sub>   | 0     | —   | —   | ns   |
|                                                                                           | Toggle and $\overline{Data}$ Polling |                    |                    | 10    | —   | —   | ns   |
| $\overline{CEf}$ High During Toggle Bit Polling                                           |                                      | —                  | t <sub>CEPH</sub>  | 20    | —   | —   | ns   |
| $\overline{OE}$ High During Toggle Bit Polling                                            |                                      | —                  | t <sub>OEPh</sub>  | 20    | —   | —   | ns   |
| Read Recover Time Before Write                                                            |                                      | t <sub>GHWL</sub>  | t <sub>GHWL</sub>  | 0     | —   | —   | ns   |
| Read Recover Time Before Write                                                            |                                      | t <sub>GHEL</sub>  | t <sub>GHEL</sub>  | 0     | —   | —   | ns   |
| $\overline{CEf}$ Setup Time                                                               |                                      | t <sub>ELWL</sub>  | t <sub>CS</sub>    | 0     | —   | —   | ns   |
| $\overline{WE}$ Setup Time                                                                |                                      | t <sub>WLLEL</sub> | t <sub>WS</sub>    | 0     | —   | —   | ns   |
| $\overline{CEf}$ Hold Time                                                                |                                      | t <sub>WHEH</sub>  | t <sub>CH</sub>    | 0     | —   | —   | ns   |
| $\overline{WE}$ Hold Time                                                                 |                                      | t <sub>EHWH</sub>  | t <sub>WH</sub>    | 0     | —   | —   | ns   |
| Write Pulse Width                                                                         |                                      | t <sub>WLWH</sub>  | t <sub>WP</sub>    | 35    | —   | —   | ns   |
| $\overline{CEf}$ Pulse Width                                                              |                                      | t <sub>ELEH</sub>  | t <sub>CP</sub>    | 35    | —   | —   | ns   |
| Write Pulse Width High                                                                    |                                      | t <sub>WHWL</sub>  | t <sub>WPH</sub>   | 20    | —   | —   | ns   |
| $\overline{CEf}$ Pulse Width High                                                         |                                      | t <sub>EHEL</sub>  | t <sub>CPH</sub>   | 20    | —   | —   | ns   |
| Programming Operation                                                                     |                                      | t <sub>WHWH1</sub> | t <sub>WHWH1</sub> | —     | 6   | —   | μs   |
| Sector Erase Operation *1                                                                 |                                      | t <sub>WHWH2</sub> | t <sub>WHWH2</sub> | —     | 0.5 | —   | s    |
| V <sub>CCf</sub> Setup Time                                                               |                                      | —                  | t <sub>VCS</sub>   | 50    | —   | —   | μs   |
| Rise Time to V <sub>ID</sub> *2                                                           |                                      | —                  | t <sub>VIDR</sub>  | 500   | —   | —   | ns   |
| Rise Time to V <sub>ACC</sub> *3                                                          |                                      | —                  | t <sub>VACCR</sub> | 500   | —   | —   | ns   |
| Voltage Transition Time *2                                                                |                                      | —                  | t <sub>VLHT</sub>  | 4     | —   | —   | μs   |
| Write Pulse Width *2                                                                      |                                      | —                  | t <sub>WPP</sub>   | 100   | —   | —   | μs   |

(Continued)

# MB84VF5F4F4J1-70

(Continued)

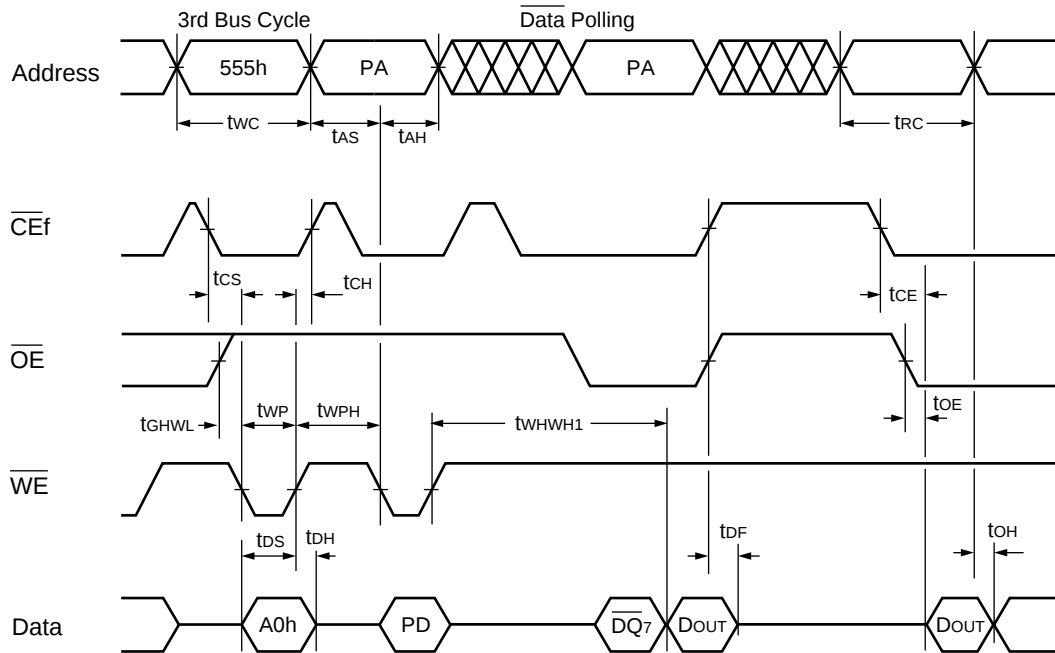
| Parameter                                                | Symbol |            | Value |     |     | Unit    |
|----------------------------------------------------------|--------|------------|-------|-----|-----|---------|
|                                                          | JEDEC  | Standard   | Min   | Typ | Max |         |
| $\overline{OE}$ Setup Time to $\overline{WE}$ Active *2  | —      | $t_{OESP}$ | 4     | —   | —   | $\mu s$ |
| $\overline{CEf}$ Setup Time to $\overline{WE}$ Active *2 | —      | $t_{CSP}$  | 4     | —   | —   | $\mu s$ |
| Recover Time from $RY/\overline{BY}$                     | —      | $t_{RB}$   | 0     | —   | —   | ns      |
| $\overline{RESET}$ Pulse Width                           | —      | $t_{RP}$   | 500   | —   | —   | ns      |
| $\overline{RESET}$ High Level Period Before Read         | —      | $t_{RH}$   | 200   | —   | —   | ns      |
| Program/Erase Valid to $RY/\overline{BY}$ Delay          | —      | $t_{BUSY}$ | —     | —   | 90  | ns      |
| Delay Time from Embedded Output Enable                   | —      | $t_{EOE}$  | —     | —   | 70  | ns      |
| Erase Time-out Time                                      | —      | $t_{TOW}$  | 50    | —   | —   | $\mu s$ |
| Erase Suspend Transition Time                            | —      | $t_{SPD}$  | —     | —   | 20  | $\mu s$ |

\*1: This does not include preprogramming time.

\*2: This timing is for Sector Group Protection operation.

\*3: This timing is for Accelerated Program operation.

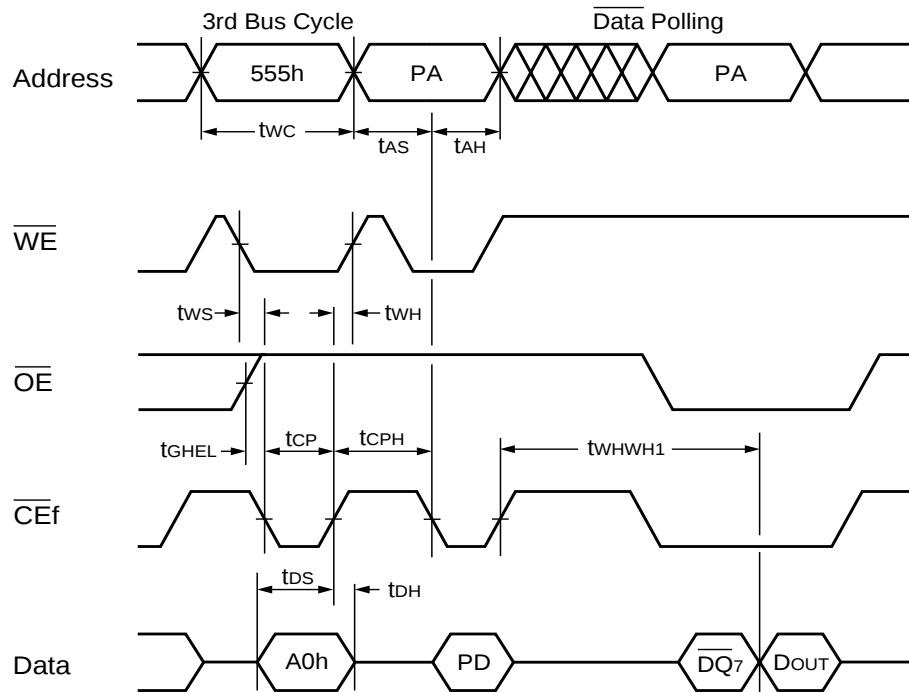
## • Write Cycle ( $\overline{\text{WE}}$ control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at word address.
  - $\overline{\text{DQ7}}$  is the output of the complement of the data written to the device.
  - DOUT is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.

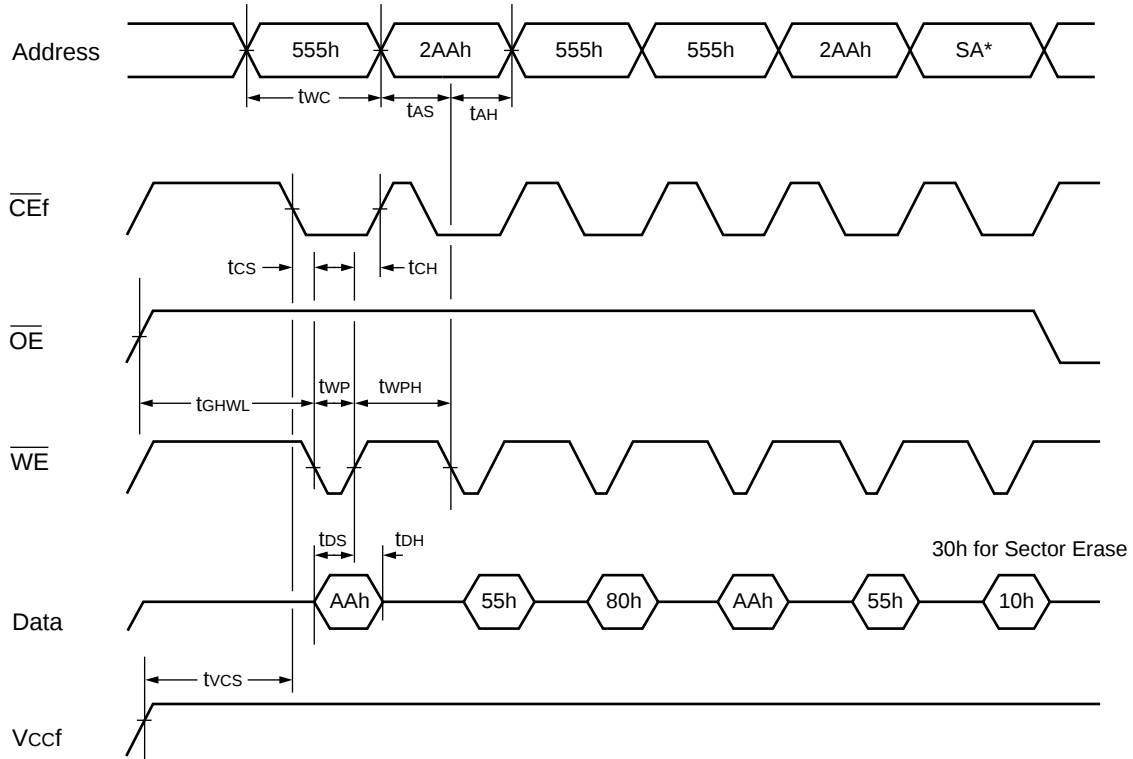
# MB84VF5F4F4J1-70

## • Write Cycle ( $\overline{\text{CEf}}$ control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at word address.
  - $\overline{\text{DQ}}_7$  is the output of the complement of the data written to the device.
  - D<sub>OUT</sub> is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.

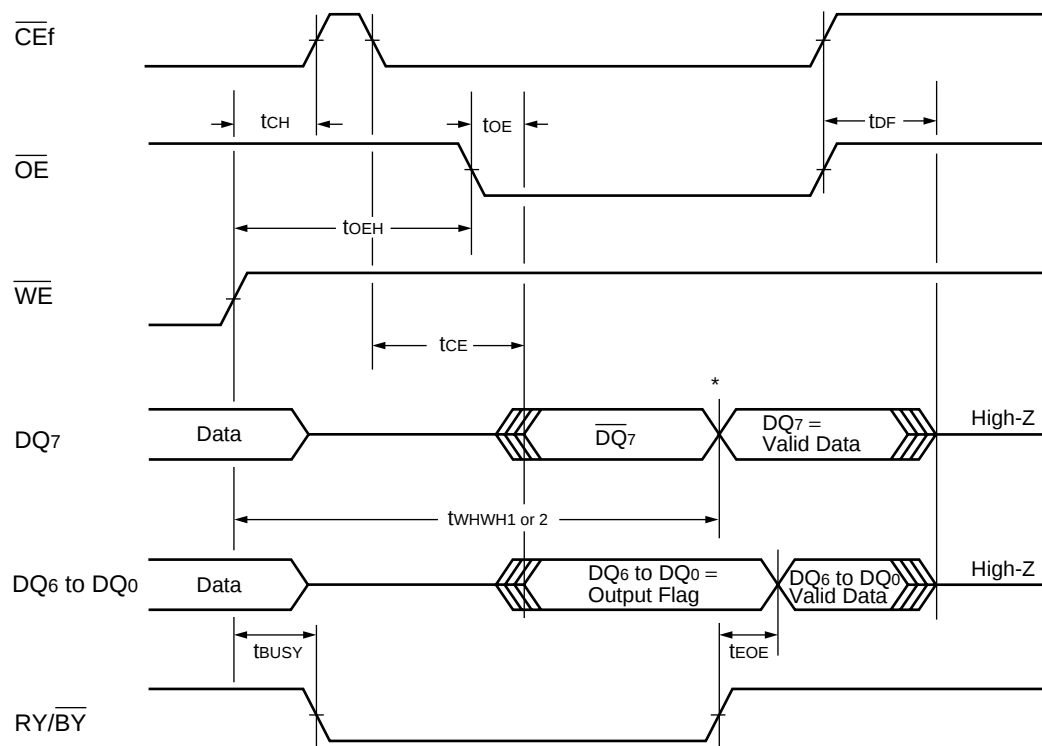
## • AC Waveforms Chip/Sector Erase Operations (Flash)



\* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

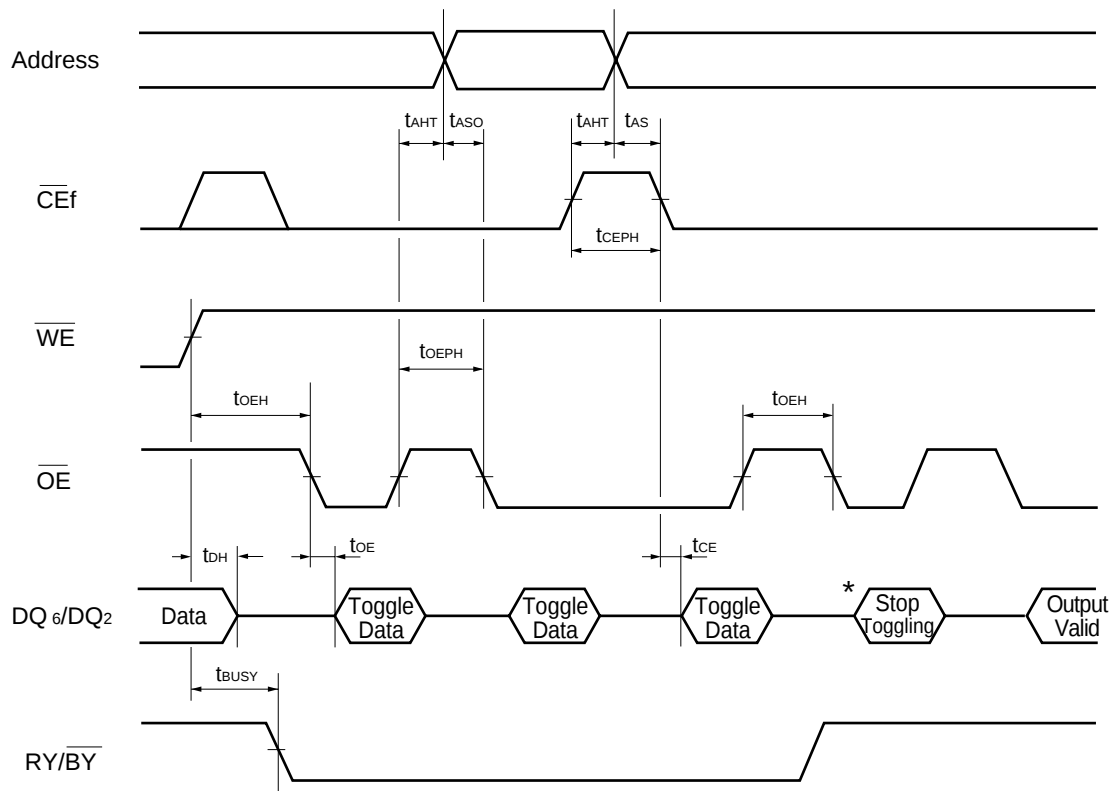
# MB84VF5F4F4J1-70

- AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)



\* :  $DQ_7$  = Valid Data (the device has completed the Embedded operation) .

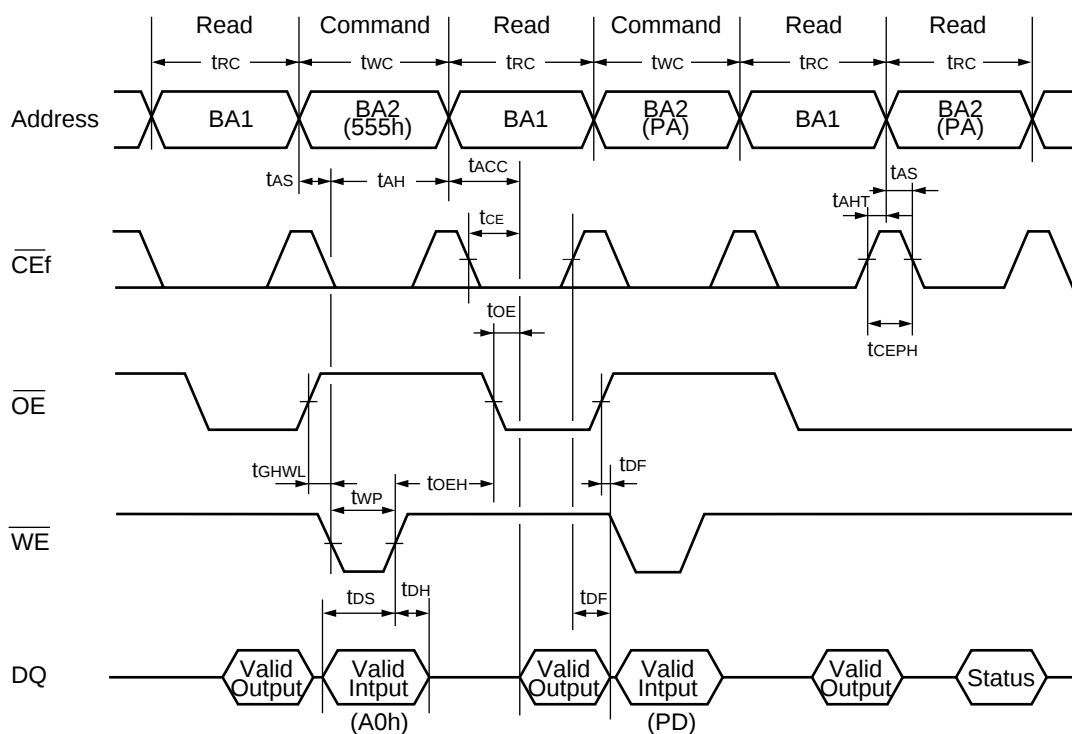
## • AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)



\* : DQ<sub>6</sub> stops toggling (the device has completed the Embedded operation).

# MB84VF5F4F4J1-70

## • Bank-to-bank Read/Write Timing Diagram (Flash)

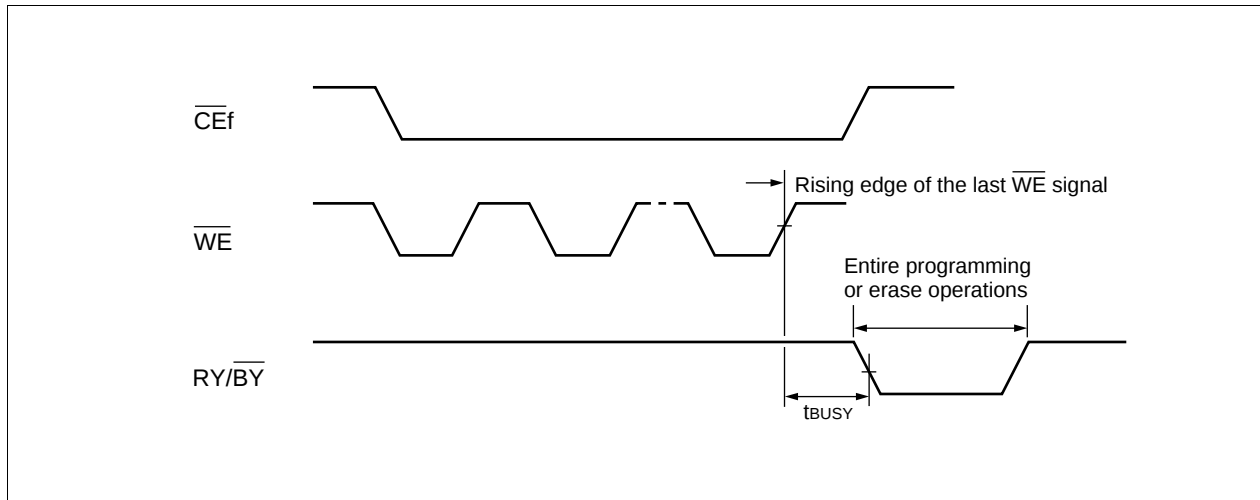


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.

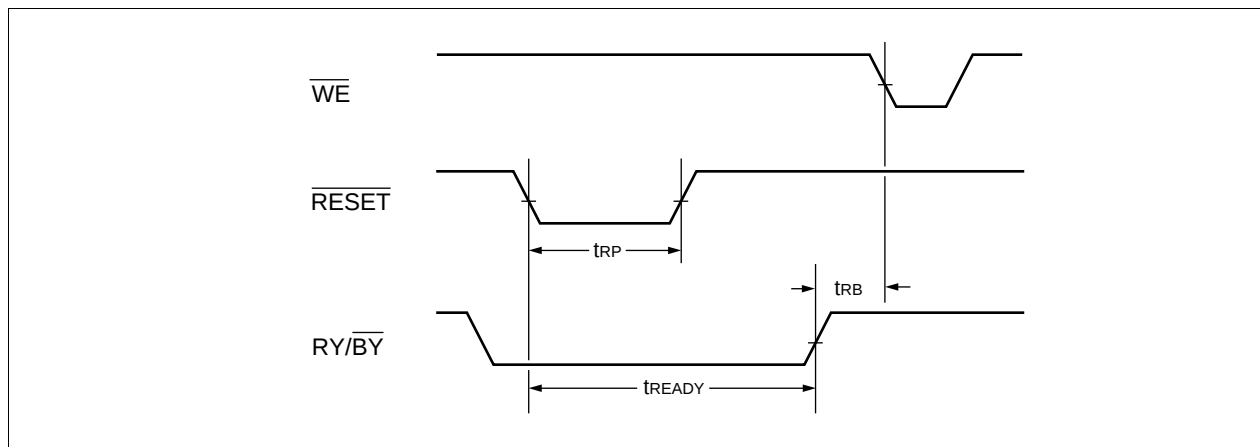
BA1 : Address corresponding to Bank 1

BA2 : Address corresponding to Bank 2

- $\overline{RY}/\overline{BY}$  Timing Diagram during Write/Erase Operations (Flash)

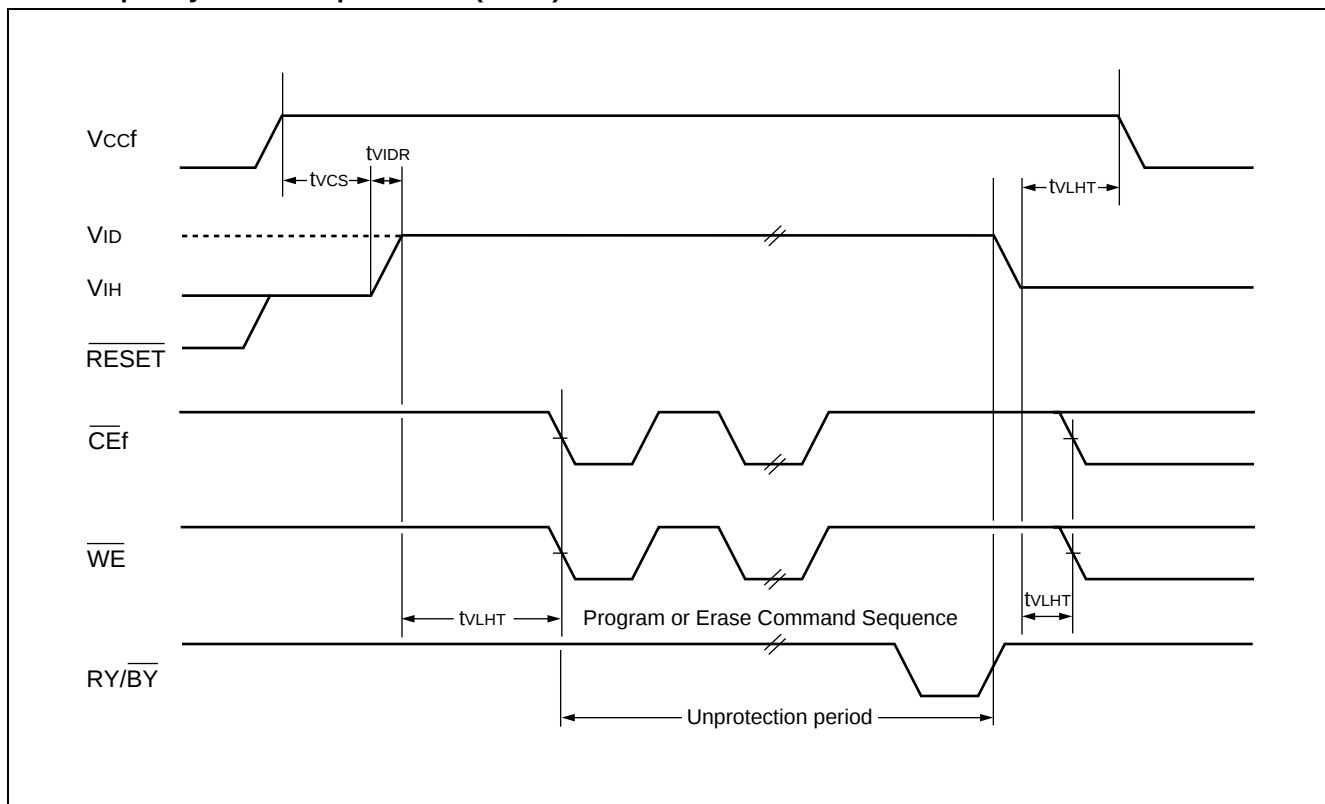


- $\overline{RESET}$ ,  $\overline{RY}/\overline{BY}$  Timing Diagram (Flash)

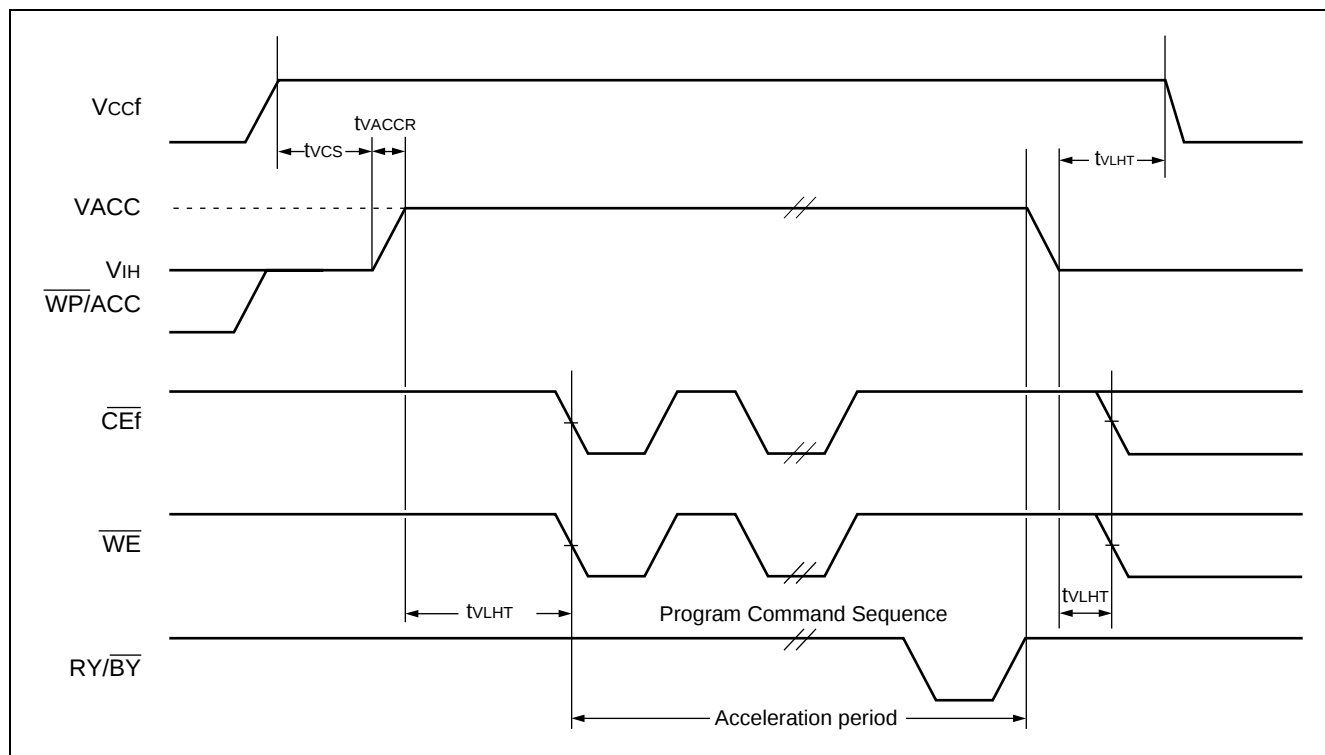


# MB84VF5F4F4J1-70

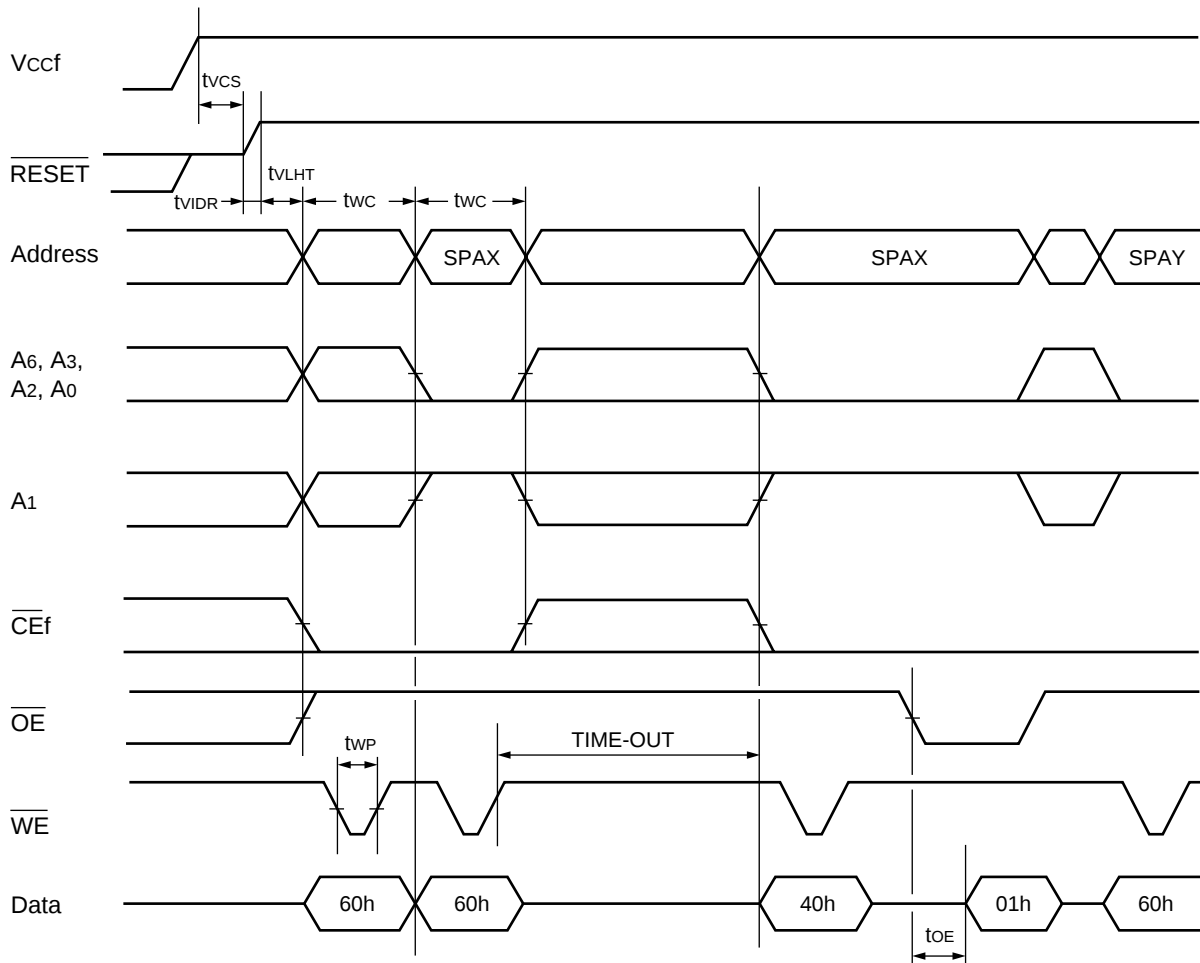
## • Temporary Sector Unprotection (Flash)



## • Acceleration Mode Timing Diagram (Flash)



## • Extended Sector Group Protection (Flash)



SPAX : Sector Group Address to be protected  
 SPAY : Next Sector Group Address to be protected  
 TIME-OUT : Time-Out window = 250  $\mu$ s (Min)

# MB84VF5F4F4J1-70

## 3. Erase and Programming Performance (Flash)

| Parameter             | Value   |     |     | Unit  | Remarks                                    |
|-----------------------|---------|-----|-----|-------|--------------------------------------------|
|                       | Min     | Typ | Max |       |                                            |
| Sector Erase Time     | —       | 0.5 | 2.0 | s     | Excludes programming time prior to erasure |
| Word Programming Time | —       | 6   | 100 | μs    | Excludes system-level overhead             |
| Chip Programming Time | —       | —   | 200 | s     | Excludes system-level overhead             |
| Erase/Program Cycle   | 100,000 | —   | —   | cycle |                                            |

Typical Erase conditions  $T_A = +25^{\circ}\text{C}$ ,  $V_{CCf\_1}$  &  $V_{CCf\_2} = 2.9\text{ V}$

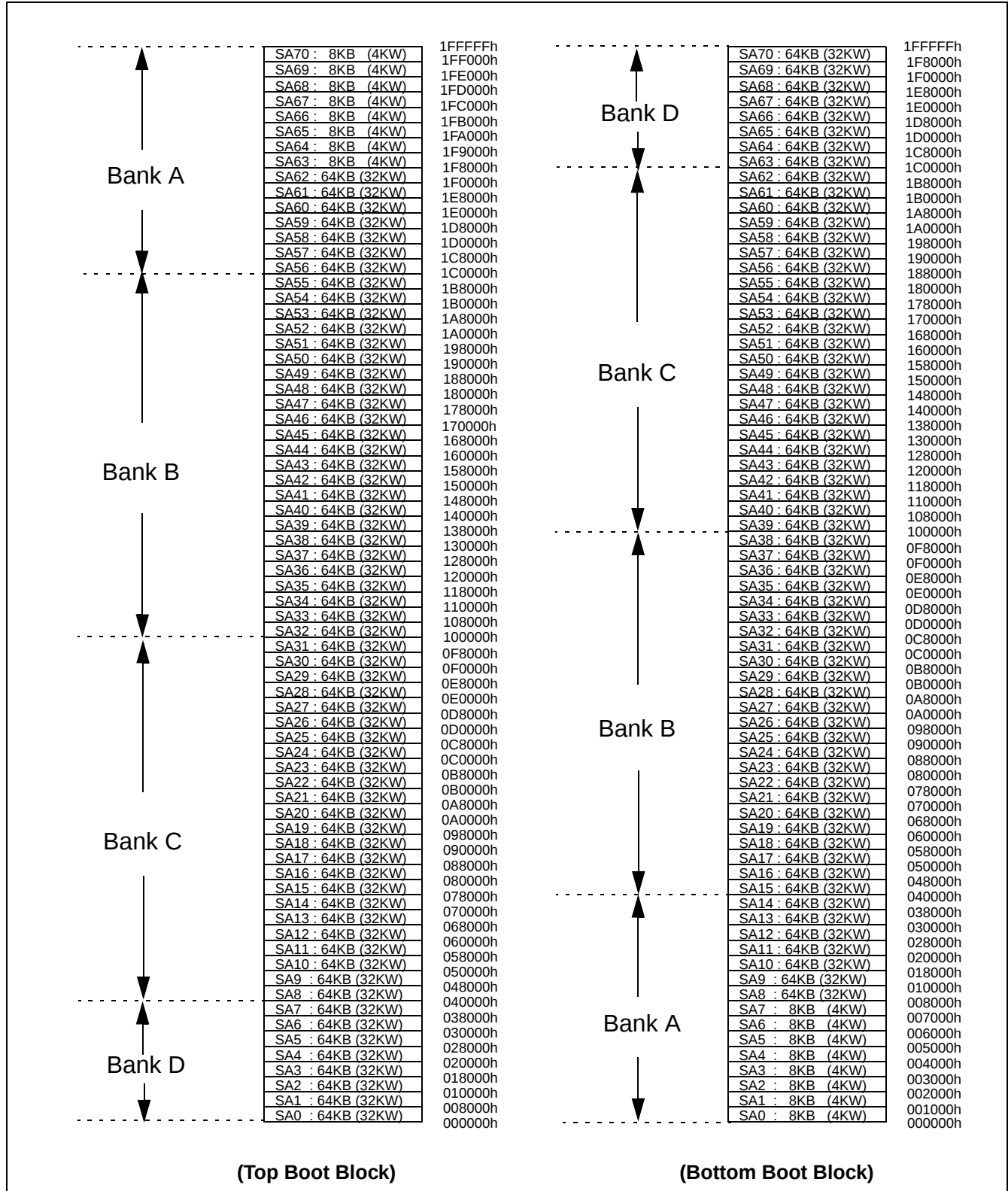
Typical Program conditions  $T_A = +25^{\circ}\text{C}$ ,  $V_{CCf\_1}$  &  $V_{CCf\_2} = 2.9\text{ V}$

Data= Checker

## ■ 32M FLASH MEMORY CHARACTERISTICS for MCP

### 1. Flexible Sector-erase Architecture on Flash Memory

- Eight 4 K words, and sixty three 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



# MB84VF5F4F4J1-70

**FlexBank™ Architecture Table**

| Bank Splits | Bank 1  |             | Bank 2  |              |
|-------------|---------|-------------|---------|--------------|
|             | Volume  | Combination | Volume  | Combination  |
| 1           | 4 Mbit  | Bank A      | 28 Mbit | Bank B, C, D |
| 2           | 12 Mbit | Bank B      | 20 Mbit | Bank A, C, D |
| 3           | 12 Mbit | Bank C      | 20 Mbit | Bank A, B, D |
| 4           | 4 Mbit  | Bank D      | 28 Mbit | Bank A, B, C |

**Example of Virtual Banks Combination Table**

| Bank Splits | Bank 1  |                       |                                                    | Bank 2  |                                      |                        |
|-------------|---------|-----------------------|----------------------------------------------------|---------|--------------------------------------|------------------------|
|             | Volume  | Combination           | Sector Size                                        | Volume  | Combination                          | Sector Size            |
| 1           | 4 Mbit  | Bank A                | 8 × 8 Kbyte/4 Kword<br>+<br>7 × 64 Kbyte/32 Kword  | 28 Mbit | Bank B<br>+<br>Bank C<br>+<br>Bank D | 56 × 64 Kbyte/32 Kword |
| 2           | 8 Mbit  | Bank A<br>+<br>Bank D | 8 × 8 Kbyte/4 Kword<br>+<br>15 × 64 Kbyte/32 Kword | 24 Mbit | Bank B<br>+<br>Bank C                | 48 × 64 Kbyte/32 Kword |
| 3           | 16 Mbit | Bank A<br>+<br>Bank B | 8 × 8 Kbyte/4 Kword<br>+<br>31 × 64 Kbyte/32 Kword | 16 Mbit | Bank C<br>+<br>Bank D                | 32 × 64 Kbyte/32 Kword |

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Sector Address Table (Top Boot Type)

| Bank   | Sector | Sector address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Sector size<br>(Kwords) | Address range      |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------|--------------------|
|        |        | Bank address    |                 |                 | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | A <sub>11</sub> |                         |                    |
|        |        | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> |                 |                 |                 |                 |                 |                 |                 |                         |                    |
| Bank D | SA0    | 0               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 000000h to 007FFFh |
|        | SA1    | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 008000h to 00FFFFh |
|        | SA2    | 0               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 010000h to 017FFFh |
|        | SA3    | 0               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 018000h to 01FFFFh |
|        | SA4    | 0               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 020000h to 027FFFh |
|        | SA5    | 0               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 028000h to 02FFFFh |
|        | SA6    | 0               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 030000h to 037FFFh |
|        | SA7    | 0               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 038000h to 03FFFFh |
| Bank C | SA8    | 0               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 040000h to 047FFFh |
|        | SA9    | 0               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 048000h to 04FFFFh |
|        | SA10   | 0               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 050000h to 057FFFh |
|        | SA11   | 0               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 058000h to 05FFFFh |
|        | SA12   | 0               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 060000h to 067FFFh |
|        | SA13   | 0               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 068000h to 06FFFFh |
|        | SA14   | 0               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 070000h to 077FFFh |
|        | SA15   | 0               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 078000h to 07FFFFh |
|        | SA16   | 0               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 080000h to 087FFFh |
|        | SA17   | 0               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 088000h to 08FFFFh |
|        | SA18   | 0               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 090000h to 097FFFh |
|        | SA19   | 0               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 098000h to 09FFFFh |
|        | SA20   | 0               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 0A0000h to 0A7FFFh |
|        | SA21   | 0               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 0A8000h to 0AFFFFh |
|        | SA22   | 0               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 0B0000h to 0B7FFFh |
|        | SA23   | 0               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 0B8000h to 0BFFFFh |
|        | SA24   | 0               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 0C0000h to 0C7FFFh |
|        | SA25   | 0               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 0C8000h to 0CFFFFh |
|        | SA26   | 0               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 0D0000h to 0D7FFFh |
|        | SA27   | 0               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 0D8000h to 0DFFFFh |
|        | SA28   | 0               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 0E0000h to 0E7FFFh |
|        | SA29   | 0               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 0E8000h to 0EFFFFh |
|        | SA30   | 0               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 0F0000h to 0F7FFFh |
|        | SA31   | 0               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 0F8000h to 0FFFFFh |

(Continued)

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(Continued)

| Bank   | Sector | Sector address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Sector size<br>(Kwords) | Address range      |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------|--------------------|
|        |        | Bank address    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                         |                    |
|        |        | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | A <sub>11</sub> |                         |                    |
| Bank B | SA32   | 1               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 100000h to 107FFFh |
|        | SA33   | 1               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 108000h to 10FFFFh |
|        | SA34   | 1               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 110000h to 117FFFh |
|        | SA35   | 1               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 118000h to 11FFFFh |
|        | SA36   | 1               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 120000h to 127FFFh |
|        | SA37   | 1               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 128000h to 12FFFFh |
|        | SA38   | 1               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 130000h to 137FFFh |
|        | SA39   | 1               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 138000h to 13FFFFh |
|        | SA40   | 1               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 140000h to 147FFFh |
|        | SA41   | 1               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 148000h to 14FFFFh |
|        | SA42   | 1               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 150000h to 157FFFh |
|        | SA43   | 1               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 158000h to 15FFFFh |
|        | SA44   | 1               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 160000h to 167FFFh |
|        | SA45   | 1               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 168000h to 16FFFFh |
|        | SA46   | 1               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 170000h to 177FFFh |
|        | SA47   | 1               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 178000h to 17FFFFh |
|        | SA48   | 1               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 180000h to 187FFFh |
|        | SA49   | 1               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 188000h to 18FFFFh |
|        | SA50   | 1               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 190000h to 197FFFh |
|        | SA51   | 1               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 198000h to 19FFFFh |
| SA52   | 1      | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32              | 1A0000h to 1A7FFFh      |                    |
| SA53   | 1      | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32              | 1A8000h to 1AFFFFh      |                    |
| SA54   | 1      | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32              | 1B0000h to 1B7FFFh      |                    |
| SA55   | 1      | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32              | 1B8000h to 1BFFFFh      |                    |
| Bank A | SA56   | 1               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 1C0000h to 1C7FFFh |
|        | SA57   | 1               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 1C8000h to 1CFFFFh |
|        | SA58   | 1               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 1D0000h to 1D7FFFh |
|        | SA59   | 1               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 1D8000h to 1DFFFFh |
|        | SA60   | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 1E0000h to 1E7FFFh |
|        | SA61   | 1               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 1E8000h to 1EFFFFh |
|        | SA62   | 1               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 1F0000h to 1F7FFFh |
|        | SA63   | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 0               | X               | 4                       | 1F8000h to 1F8FFFh |
|        | SA64   | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 1               | X               | 4                       | 1F9000h to 1F9FFFh |
|        | SA65   | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 0               | X               | 4                       | 1FA000h to 1FAFFFh |
|        | SA66   | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 1               | X               | 4                       | 1FB000h to 1FBFFFh |
|        | SA67   | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | X               | 4                       | 1FC000h to 1FCFFFh |
|        | SA68   | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | X               | 4                       | 1FD000h to 1FDFFFh |
|        | SA69   | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | X               | 4                       | 1FE000h to 1FEFFFh |
|        | SA70   | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | X               | 4                       | 1FF000h to 1FFFFFh |

Sector Address Table (Bottom Boot Type)

| Bank   | Sector | Sector address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Sector size<br>(Kwords) | Address range       |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------|---------------------|
|        |        | Bank address    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                         |                     |
|        |        | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | A <sub>11</sub> |                         |                     |
| Bank D | SA70   | 1               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 1F8000h to 1FFFFFFh |
|        | SA69   | 1               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 1F0000h to 1F7FFFh  |
|        | SA68   | 1               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 1E8000h to 1EFFFFh  |
|        | SA67   | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 1E0000h to 1E7FFFh  |
|        | SA66   | 1               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 1D8000h to 1DFFFFh  |
|        | SA65   | 1               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 1D0000h to 1D7FFFh  |
|        | SA64   | 1               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 1C8000h to 1CFFFFh  |
|        | SA63   | 1               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 1C0000h to 1C7FFFh  |
| Bank C | SA62   | 1               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 1B8000h to 1BFFFFh  |
|        | SA61   | 1               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 1B0000h to 1B7FFFh  |
|        | SA60   | 1               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 1A8000h to 1AFFFFh  |
|        | SA59   | 1               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 1A0000h to 1A7FFFh  |
|        | SA58   | 1               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 198000h to 19FFFFh  |
|        | SA57   | 1               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 190000h to 197FFFh  |
|        | SA56   | 1               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 188000h to 18FFFFh  |
|        | SA55   | 1               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 180000h to 187FFFh  |
|        | SA54   | 1               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 178000h to 17FFFFh  |
|        | SA53   | 1               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 170000h to 177FFFh  |
|        | SA52   | 1               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 168000h to 16FFFFh  |
|        | SA51   | 1               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 160000h to 167FFFh  |
|        | SA50   | 1               | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 158000h to 15FFFFh  |
|        | SA49   | 1               | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 150000h to 157FFFh  |
|        | SA48   | 1               | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 148000h to 14FFFFh  |
|        | SA47   | 1               | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 140000h to 147FFFh  |
|        | SA46   | 1               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 138000h to 13FFFFh  |
|        | SA45   | 1               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 130000h to 137FFFh  |
|        | SA44   | 1               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 128000h to 12FFFFh  |
|        | SA43   | 1               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 120000h to 127FFFh  |
|        | SA42   | 1               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 118000h to 11FFFFh  |
|        | SA41   | 1               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 110000h to 117FFFh  |
|        | SA40   | 1               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 108000h to 10FFFFh  |
|        | SA39   | 1               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 100000h to 107FFFh  |

(Continued)

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| Bank   | Sector | Sector address  |                 |                 |                 |                 |                 |                 |                 |                 |                 | Sector size<br>(Kwords) | Address range       |
|--------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------|---------------------|
|        |        | Bank address    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                         |                     |
|        |        | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | A <sub>11</sub> |                         |                     |
| Bank B | SA38   | 0               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 0F8000h to 0FFFFFFh |
|        | SA37   | 0               | 1               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 0F0000h to 0F7FFFh  |
|        | SA36   | 0               | 1               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 0E8000h to 0EFFFFh  |
|        | SA35   | 0               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 0E0000h to 0E7FFFh  |
|        | SA34   | 0               | 1               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 0D8000h to 0DFFFFh  |
|        | SA33   | 0               | 1               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 0D0000h to 0D7FFFh  |
|        | SA32   | 0               | 1               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 0C8000h to 0CFFFFh  |
|        | SA31   | 0               | 1               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 0C0000h to 0C7FFFh  |
|        | SA30   | 0               | 1               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 0B8000h to 0BFFFFh  |
|        | SA29   | 0               | 1               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 0B0000h to 0B7FFFh  |
|        | SA28   | 0               | 1               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 0A8000h to 0AFFFFh  |
|        | SA27   | 0               | 1               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 0A0000h to 0A7FFFh  |
|        | SA26   | 0               | 1               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 098000h to 09FFFFh  |
|        | SA25   | 0               | 1               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 090000h to 097FFFh  |
|        | SA24   | 0               | 1               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 088000h to 08FFFFh  |
|        | SA23   | 0               | 1               | 0               | 0               | 0               | 0               | X               | X               | X               | X               | 32                      | 080000h to 087FFFh  |
|        | SA22   | 0               | 0               | 1               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 078000h to 07FFFFh  |
|        | SA21   | 0               | 0               | 1               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 070000h to 077FFFh  |
|        | SA20   | 0               | 0               | 1               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 068000h to 06FFFFh  |
|        | SA19   | 0               | 0               | 1               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 060000h to 067FFFh  |
| SA18   | 0      | 0               | 1               | 0               | 1               | 1               | X               | X               | X               | X               | 32              | 058000h to 05FFFFh      |                     |
| SA17   | 0      | 0               | 1               | 0               | 1               | 0               | X               | X               | X               | X               | 32              | 050000h to 057FFFh      |                     |
| SA16   | 0      | 0               | 1               | 0               | 0               | 1               | X               | X               | X               | X               | 32              | 048000h to 04FFFFh      |                     |
| SA15   | 0      | 0               | 1               | 0               | 0               | 0               | X               | X               | X               | X               | 32              | 040000h to 047FFFh      |                     |
| Bank A | SA14   | 0               | 0               | 0               | 1               | 1               | 1               | X               | X               | X               | X               | 32                      | 038000h to 03FFFFh  |
|        | SA13   | 0               | 0               | 0               | 1               | 1               | 0               | X               | X               | X               | X               | 32                      | 030000h to 037FFFh  |
|        | SA12   | 0               | 0               | 0               | 1               | 0               | 1               | X               | X               | X               | X               | 32                      | 028000h to 02FFFFh  |
|        | SA11   | 0               | 0               | 0               | 1               | 0               | 0               | X               | X               | X               | X               | 32                      | 020000h to 027FFFh  |
|        | SA10   | 0               | 0               | 0               | 0               | 1               | 1               | X               | X               | X               | X               | 32                      | 018000h to 01FFFFh  |
|        | SA9    | 0               | 0               | 0               | 0               | 1               | 0               | X               | X               | X               | X               | 32                      | 010000h to 017FFFh  |
|        | SA8    | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | X               | 32                      | 008000h to 00FFFFh  |
|        | SA7    | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 1               | X               | 4                       | 007000h to 007FFFh  |
|        | SA6    | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 0               | X               | 4                       | 006000h to 006FFFh  |
|        | SA5    | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | X               | 4                       | 005000h to 005FFFh  |
|        | SA4    | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               | X               | 4                       | 004000h to 004FFFh  |
|        | SA3    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | X               | 4                       | 003000h to 003FFFh  |
|        | SA2    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | X               | 4                       | 002000h to 002FFFh  |
|        | SA1    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | X               | 4                       | 001000h to 001FFFh  |
|        | SA0    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | X               | 4                       | 000000h to 000FFFh  |

Sector Group Address Table (Top Boot Type)

| Sector group | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | Sectors      |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0         | 0               | 0               | 0               | 0               | 0               | 0               | X               | X               | X               | SA0          |
| SGA1         | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | SA1 to SA3   |
|              |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |              |
|              |                 |                 |                 |                 | 1               | 1               |                 |                 |                 |              |
| SGA2         | 0               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA4 to SA7   |
| SGA3         | 0               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA8 to SA11  |
| SGA4         | 0               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA12 to SA15 |
| SGA5         | 0               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA16 to SA19 |
| SGA6         | 0               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA20 to SA23 |
| SGA7         | 0               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA24 to SA27 |
| SGA8         | 0               | 1               | 1               | 1               | X               | X               | X               | X               | X               | SA28 to SA31 |
| SGA9         | 1               | 0               | 0               | 0               | X               | X               | X               | X               | X               | SA32 to SA35 |
| SGA10        | 1               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA36 to SA39 |
| SGA11        | 1               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA40 to SA43 |
| SGA12        | 1               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA44 to SA47 |
| SGA13        | 1               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA48 to SA51 |
| SGA14        | 1               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA52 to SA55 |
| SGA15        | 1               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA56 to SA59 |
| SGA16        | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | SA60 to SA62 |
|              |                 |                 |                 |                 | 0               | 1               |                 |                 |                 |              |
|              |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |              |
| SGA17        | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 0               | SA63         |
| SGA18        | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | 1               | SA64         |
| SGA19        | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 0               | SA65         |
| SGA20        | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | 1               | SA66         |
| SGA21        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 0               | SA67         |
| SGA22        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | 1               | SA68         |
| SGA23        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 0               | SA69         |
| SGA24        | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | 1               | SA70         |

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Sector Group Address Table (Bottom Boot Type)

| Sector group | A <sub>20</sub> | A <sub>19</sub> | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> | A <sub>15</sub> | A <sub>14</sub> | A <sub>13</sub> | A <sub>12</sub> | Sectors      |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------|
| SGA0         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | SA0          |
| SGA1         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | SA1          |
| SGA2         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | SA2          |
| SGA3         | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | SA3          |
| SGA4         | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               | SA4          |
| SGA5         | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | SA5          |
| SGA6         | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 0               | SA6          |
| SGA7         | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 1               | 1               | SA7          |
| SGA8         | 0               | 0               | 0               | 0               | 0               | 1               | X               | X               | X               | SA8 to SA10  |
|              |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |              |
|              |                 |                 |                 |                 | 1               | 1               |                 |                 |                 |              |
| SGA9         | 0               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA11 to SA14 |
| SGA10        | 0               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA15 to SA18 |
| SGA11        | 0               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA19 to SA22 |
| SGA12        | 0               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA23 to SA26 |
| SGA13        | 0               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA27 to SA30 |
| SGA14        | 0               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA31 to SA34 |
| SGA15        | 0               | 1               | 1               | 1               | X               | X               | X               | X               | X               | SA35 to SA38 |
| SGA16        | 1               | 0               | 0               | 0               | X               | X               | X               | X               | X               | SA39 to SA42 |
| SGA17        | 1               | 0               | 0               | 1               | X               | X               | X               | X               | X               | SA43 to SA46 |
| SGA18        | 1               | 0               | 1               | 0               | X               | X               | X               | X               | X               | SA47 to SA50 |
| SGA19        | 1               | 0               | 1               | 1               | X               | X               | X               | X               | X               | SA51 to SA54 |
| SGA20        | 1               | 1               | 0               | 0               | X               | X               | X               | X               | X               | SA55 to SA58 |
| SGA21        | 1               | 1               | 0               | 1               | X               | X               | X               | X               | X               | SA59 to SA62 |
| SGA22        | 1               | 1               | 1               | 0               | X               | X               | X               | X               | X               | SA63 to SA66 |
| SGA23        | 1               | 1               | 1               | 1               | 0               | 0               | X               | X               | X               | SA67 to SA69 |
|              |                 |                 |                 |                 | 0               | 1               |                 |                 |                 |              |
|              |                 |                 |                 |                 | 1               | 0               |                 |                 |                 |              |
| SGA24        | 1               | 1               | 1               | 1               | 1               | 1               | X               | X               | X               | SA70         |

**Sector Group Protection Verify Autoselect Codes Table (Top Boot Type)**

| Type                    | A <sub>20</sub> to A <sub>12</sub> | A <sub>6</sub>  | A <sub>3</sub>  | A <sub>2</sub>  | A <sub>1</sub>  | A <sub>0</sub>  | Code (HEX) |
|-------------------------|------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------|
| Manufacture's Code      | BA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | 04h        |
| Device Code             | BA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | 227Eh      |
| Extended Device Code    | BA                                 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IL</sub> | 220Ah      |
|                         | BA                                 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | 2201h      |
| Sector Group Protection | SA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | 01h*       |

\* : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

**Expanded Autoselect Code Table (Top Boot Type)**

| Type                    | Code  | DQ <sub>15</sub> | DQ <sub>14</sub> | DQ <sub>13</sub> | DQ <sub>12</sub> | DQ <sub>11</sub> | DQ <sub>10</sub> | DQ <sub>9</sub> | DQ <sub>8</sub> | DQ <sub>7</sub> | DQ <sub>6</sub> | DQ <sub>5</sub> | DQ <sub>4</sub> | DQ <sub>3</sub> | DQ <sub>2</sub> | DQ <sub>1</sub> | DQ <sub>0</sub> |
|-------------------------|-------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Manufacture's Code      | 04h   | 0                | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               |
| Device Code             | 227Eh | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 1               | 1               | 1               | 1               | 1               | 1               | 0               |
| Extended Device Code    | 220Ah | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | 0               |
|                         | 2201h | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               |
| Sector Group Protection | 01h   | 0                | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               |

**Sector Group Protection Verify Autoselect Codes Table (Bottom Boot Type)**

| Type                    | A <sub>20</sub> to A <sub>12</sub> | A <sub>6</sub>  | A <sub>3</sub>  | A <sub>2</sub>  | A <sub>1</sub>  | A <sub>0</sub>  | Code (HEX) |
|-------------------------|------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------|
| Manufacture's Code      | BA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | 04h        |
| Device Code             | BA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | 227Eh      |
| Extended Device Code    | BA                                 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IL</sub> | 220Ah      |
|                         | BA                                 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | 2200h      |
| Sector Group Protection | SA                                 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | 01h*       |

\* : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

**Expanded Autoselect Code Table (Bottom Boot Type)**

| Type                    | Code  | DQ <sub>15</sub> | DQ <sub>14</sub> | DQ <sub>13</sub> | DQ <sub>12</sub> | DQ <sub>11</sub> | DQ <sub>10</sub> | DQ <sub>9</sub> | DQ <sub>8</sub> | DQ <sub>7</sub> | DQ <sub>6</sub> | DQ <sub>5</sub> | DQ <sub>4</sub> | DQ <sub>3</sub> | DQ <sub>2</sub> | DQ <sub>1</sub> | DQ <sub>0</sub> |
|-------------------------|-------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Manufacture's Code      | 04h   | 0                | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 0               |
| Device Code             | 227Eh | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 1               | 1               | 1               | 1               | 1               | 1               | 0               |
| Extended Device Code    | 220Ah | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 0               | 0               | 0               | 1               | 0               | 1               | 0               |
|                         | 2200h | 0                | 0                | 1                | 0                | 0                | 0                | 1               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |
| Sector Group Protection | 01h   | 0                | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 1               |

# MB84VF5F4F4J1-70

Command Definitions Table

| Command sequence                               | Bus write cycles req'd | First bus write cycle       |      | Second bus write cycle |                   | Third bus write cycle          |      | Fourth bus read/write cycle               |                   | Fifth bus write cycle |      | Sixth bus write cycle |      |
|------------------------------------------------|------------------------|-----------------------------|------|------------------------|-------------------|--------------------------------|------|-------------------------------------------|-------------------|-----------------------|------|-----------------------|------|
|                                                |                        | Addr.                       | Data | Addr.                  | Data              | Addr.                          | Data | Addr.                                     | Data              | Addr.                 | Data | Addr.                 | Data |
| Read/Reset <sup>*1</sup>                       | 1                      | XXXh                        | F0h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Read/Reset <sup>*1</sup>                       | 3                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | F0h  | RA <sup>*7</sup>                          | RD <sup>*11</sup> | —                     | —    | —                     | —    |
| Autoselect                                     | 3                      | 555h                        | AAh  | 2AAh                   | 55h               | (BA <sup>*10</sup> )<br>555h   | 90h  | —                                         | —                 | —                     | —    | —                     | —    |
| Program                                        | 4                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | A0h  | PA <sup>*8</sup>                          | PD <sup>*12</sup> | —                     | —    | —                     | —    |
| Program Suspend                                | 1                      | BA <sup>*10</sup>           | B0h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Program Resume                                 | 1                      | BA <sup>*10</sup>           | 30h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Chip Erase                                     | 6                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | 80h  | 555h                                      | AAh               | 2AAh                  | 55h  | 555h                  | 10h  |
| Sector Erase                                   | 6                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | 80h  | 555h                                      | AAh               | 2AAh                  | 55h  | SA <sup>*9</sup>      | 30h  |
| Erase Suspend                                  | 1                      | BA <sup>*10</sup>           | B0h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Erase Resume                                   | 1                      | BA <sup>*10</sup>           | 30h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Set to Fast Mode                               | 3                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | 20h  | —                                         | —                 | —                     | —    | —                     | —    |
| Fast Program <sup>*2</sup>                     | 2                      | XXXh                        | A0h  | PA <sup>*8</sup>       | PD <sup>*12</sup> | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Reset from Fast Mode <sup>*2</sup>             | 2                      | BA <sup>*10</sup>           | 90h  | XXXh                   | F0h <sup>*6</sup> | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| Extended Sector Group Protection <sup>*3</sup> | 4                      | XXXh                        | 60h  | SPA <sup>*13</sup>     | 60h               | SPA <sup>*13</sup>             | 40h  | SPA <sup>*13</sup>                        | SD <sup>*14</sup> | —                     | —    | —                     | —    |
| Query <sup>*4</sup>                            | 1                      | (BA <sup>*10</sup> )<br>55h | 98h  | —                      | —                 | —                              | —    | —                                         | —                 | —                     | —    | —                     | —    |
| HiddenROM Entry                                | 3                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | 88h  | —                                         | —                 | —                     | —    | —                     | —    |
| HiddenROM Program <sup>*5</sup>                | 4                      | 555h                        | AAh  | 2AAh                   | 55h               | 555h                           | A0h  | (HRA <sup>*15</sup> )<br>PA <sup>*8</sup> | PD <sup>*12</sup> | —                     | —    | —                     | —    |
| HiddenROM Exit <sup>*5</sup>                   | 4                      | 555h                        | AAh  | 2AAh                   | 55h               | (HRBA <sup>*16</sup> )<br>555h | 90h  | XXXh                                      | 00h               | —                     | —    | —                     | —    |

(Continued)

(Continued)

- \*1 : Both of these reset commands are equivalent.
- \*2 : This command is valid during Fast Mode.
- \*3 : This command is valid while  $\overline{\text{RESET}} = V_{\text{ID}}$ .
- \*4 : The valid address are  $A_6$  to  $A_0$ .
- \*5 : This command is valid during HiddenROM mode.
- \*6 : The date "00h" is also acceptable.
- \*7: RA = Address of the memory location to be read
- \*8: PA = Address of the memory location to be programmed  
Addresses are latched on the falling edge of the write pulse.
- \*9: SA = Address of the sector to be erased. The combination of  $A_{20}$ ,  $A_{19}$ ,  $A_{18}$ ,  $A_{17}$ ,  $A_{16}$ ,  $A_{15}$ ,  $A_{14}$ ,  $A_{13}$ , and  $A_{12}$  will uniquely select any sector.
- \*10:BA = Bank Address ( $A_{20}$  to  $A_{18}$ )
- \*11:RD = Data read from location RA during read operation.
- \*12:PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- \*13:SPA = Sector group address to be protected. Set sector group address and  $(A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0)$ .
- \*14:SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- \*15:HRA = Address of the HiddenROM area  
Top Boot Type      Word Mode : 1FFF80h to 1FFFFFh  
Bottom Boot Type Word Mode : 000000h to 00007Fh
- \*16:HRBA = Bank Address of the HiddenROM area  
Top Boot Type      :  $A_{20} = A_{19} = A_{18} = 1$   
Bottom Boot Type :  $A_{20} = A_{19} = A_{18} = 0$

- Notes:
- Address bits  $A_{20}$  to  $A_{11} = X = "H"$  or  $"L"$  for all address commands except or Program Address (PA) , Sector Address (SA) , Bank Address (BA) .
  - Bus operations are defined in "User Bus Operations Tables ( $\overline{\text{BYTE}} = V_{\text{IH}}$ )" (■DEVICE BUS OPERATION).
  - The system should generate the following address patterns :  
Word Mode : 555h or 2AAh to addresses  $A_{10}$  to  $A_0$
  - Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
  - Command combinations not described in "Command Definitions Table" are illegal.

# MB84VF5F4F4J1-70

## 2. AC Characteristics

### • Read Only Operations Characteristics

| Parameter                                                                                       | Symbols    |             | Condition                                             | Value* |     | Unit    |
|-------------------------------------------------------------------------------------------------|------------|-------------|-------------------------------------------------------|--------|-----|---------|
|                                                                                                 | JEDEC      | Standard    |                                                       | Min    | Max |         |
| Read Cycle Time                                                                                 | $t_{AVAV}$ | $t_{RC}$    | —                                                     | 70     | —   | ns      |
| Address to Output Delay                                                                         | $t_{AVQV}$ | $t_{ACC}$   | $\overline{CE} = V_{IL},$<br>$\overline{OE} = V_{IL}$ | —      | 70  | ns      |
| Chip Enable to Output Delay                                                                     | $t_{ELQV}$ | $t_{CE}$    | $\overline{OE} = V_{IL}$                              | —      | 70  | ns      |
| Output Enable to Output Delay                                                                   | $t_{GLQV}$ | $t_{OE}$    | —                                                     | —      | 30  | ns      |
| Chip Enable to Output High-Z                                                                    | $t_{EHQZ}$ | $t_{DF}$    | —                                                     | —      | 25  | ns      |
| Output Enable to Output High-Z                                                                  | $t_{GHQZ}$ | $t_{DF}$    | —                                                     | —      | 25  | ns      |
| Output Hold Time from Addresses,<br>$\overline{CE}$ or $\overline{OE}$ , Whichever Occurs First | $t_{AXQX}$ | $t_{OH}$    | —                                                     | 0      | —   | ns      |
| $\overline{RESET}$ Pin Low to Read Mode                                                         | —          | $t_{READY}$ | —                                                     | —      | 20  | $\mu s$ |

\* : Test Conditions — Output Load : 1 TTL gate and 30 pF  
 Input rise and fall times : 5 ns  
 Input pulse levels : 0.0 V to 3.0 V  
 Timing measurement reference level  
 Input:  $0.5 \times V_{CCf}$   
 Output:  $0.5 \times V_{CCf}$

## • Write/Erase/Program Operations

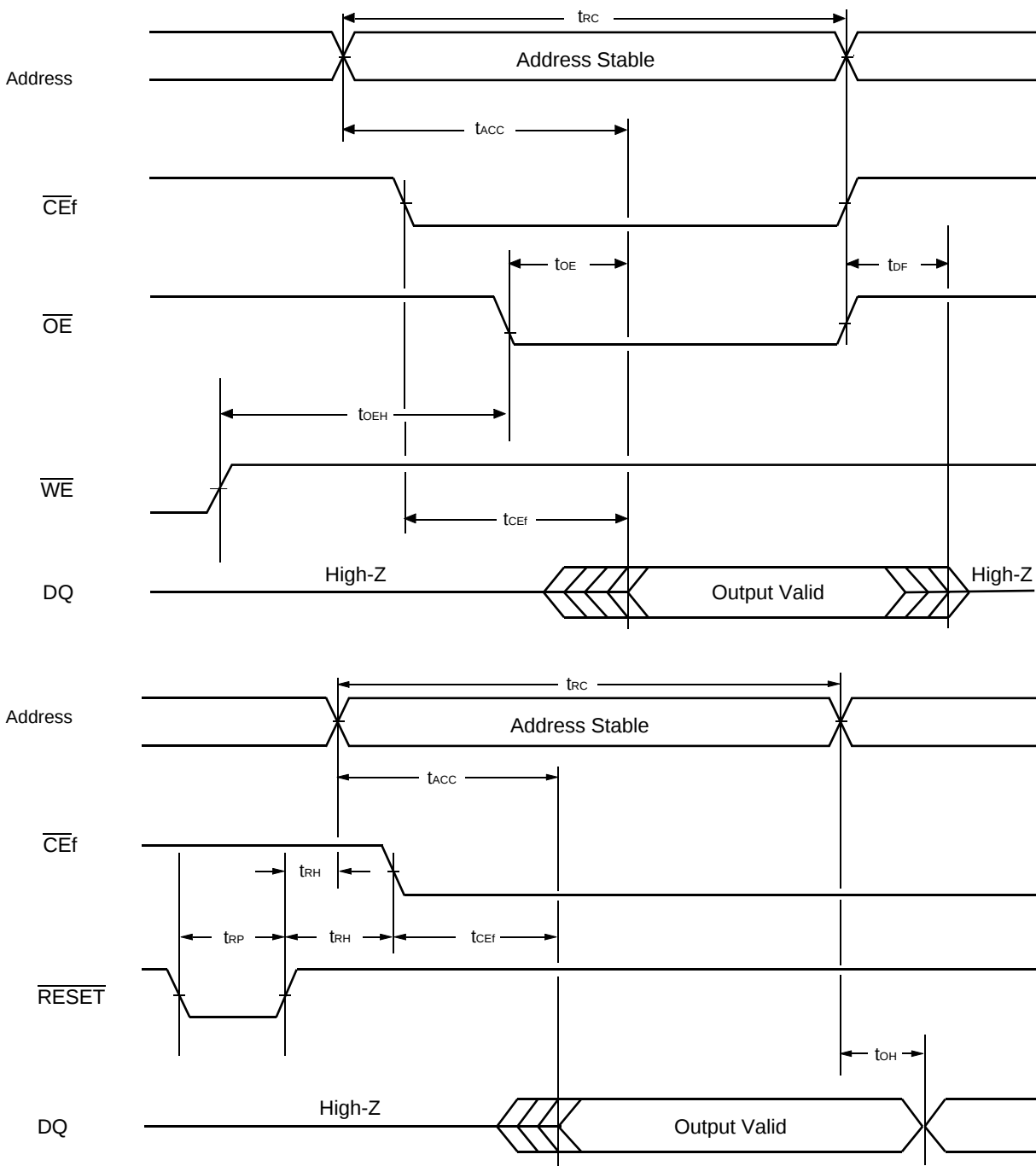
| Parameter                                                                                               |                                             | Symbols            |                    | Value |     |     | Unit |
|---------------------------------------------------------------------------------------------------------|---------------------------------------------|--------------------|--------------------|-------|-----|-----|------|
|                                                                                                         |                                             | JEDEC              | Standard           | Min   | Typ | Max |      |
| Write Cycle Time                                                                                        |                                             | t <sub>AVAV</sub>  | t <sub>WC</sub>    | 70    | —   | —   | ns   |
| Address Setup Time                                                                                      |                                             | t <sub>AVWL</sub>  | t <sub>AS</sub>    | 0     | —   | —   | ns   |
| Address Setup Time to $\overline{\text{OE}}$ Low During Toggle Bit Polling                              |                                             | —                  | t <sub>ASO</sub>   | 12    | —   | —   | ns   |
| Address Hold Time                                                                                       |                                             | t <sub>WLAX</sub>  | t <sub>AH</sub>    | 45    | —   | —   | ns   |
| Address Hold Time from $\overline{\text{CEf}}$ or $\overline{\text{OE}}$ High During Toggle Bit Polling |                                             | —                  | t <sub>AHT</sub>   | 0     | —   | —   | ns   |
| Data Setup Time                                                                                         |                                             | t <sub>DVWH</sub>  | t <sub>DS</sub>    | 30    | —   | —   | ns   |
| Data Hold Time                                                                                          |                                             | t <sub>WHDx</sub>  | t <sub>DH</sub>    | 0     | —   | —   | ns   |
| Output Enable Hold Time                                                                                 | Read                                        | —                  | t <sub>OEh</sub>   | 0     | —   | —   | ns   |
|                                                                                                         | Toggle and $\overline{\text{Data}}$ Polling |                    |                    | 10    | —   | —   | ns   |
| $\overline{\text{CEf}}$ High During Toggle Bit Polling                                                  |                                             | —                  | t <sub>CEPH</sub>  | 20    | —   | —   | ns   |
| $\overline{\text{OE}}$ High During Toggle Bit Polling                                                   |                                             | —                  | t <sub>OEPH</sub>  | 20    | —   | —   | ns   |
| Read Recover Time Before Write                                                                          |                                             | t <sub>GHWL</sub>  | t <sub>GHWL</sub>  | 0     | —   | —   | ns   |
| Read Recover Time Before Write                                                                          |                                             | t <sub>GHEL</sub>  | t <sub>GHEL</sub>  | 0     | —   | —   | ns   |
| $\overline{\text{CEf}}$ Setup Time                                                                      |                                             | t <sub>ELWL</sub>  | t <sub>CS</sub>    | 0     | —   | —   | ns   |
| $\overline{\text{WE}}$ Setup Time                                                                       |                                             | t <sub>WLEL</sub>  | t <sub>WS</sub>    | 0     | —   | —   | ns   |
| $\overline{\text{CEf}}$ Hold Time                                                                       |                                             | t <sub>WHEH</sub>  | t <sub>CH</sub>    | 0     | —   | —   | ns   |
| $\overline{\text{WE}}$ Hold Time                                                                        |                                             | t <sub>EHWH</sub>  | t <sub>WH</sub>    | 0     | —   | —   | ns   |
| Write Pulse Width                                                                                       |                                             | t <sub>WLWH</sub>  | t <sub>WP</sub>    | 35    | —   | —   | ns   |
| $\overline{\text{CEf}}$ Pulse Width                                                                     |                                             | t <sub>ELEH</sub>  | t <sub>CP</sub>    | 35    | —   | —   | ns   |
| Write Pulse Width High                                                                                  |                                             | t <sub>WHWL</sub>  | t <sub>WPH</sub>   | 25    | —   | —   | ns   |
| $\overline{\text{CEf}}$ Pulse Width High                                                                |                                             | t <sub>EHEL</sub>  | t <sub>CPH</sub>   | 25    | —   | —   | ns   |
| Sector Erase Operation *1                                                                               |                                             | t <sub>WHWH2</sub> | t <sub>WHWH2</sub> | —     | 0.5 | —   | s    |
| V <sub>ccf</sub> Setup Time                                                                             |                                             | —                  | t <sub>VCS</sub>   | 50    | —   | —   | μs   |
| Rise Time to V <sub>ID</sub> *2                                                                         |                                             | —                  | t <sub>VIDR</sub>  | 500   | —   | —   | ns   |
| Rise Time to V <sub>ID</sub> *2                                                                         |                                             | —                  | t <sub>VACCR</sub> | 500   | —   | —   | ns   |
| Voltage Transition Time *2                                                                              |                                             | —                  | t <sub>VLHT</sub>  | 4     | —   | —   | μs   |
| Write Pulse Width *2                                                                                    |                                             | —                  | t <sub>WPP</sub>   | 100   | —   | —   | μs   |
| $\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active *2                                   |                                             | —                  | t <sub>OESP</sub>  | 4     | —   | —   | μs   |
| $\overline{\text{CEf}}$ Setup Time to $\overline{\text{WE}}$ Active *2                                  |                                             | —                  | t <sub>CSP</sub>   | 4     | —   | —   | μs   |
| Recover Time from RY/ $\overline{\text{BY}}$                                                            |                                             | —                  | t <sub>RB</sub>    | 0     | —   | —   | ns   |
| $\overline{\text{RESET}}$ Pulse Width                                                                   |                                             | —                  | t <sub>RP</sub>    | 500   | —   | —   | ns   |
| $\overline{\text{RESET}}$ High Level Period before Read                                                 |                                             | —                  | t <sub>RH</sub>    | 200   | —   | —   | ns   |
| Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay                                                 |                                             | —                  | t <sub>BUSY</sub>  | —     | —   | 90  | ns   |
| Delay Time from Embedded Output Enable                                                                  |                                             | —                  | t <sub>EOE</sub>   | —     | —   | 70  | ns   |
| Erase Time-Out Time                                                                                     |                                             | —                  | t <sub>TOW</sub>   | 50    | —   | —   | μs   |
| Erase Suspend Transition Time                                                                           |                                             | —                  | t <sub>SPD</sub>   | —     | —   | 20  | μs   |

\*1: This does not include the preprogramming time.

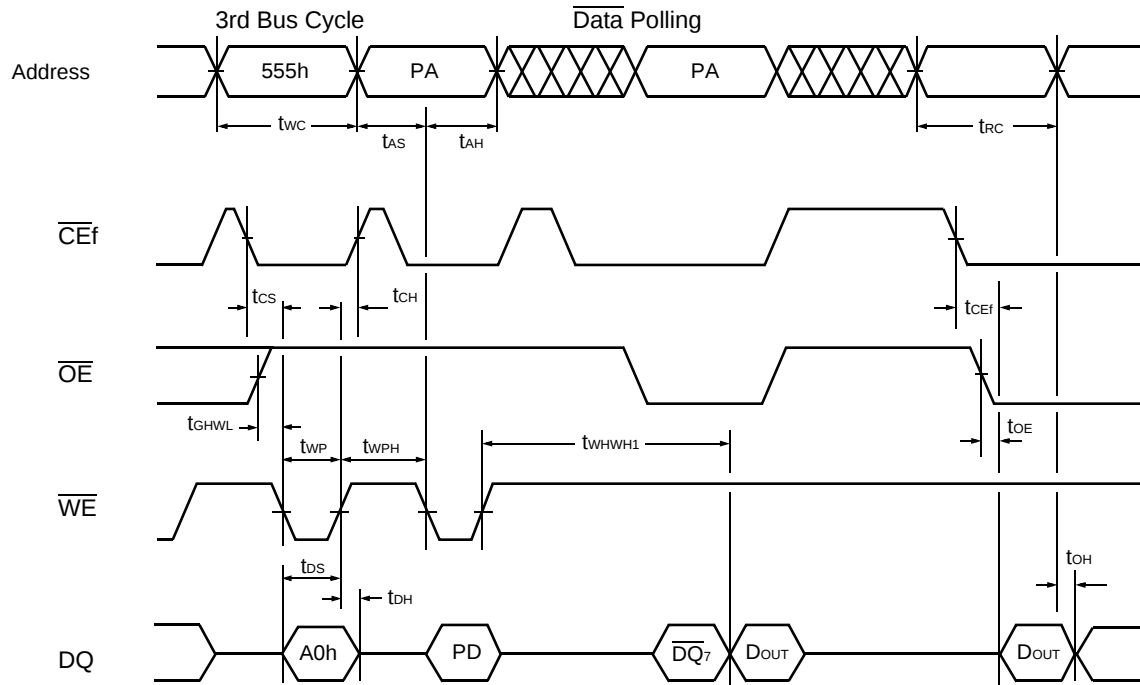
\*2: This timing is for Sector Group Protection operation.

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## • Read Cycle (Flash)

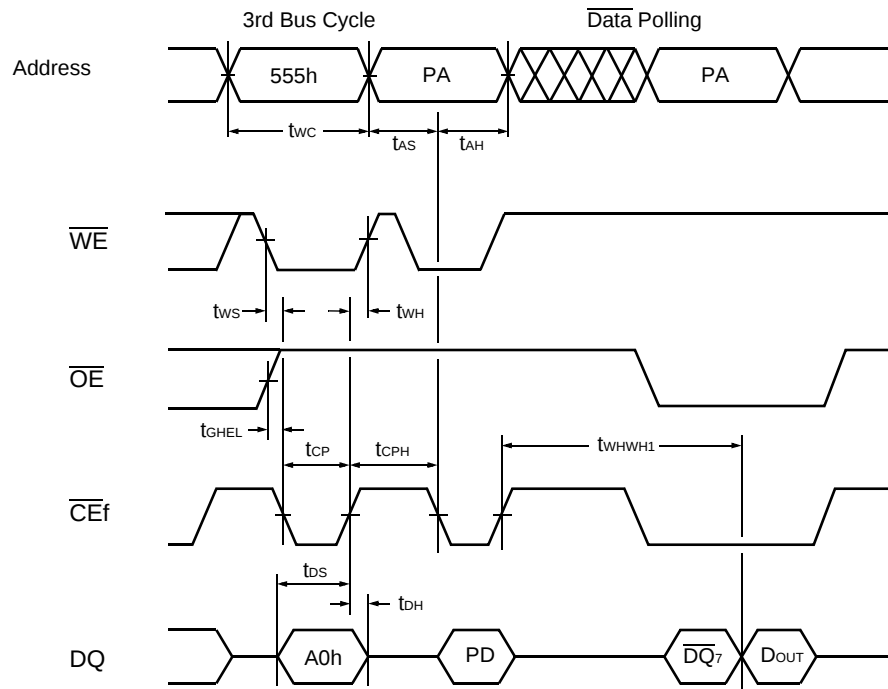


## • Write Cycle ( $\overline{\text{WE}}$ control) (Flash)



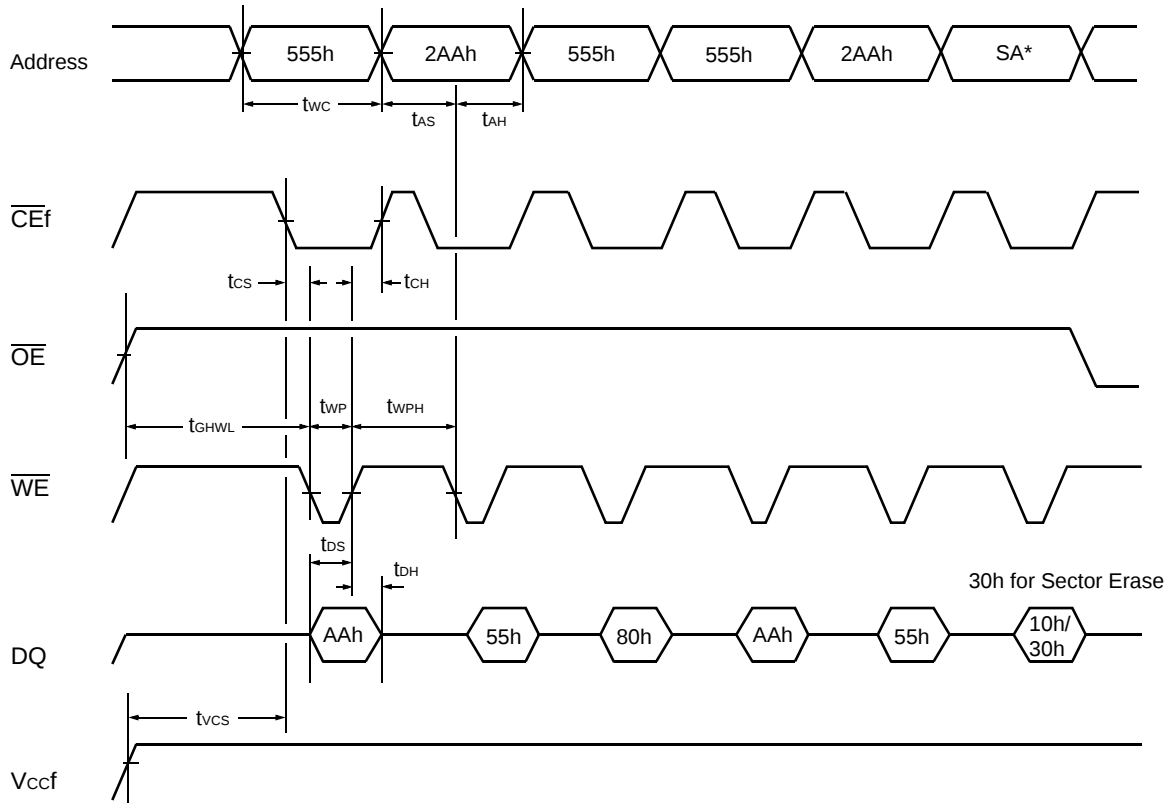
- Notes :
- PA is address of the memory location to be programmed.
  - $\overline{\text{DQ}}_7$  is the output of the complement of the data written to the device.
  - DOUT is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.
  - These waveforms are for the  $\times 16$  mode.

## • Write Cycle ( $\overline{\text{CEf}}$ control) (Flash)



- Notes :
- PA is address of the memory location to be programmed.
  - $\overline{\text{DQ}}_7$  is the output of the complement of the data written to the device.
  - $\text{D}_{\text{OUT}}$  is the output of the data written to the device.
  - Figure indicates last two bus cycles out of four bus cycle sequence.
  - These waveforms are for the  $\times 16$  mode.

## • AC Waveforms Chip/Sector Erase Operations (Flash)

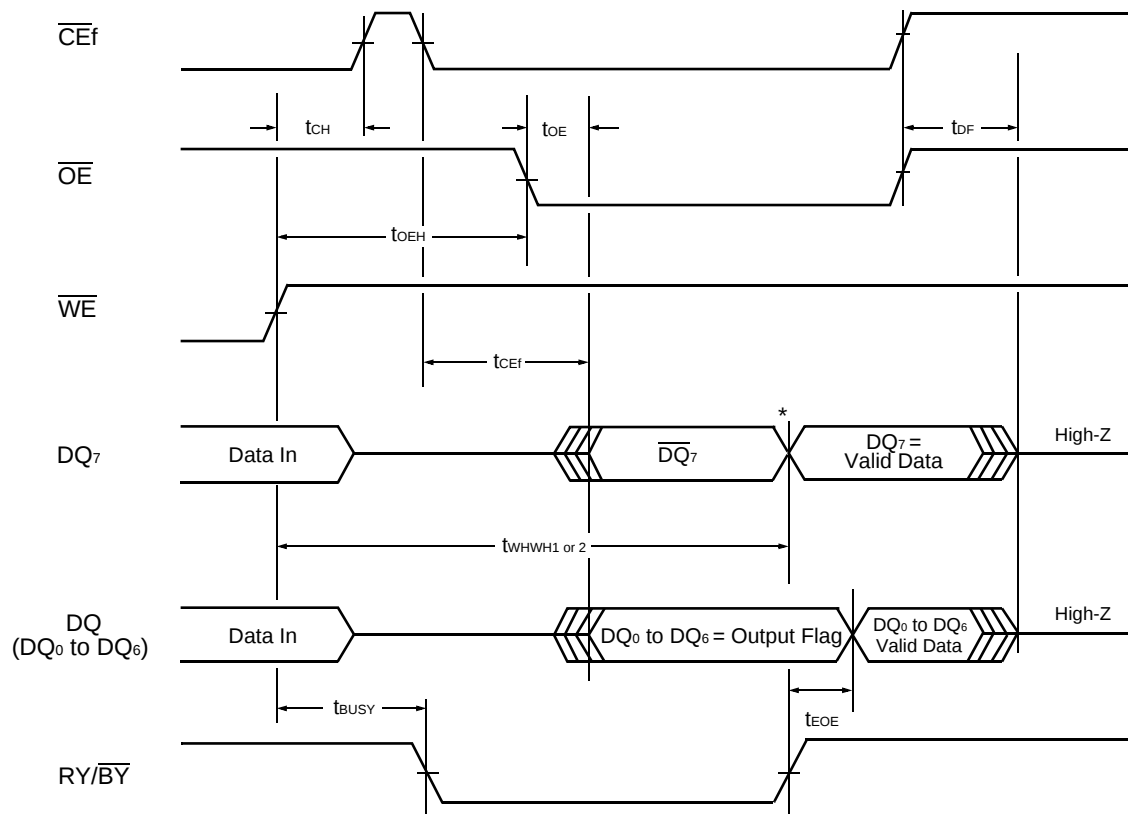


\*: SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

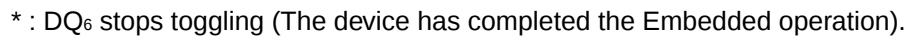
Note: These waveform are for the  $\times 16$  mode.

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## • AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)

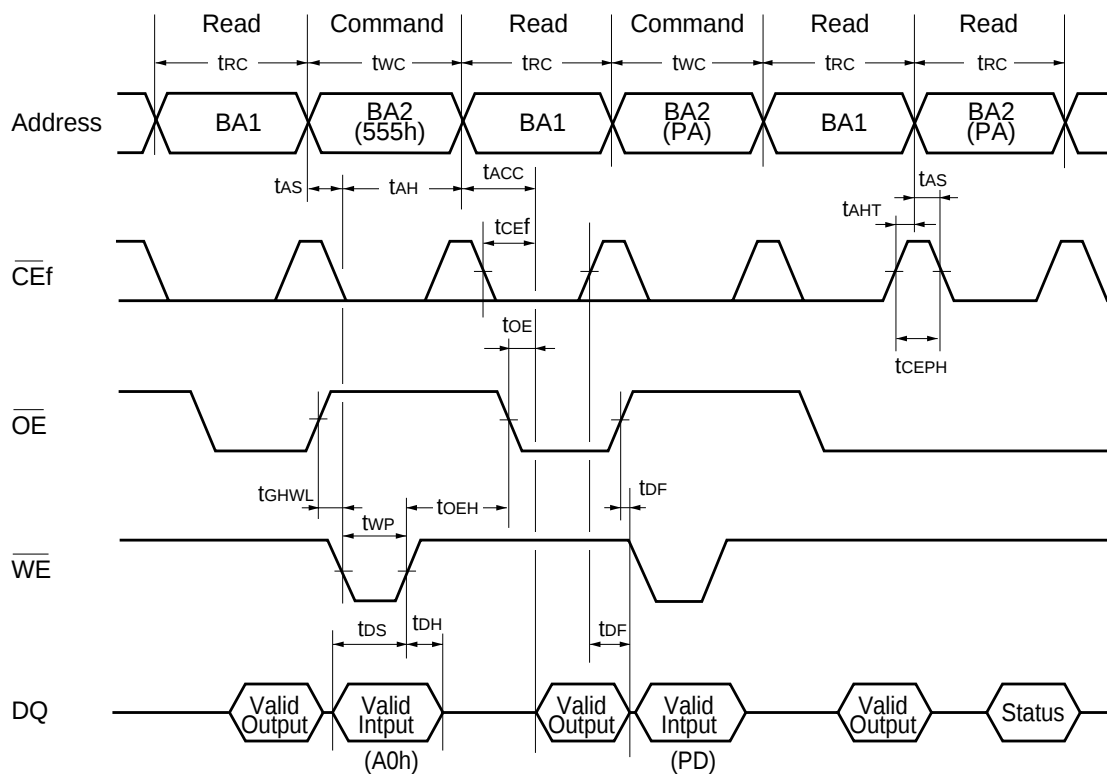


\* :  $DQ_7$  = Valid Data (The device has completed the Embedded operation.)



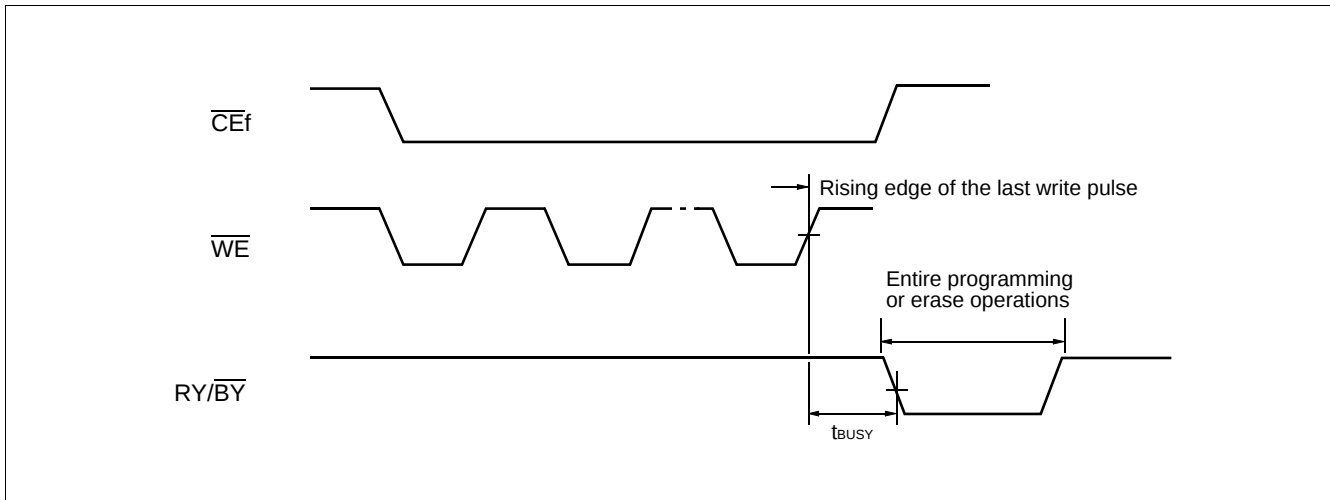
# MB84VF5F4F4J1-70

## • Bank-to-bank Read/Write Timing Diagram (Flash)

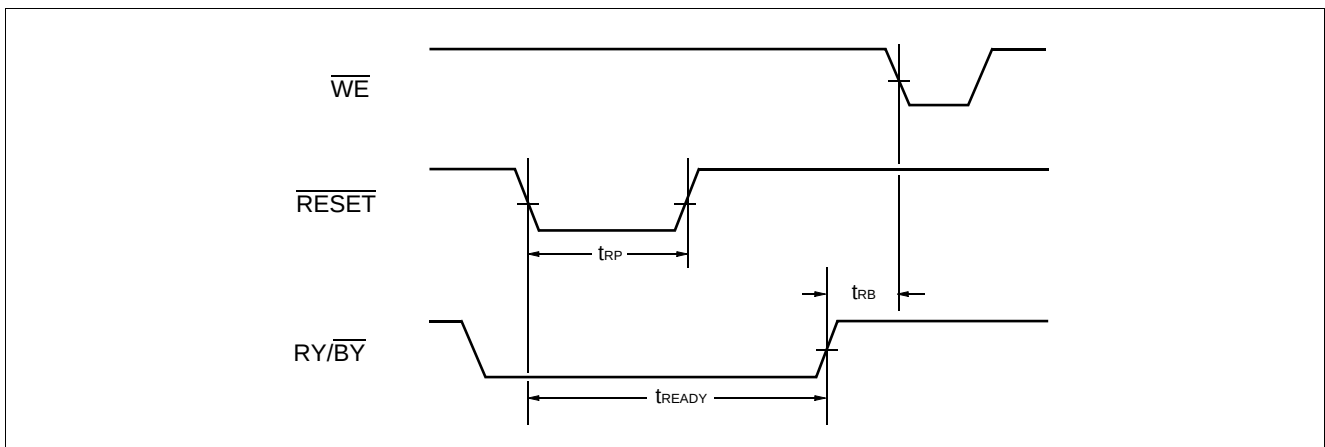


Note: This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.  
 BA1: Address of Bank 1.  
 BA2: Address of Bank 2.

- $\overline{\text{RY}}/\overline{\text{BY}}$  Timing Diagram during Write/Erase Operations (Flash)

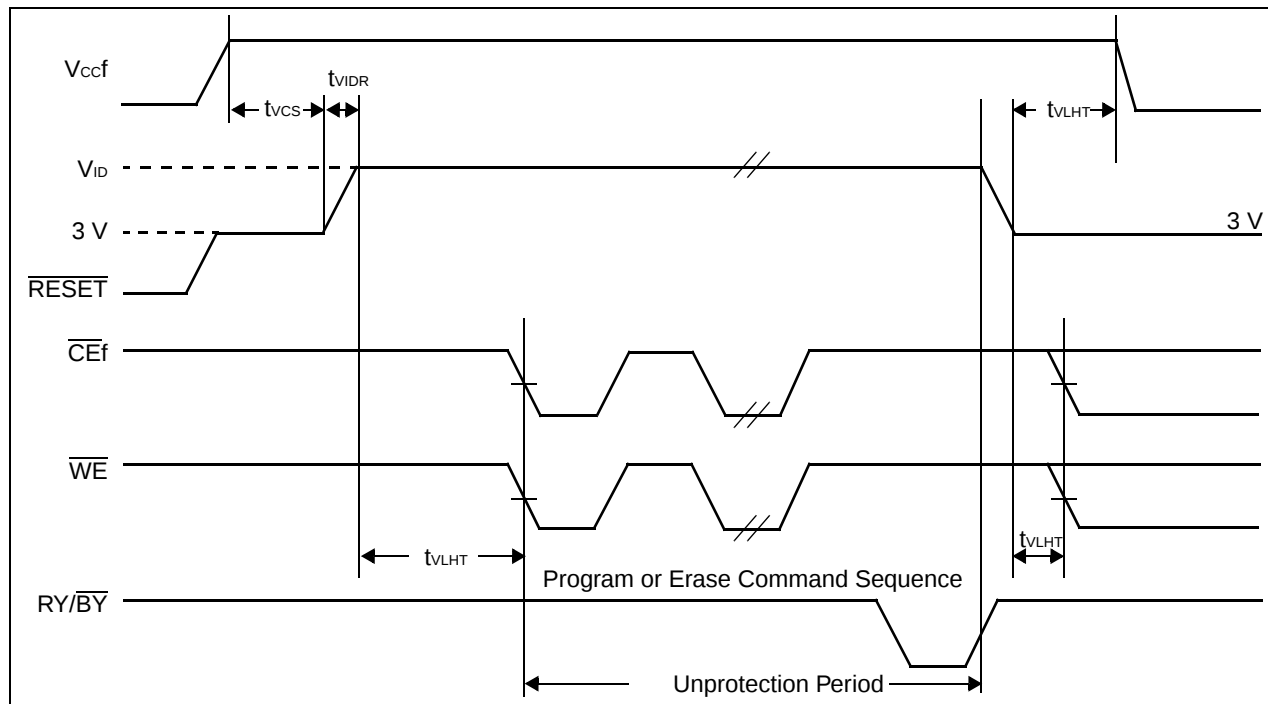


- $\overline{\text{RESET}}$ ,  $\overline{\text{RY}}/\overline{\text{BY}}$  Timing Diagram (Flash)

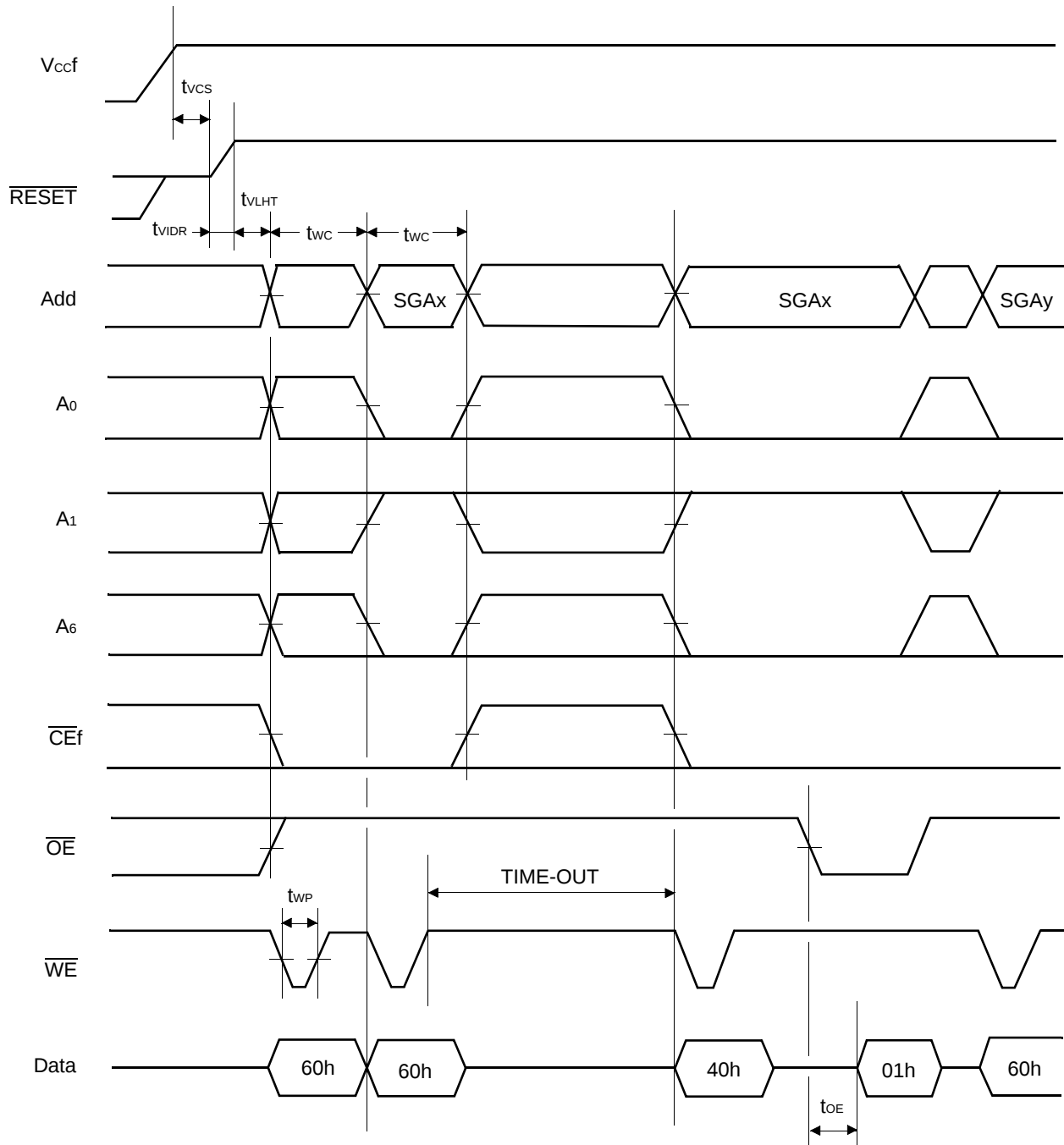


# MB84VF5F4F4J1-70

## • Temporary Sector Unprotection (Flash)



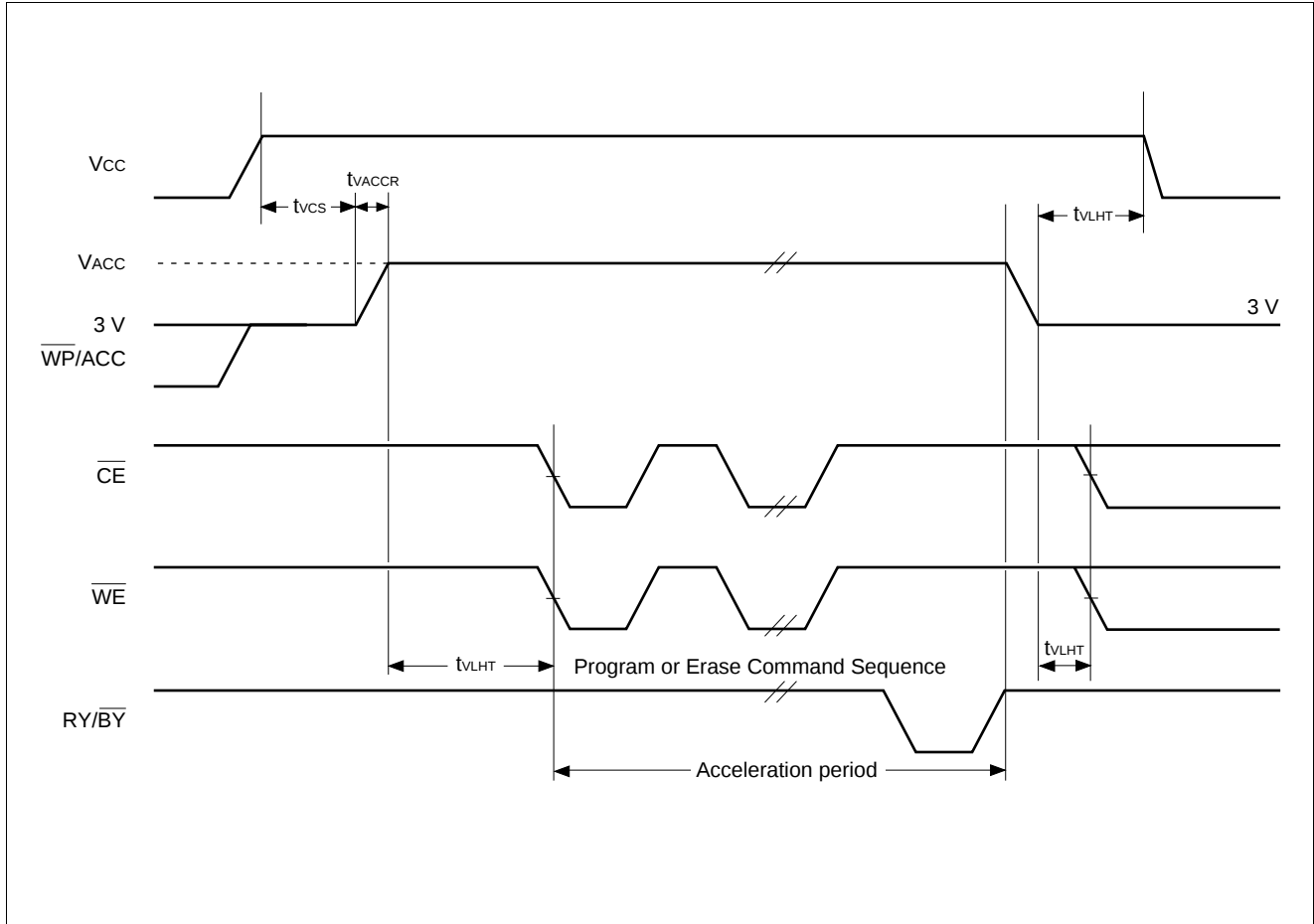
## • Extended Sector Group Protection (Flash)



SGAx : Sector Group Address to be protected  
 SGAy : Next Group Sector Address to be protected  
 TIME-OUT : Time-Out window = 250  $\mu$ s (Min)

# MB84VF5F4F4J1-70

- **Accelerated Program (Flash)**



## 3. Erase and Programming Performance

| Parameter             | Limits  |     |     | Unit  | Comments                                   |
|-----------------------|---------|-----|-----|-------|--------------------------------------------|
|                       | Min     | Typ | Max |       |                                            |
| Sector Erase Time     | —       | 0.5 | 2.0 | s     | Excludes programming time prior to erasure |
| Word Programming Time | —       | 6.0 | 100 | μs    | Excludes system-level overhead             |
| Chip Programming Time | —       | —   | 100 | s     | Excludes system-level overhead             |
| Program/Erase Cycle   | 100,000 | —   | —   | cycle | —                                          |

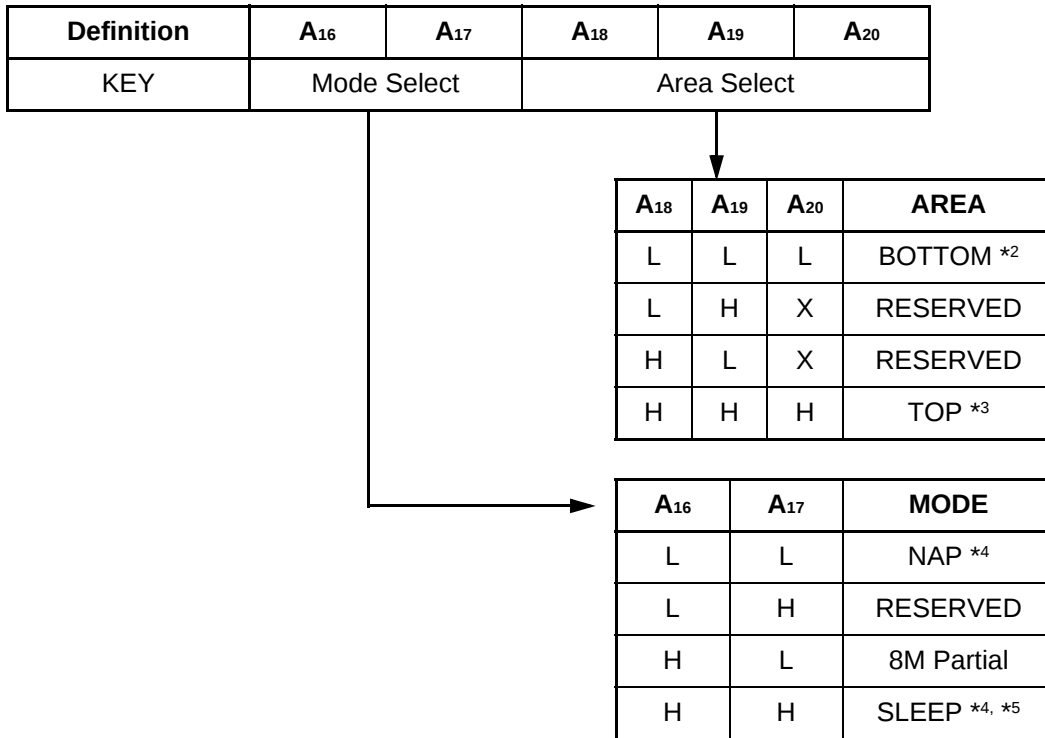
Notes: • Typical erase conditions  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.9\text{ V}$   
 • Typical program conditions  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 2.9\text{ V}$ , Data = Checker

# MB84VF5F4F4J1-70

## ■ 32M FCRAM CHARACTERISTICS for MCP

### 1. FCRAM Power Down Program Key Table

Basic Key Table



Available Key Table

| MODE       | A <sub>16</sub> | A <sub>17</sub> | A <sub>18</sub> | A <sub>19</sub> | A <sub>20</sub> | Data Retention Area |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------------------|
|            | Mode Select     |                 | Area Select     |                 |                 |                     |
| NAP        | L               | L               | X               | X               | X               | None                |
| 8M Partial | H               | L               | L               | L               | L               | Bottom 8M only      |
|            | H               | L               | H               | H               | H               | Top 8M only         |
| SLEEP      | H               | H               | X               | X               | X               | None                |

\*1: The Power Down Program can be performed one time after compliance of Power-up timings and it should not be re-programmed after regular Read or Write.

Unspecified addresses, A<sub>15</sub> to A<sub>0</sub>, can be either High or Low during the programming.

The RESERVED key should not be used.

\*2: BOTTOM area is from the lowest address location. (i.e., A<sub>20</sub> to A<sub>0</sub> = L)

\*3: TOP area is from the highest address location. (i.e., A<sub>20</sub> to A<sub>0</sub> = H)

\*4: NAP and SLEEP do not retain the data and Area Select is ignored.

\*5: Default state. Power Down Program to this SLEEP mode can be omitted.

## 2. AC Characteristics (FCRAM)

### • READ OPERATION (FCRAM)

| Parameter                                                             | Symbol         | Value |      | Unit | Remarks      |
|-----------------------------------------------------------------------|----------------|-------|------|------|--------------|
|                                                                       |                | Min   | Max  |      |              |
| Read Cycle Time                                                       | $t_{RC}$       | 70    | —    | ns   |              |
| Chip Enable Access Time                                               | $t_{CE}$       | —     | 65   | ns   | *1,*3        |
| Output Enable Access Time                                             | $t_{OE}$       | —     | 40   | ns   | *1           |
| Address Access Time                                                   | $t_{AA}$       | —     | 65   | ns   | *1,*4        |
| Output Data Hold Time                                                 | $t_{OH}$       | 5     | —    | ns   | *1           |
| $\overline{CE1r}$ Low to Output Low-Z                                 | $t_{CLZ}$      | 5     | —    | ns   | *2           |
| $\overline{OE}$ Low to Output Low-Z                                   | $t_{OLZ}$      | 0     | —    | ns   | *2           |
| $\overline{CE1r}$ High to Output High-Z                               | $t_{CHZ}$      | —     | 20   | ns   | *2           |
| $\overline{OE}$ High to Output High-Z                                 | $t_{OHZ}$      | —     | 20   | ns   | *2           |
| Address Setup Time to $\overline{CE1r}$ Low                           | $t_{ASC}$      | −5    | —    | ns   | *5           |
| Address Setup Time to $\overline{OE}$                                 | $t_{ASO}$      | 25    | —    | ns   | *3,*6        |
|                                                                       | $t_{ASO(ABS)}$ | 10    | —    | ns   | *7           |
| $\overline{LB} / \overline{UB}$ Setup Time to $\overline{CE1r}$ Low   | $t_{BSC}$      | −5    | —    | ns   | *5           |
| $\overline{LB} / \overline{UB}$ Setup Time to $\overline{OE}$ Low     | $t_{BSO}$      | 10    | —    | ns   |              |
| Address Invalid Time                                                  | $t_{AX}$       | —     | 5    | ns   | *4,*8        |
| Address Hold Time from $\overline{CE1r}$ Low                          | $t_{CLAH}$     | 70    | —    | ns   | *4           |
| Address Hold Time from $\overline{OE}$ Low                            | $t_{OLAH}$     | 45    | —    | ns   | *4,*9        |
| Address Hold Time from $\overline{CE1r}$ High                         | $t_{CHAH}$     | −5    | —    | ns   |              |
| Address Hold Time from $\overline{OE}$ High                           | $t_{OH AH}$    | −5    | —    | ns   |              |
| $\overline{LB} / \overline{UB}$ Hold Time from $\overline{CE1r}$ High | $t_{CHBH}$     | −5    | —    | ns   |              |
| $\overline{LB} / \overline{UB}$ Hold Time from $\overline{OE}$ High   | $t_{OH BH}$    | −5    | —    | ns   |              |
| $\overline{CE1r}$ Low to $\overline{OE}$ Low Delay Time               | $t_{CLOL}$     | 25    | 1000 | ns   | *3,*6,*9,*10 |
| $\overline{OE}$ Low to $\overline{CE1r}$ High Delay Time              | $t_{OLCH}$     | 45    | —    | ns   | *9           |
| $\overline{CE1r}$ High Pulse Width                                    | $t_{CP}$       | 12    | —    | ns   |              |
| $\overline{OE}$ High Pulse Width                                      | $t_{OP}$       | 25    | 1000 | ns   | *6,*9,*10    |
|                                                                       | $t_{OP(ABS)}$  | 12    | —    | ns   | *7           |

(Continued)

(Continued)

- \*1 : The output load is 30 pF.
- \*2 : The output load is 5 pF.
- \*3 : The  $t_{CE}$  is applicable if  $\overline{OE}$  is brought to Low before  $\overline{CE1r}$  goes Low and is also applicable if actual value of both or either  $t_{ASO}$  or  $t_{CLOL}$  is shorter than specified value.
- \*4 : Applicable only to  $A_1$  and  $A_0$  when both  $\overline{CE1r}$  and  $\overline{OE}$  are kept at Low for the address access.
- \*5 : Applicable if  $\overline{OE}$  is brought to Low before  $\overline{CE1r}$  goes Low.
- \*6 : The  $t_{ASO}$ ,  $t_{CLOL(Min)}$  and  $t_{OP(Min)}$  are reference values when the access time is determined by  $t_{OE}$ .  
If actual value of each parameter is shorter than specified minimum value,  $t_{OE}$  become longer by the amount of subtracting actual value from specified minimum value.  
For example, if actual  $t_{ASO}$ ,  $t_{ASO(actual)}$ , is shorter than specified minimum value,  $t_{ASO(Min)}$ , during  $\overline{OE}$  control access (i.e.,  $\overline{CE1r}$  stays Low), the  $t_{OE}$  become  $t_{OE(Max)} + t_{ASO(Min)} - t_{ASO(actual)}$ .
- \*7 : The  $t_{ASO(ABS)}$  and  $t_{OP(ABS)}$  is the absolute minimum value during  $\overline{OE}$  control access.
- \*8 : The  $t_{AX}$  is applicable when both  $A_1$  and  $A_0$  are switched from previous state.
- \*9 : If actual value of either  $t_{CLOL}$  or  $t_{OP}$  is shorter than specified minimum value, both  $t_{OLAH}$  and  $t_{OLCH}$  become  $t_{RC(Min)} - t_{CLOL(actual)}$  OR  $t_{RC(Min)} - t_{OP(actual)}$ .
- \*10 : Maximum value is applicable if  $\overline{CE1r}$  is kept at Low.

## • WRITE OPERATION (FCRAM)

| Parameter                                                | Symbol         | Value |      | Unit | Remarks    |
|----------------------------------------------------------|----------------|-------|------|------|------------|
|                                                          |                | Min   | Max  |      |            |
| Write Cycle Time                                         | $t_{WC}$       | 70    | —    | ns   | *1         |
| Address Setup Time                                       | $t_{AS}$       | 0     | —    | ns   | *2         |
| Address Hold Time                                        | $t_{AH}$       | 35    | —    | ns   | *2         |
| $\overline{CE1r}$ Write Setup Time                       | $t_{CS}$       | 0     | 1000 | ns   |            |
| $\overline{CE1r}$ Write Hold Time                        | $t_{CH}$       | 0     | 1000 | ns   |            |
| $\overline{WE}$ Setup Time                               | $t_{WS}$       | 0     | —    | ns   |            |
| $\overline{WE}$ Hold Time                                | $t_{WH}$       | 0     | —    | ns   |            |
| $\overline{LB}$ and $\overline{UB}$ Setup Time           | $t_{BS}$       | −5    | —    | ns   |            |
| $\overline{LB}$ and $\overline{UB}$ Hold Time            | $t_{BH}$       | −5    | —    | ns   |            |
| $\overline{OE}$ Setup Time                               | $t_{OES}$      | 0     | 1000 | ns   | *3         |
| $\overline{OE}$ Hold Time                                | $t_{OEh}$      | 25    | 1000 | ns   | *3, *4     |
|                                                          | $t_{OEh(ABS)}$ | 12    | —    | ns   | *5         |
| $\overline{OE}$ High to $\overline{CE1r}$ Low Setup Time | $t_{OHCL}$     | −5    | —    | ns   | *6         |
| $\overline{OE}$ High to Address Hold Time                | $t_{OHAH}$     | −5    | —    | ns   | *7         |
| $\overline{CE1r}$ Write Pulse Width                      | $t_{CW}$       | 45    | —    | ns   | *1, *8     |
| $\overline{WE}$ Write Pulse Width                        | $t_{WP}$       | 45    | —    | ns   | *1, *8     |
| $\overline{CE1r}$ Write Recovery Time                    | $t_{WRC}$      | 10    | —    | ns   | *1, *9     |
| $\overline{WE}$ Write Recovery Time                      | $t_{WR}$       | 10    | 1000 | ns   | *1, *3, *9 |
| Data Setup Time                                          | $t_{DS}$       | 15    | —    | ns   |            |
| Data Hold Time                                           | $t_{DH}$       | 0     | —    | ns   |            |
| $\overline{CE1r}$ High Pulse Width                       | $t_{CP}$       | 12    | —    | ns   | *9         |

\*1 : Minimum value must be equal or greater then the sum of actual  $t_{CW}$  (or  $t_{WP}$ ) and  $t_{WRC}$  (or  $t_{WR}$ ).

\*2 : New write address is valid from either  $\overline{CE1r}$  or  $\overline{WE}$  is brought to High.

\*3 : The  $t_{OEh}$  is specified from end of  $t_{WC(Min)}$ . The  $t_{OEh(Min)}$  is a reference value when the access time is determined by  $t_{OE}$ .  
If actual value,  $t_{OEh(actual)}$  is shorter than specified minimum value,  $t_{OE}$  become longer by the amount of subtracting actual value from specified minimum value.

\*4 : The  $t_{OEh(Max)}$  is applicable if  $\overline{CE1r}$  is kept at Low and both  $\overline{WE}$  and  $\overline{OE}$  are kept at High.

\*5 : The  $t_{OEh(ABS)}$  is the absolute minimum value if write cycle is terminated by  $\overline{WE}$  and  $\overline{CE1r}$  stays Low.

\*6 :  $t_{OHCL(Min)}$  must be satisfied if read operation is not performed prior to write operation.  
In case  $\overline{OE}$  is disabled after  $t_{OHCL(Min)}$ ,  $\overline{WE}$  Low must be asserted after  $t_{RC(Min)}$  from  $\overline{CE1r}$  Low.  
In other words, read operation is initiated if  $t_{OHCL(Min)}$  is not satisfied.

\*7 : Applicable if  $\overline{CE1r}$  stays Low after read operation.

\*8 :  $t_{CW}$  and  $t_{WP}$  is applicable if write operation is initiated by  $\overline{CE1r}$  and  $\overline{WE}$ , respectively.

\*9 :  $t_{WRC}$  and  $t_{WR}$  is applicable if write operation is terminated by  $\overline{CE1r}$  and  $\overline{WE}$ , respectively.  
The  $t_{WR(Min)}$  can be ignored if  $\overline{CE1r}$  is brought to High together or after  $\overline{WE}$  is brought to High.  
In such case, the  $t_{CP(Min)}$  must be satisfied.

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## • POWER DOWN and POWER DOWN PROGRAM PARAMETERS (FCRAM)

| Parameter                                                                                                  | Symbol            | Value |     | Unit | Remarks |
|------------------------------------------------------------------------------------------------------------|-------------------|-------|-----|------|---------|
|                                                                                                            |                   | Min   | Max |      |         |
| CE2r Low Setup Time for Power Down Entry                                                                   | t <sub>CSP</sub>  | 10    | —   | ns   |         |
| CE2r Low Hold Time after Power Down Entry                                                                  | t <sub>C2LP</sub> | 70    | —   | ns   |         |
| $\overline{\text{CE1r}}$ High Hold Time following CE2r High after Power Down Exit (SLEEP mode only)        | t <sub>CHH</sub>  | 350   | —   | μs   |         |
| $\overline{\text{CE1r}}$ High Setup Time following CE2r High after Power Down Exit (Except for SLEEP mode) | t <sub>CHHN</sub> | 1     | —   | μs   |         |
| $\overline{\text{CE1r}}$ High Setup Time following CE2r High after Power Down Exit                         | t <sub>CHS</sub>  | 10    | —   | ns   |         |
| $\overline{\text{CE1r}}$ High to $\overline{\text{PE}}$ Low Setup Time                                     | t <sub>EPS</sub>  | 70    | —   | ns   | *       |
| $\overline{\text{PE}}$ Power Down Program Pulse Width                                                      | t <sub>EP</sub>   | 70    | —   | ns   | *       |
| $\overline{\text{PE}}$ High to $\overline{\text{CE1r}}$ Low Hold Time                                      | t <sub>EPH</sub>  | 70    | —   | ns   | *       |
| Address Setup Time to $\overline{\text{PE}}$ High                                                          | t <sub>EAS</sub>  | 15    | —   | ns   | *       |
| Address Setup Time from $\overline{\text{PE}}$ High                                                        | t <sub>EAH</sub>  | 0     | —   | ns   | *       |

\*: Applicable to Power Down Program.

## • OTHER TIMING PARAMETERS (FCRAM)

| Parameter                                                                              | Symbol            | Value |     | Unit | Remarks |
|----------------------------------------------------------------------------------------|-------------------|-------|-----|------|---------|
|                                                                                        |                   | Min   | Max |      |         |
| $\overline{\text{CE1r}}$ High to $\overline{\text{OE}}$ Invalid Time for Standby Entry | t <sub>CHOX</sub> | 10    | —   | ns   |         |
| $\overline{\text{CE1r}}$ High to $\overline{\text{WE}}$ Invalid Time for Standby Entry | t <sub>CHWX</sub> | 10    | —   | ns   | *1      |
| CE2r Low Hold Time after Power-up                                                      | t <sub>C2LH</sub> | 50    | —   | μs   | *2      |
| CE2r High Hold Time after Power-up                                                     | t <sub>C2HL</sub> | 50    | —   | μs   | *3      |
| $\overline{\text{CE1r}}$ High Hold Time following CE2r High after Power-up             | t <sub>CHH</sub>  | 350   | —   | μs   | *2      |
| Input Transition Time                                                                  | t <sub>tr</sub>   | 1     | 25  | ns   | *4      |

\*1: It may write some data into any address location if t<sub>CHWX</sub> is not satisfied.

\*2: Must satisfy t<sub>CHH(Min)</sub> after t<sub>C2LH(Min)</sub>.

\*3: Requires Power Down mode entry and exit after t<sub>C2HL</sub>.

\*4: The input Transition Time (t<sub>tr</sub>) at AC testing is 5 ns as shown in below. If actual t<sub>tr</sub> is longer than 5ns, it may violate AC specification of some timing parameters.

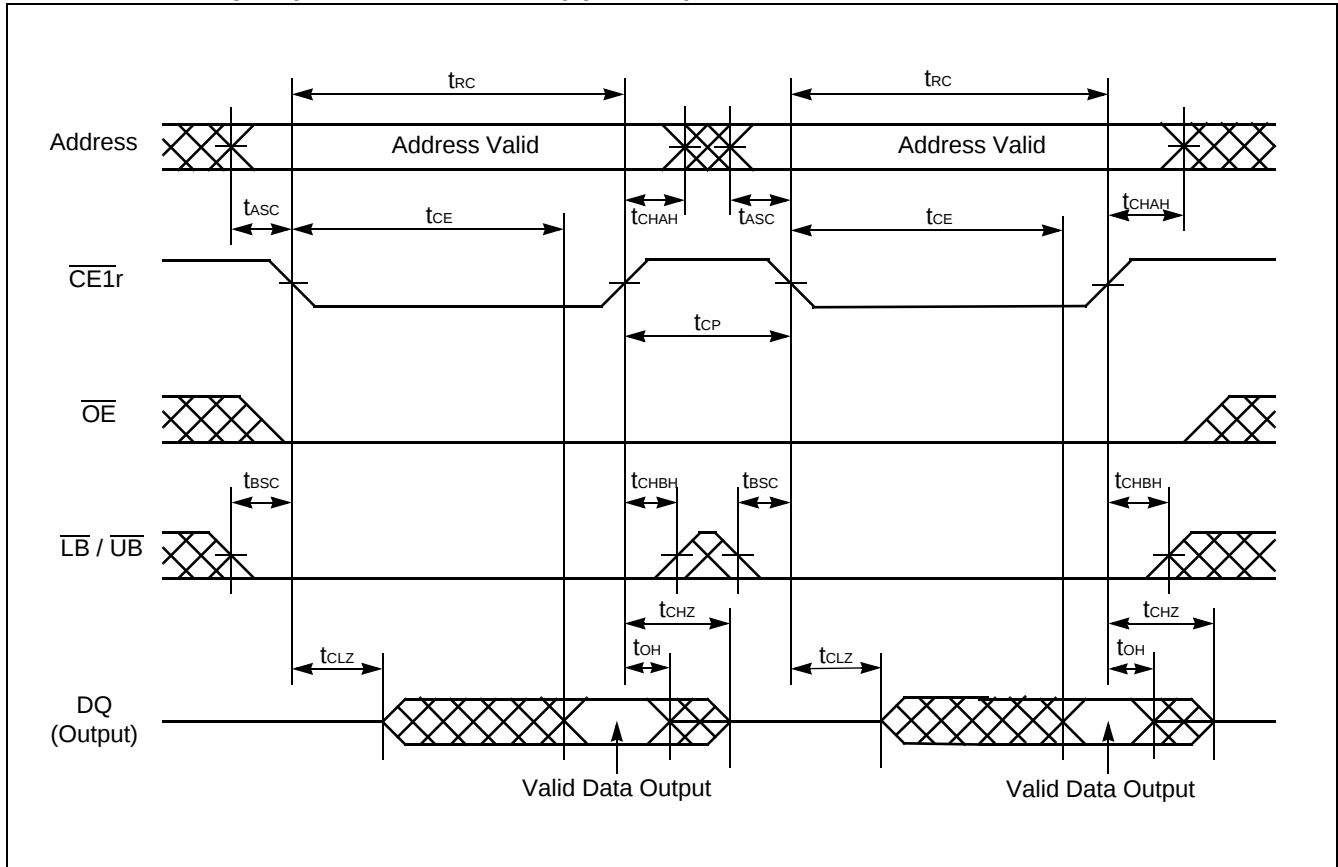
## • AC TEST CONDITIONS (FCRAM)

| Description                    | Symbol           | Test Setup                                  | Value | Unit | Remarks |
|--------------------------------|------------------|---------------------------------------------|-------|------|---------|
| Input High Level               | V <sub>IH</sub>  | V <sub>CCr</sub> = 2.7 V to 3.1 V           | 2.3   | V    |         |
| Input Low Level                | V <sub>IL</sub>  | V <sub>CCr</sub> = 2.7 V to 3.1 V           | 0.4   | V    |         |
| Input Timing Measurement Level | V <sub>REF</sub> | V <sub>CCr</sub> = 2.7 V to 3.1 V           | 1.3   | V    |         |
| Input Transition Time          | t <sub>tr</sub>  | Between V <sub>IL</sub> and V <sub>IH</sub> | 5     | ns   |         |



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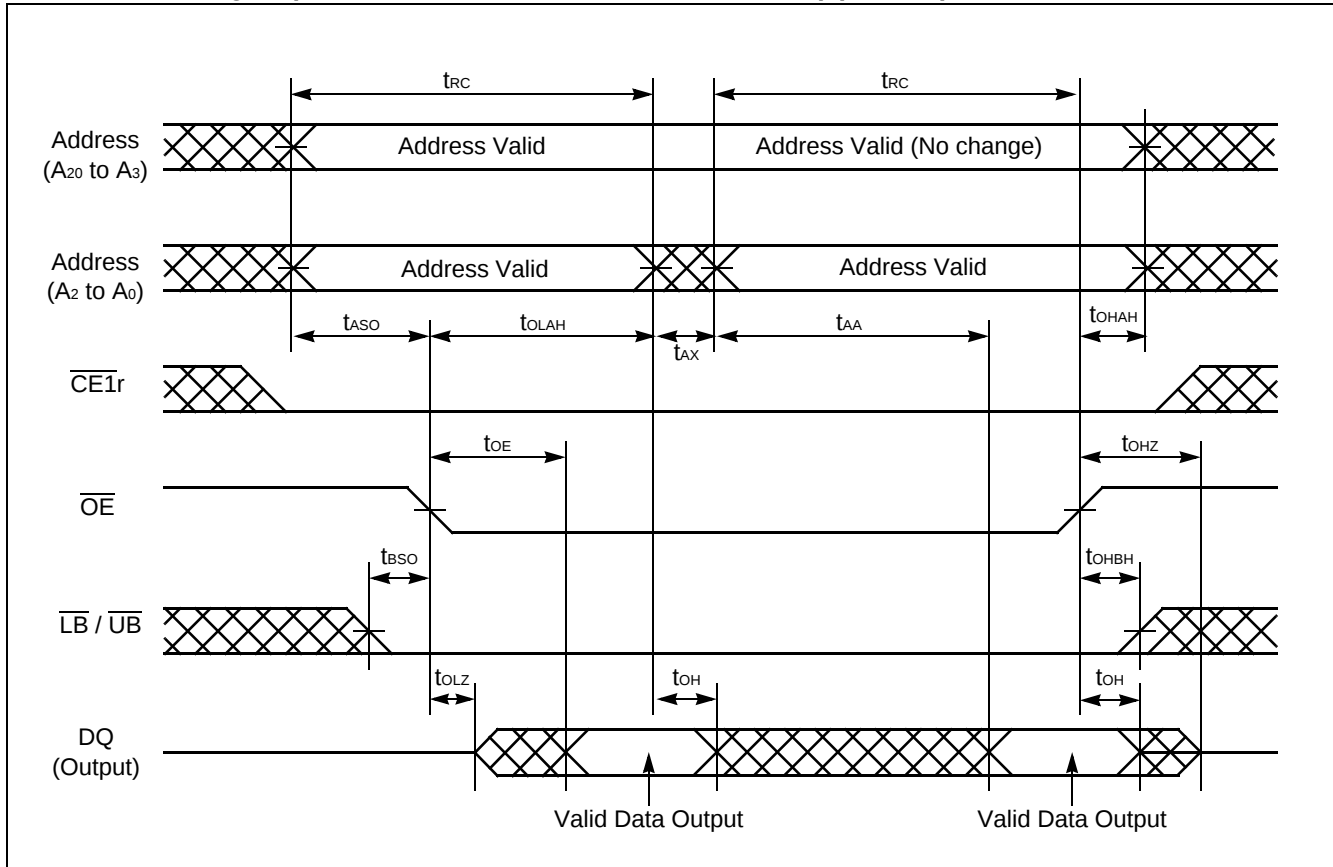
## • READ Timing #2 ( $\overline{\text{CE1r}}$ Control Access) (FCRAM)



Note :  $\text{CE2r}$ ,  $\overline{\text{PE}}$  and  $\overline{\text{WE}}$  must be High for entire read cycle.

Either or both  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  must be Low when both  $\overline{\text{CE1r}}$  and  $\overline{\text{OE}}$  are Low.

- **READ Timing #3 (Address Access after  $\overline{\text{OE}}$  Control Access) (FCRAM)**

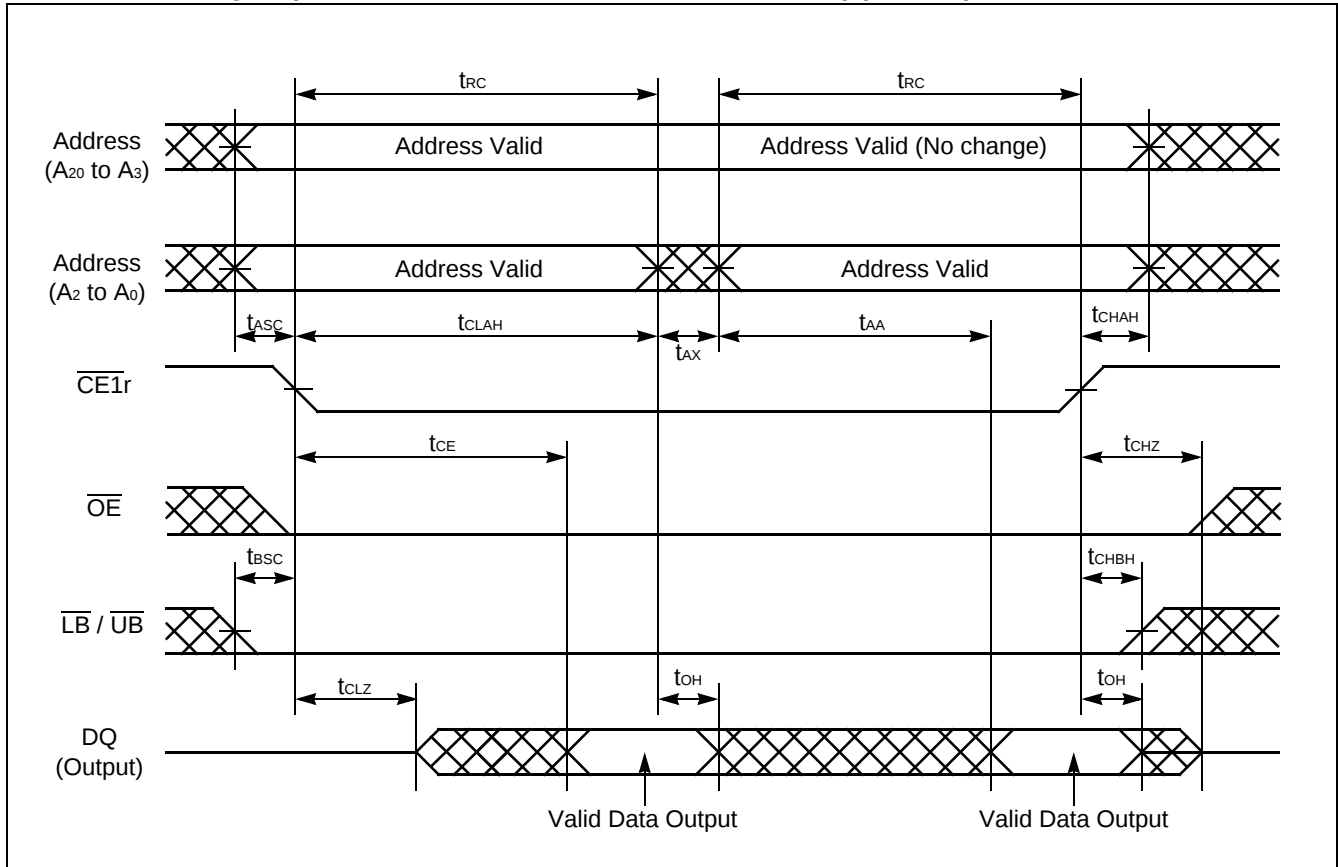


Note :  $\overline{\text{CE2r}}$ ,  $\overline{\text{PE}}$  and  $\overline{\text{WE}}$  must be High for entire read cycle.

Either or both  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  must be Low when both  $\overline{\text{CE1r}}$  and  $\overline{\text{OE}}$  are Low.

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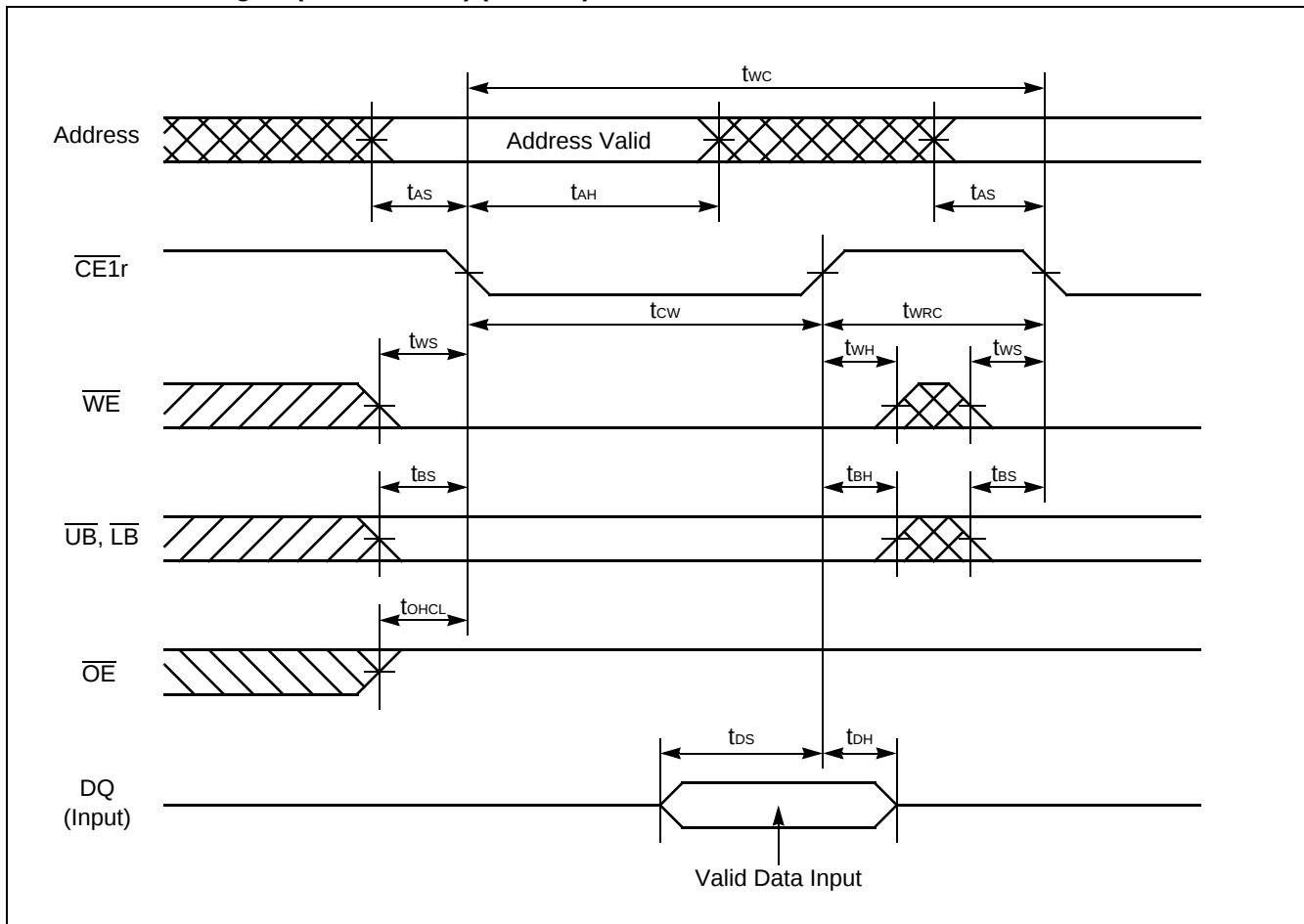
- **READ Timing #4 (Address Access after  $\overline{\text{CE1r}}$  Control Access) (FCRAM)**



Note :  $\overline{\text{CE2r}}$ ,  $\overline{\text{PE}}$  and  $\overline{\text{WE}}$  must be High for entire read cycle.

Either or both  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  must be Low when both  $\overline{\text{CE1r}}$  and  $\overline{\text{OE}}$  are Low.

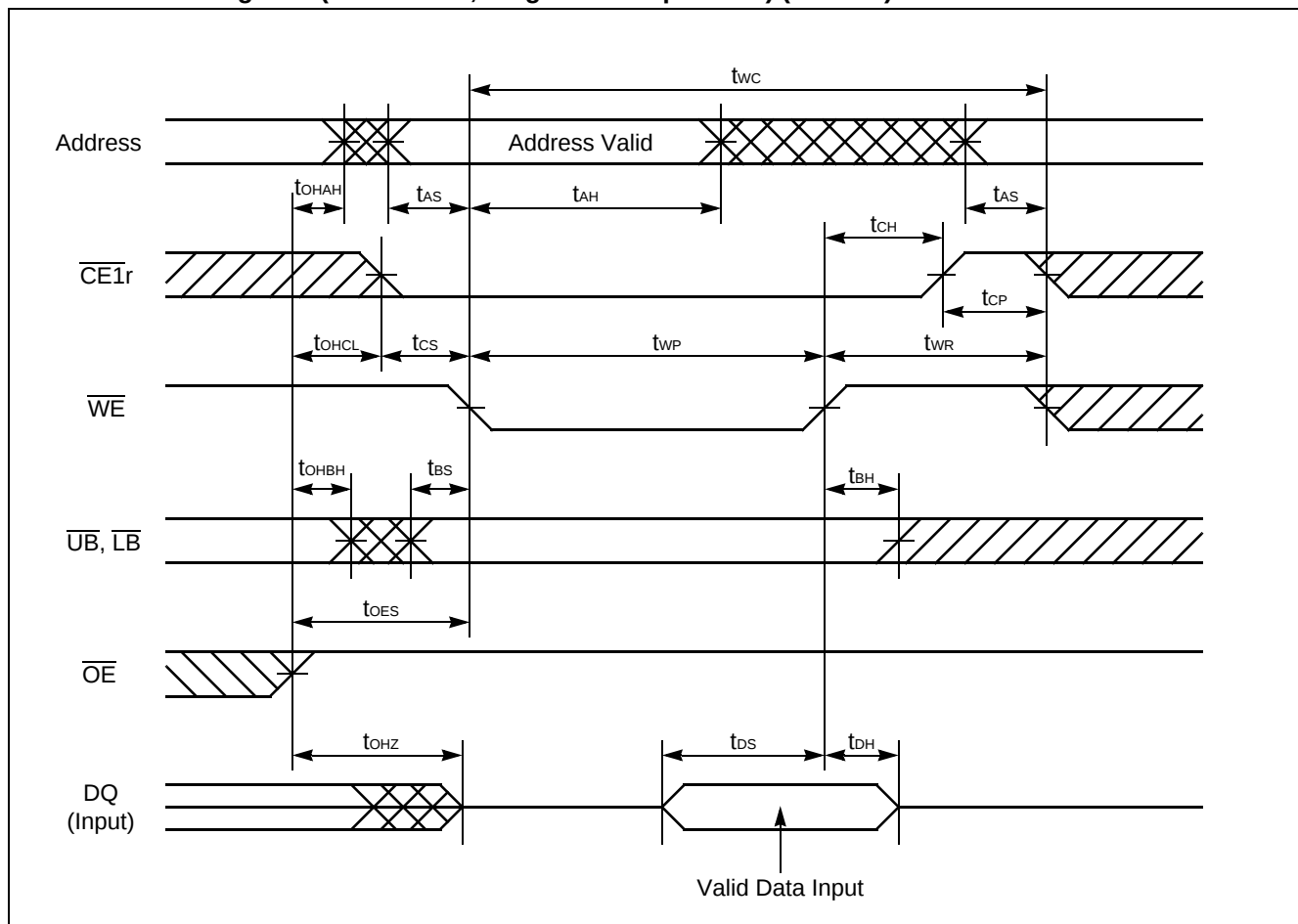
- WRITE Timing #1 ( $\overline{\text{CE1r}}$  Control) (FCRAM)



Note :  $\overline{\text{CE2r}}$  and  $\overline{\text{PE}}$  must be High for write cycle.

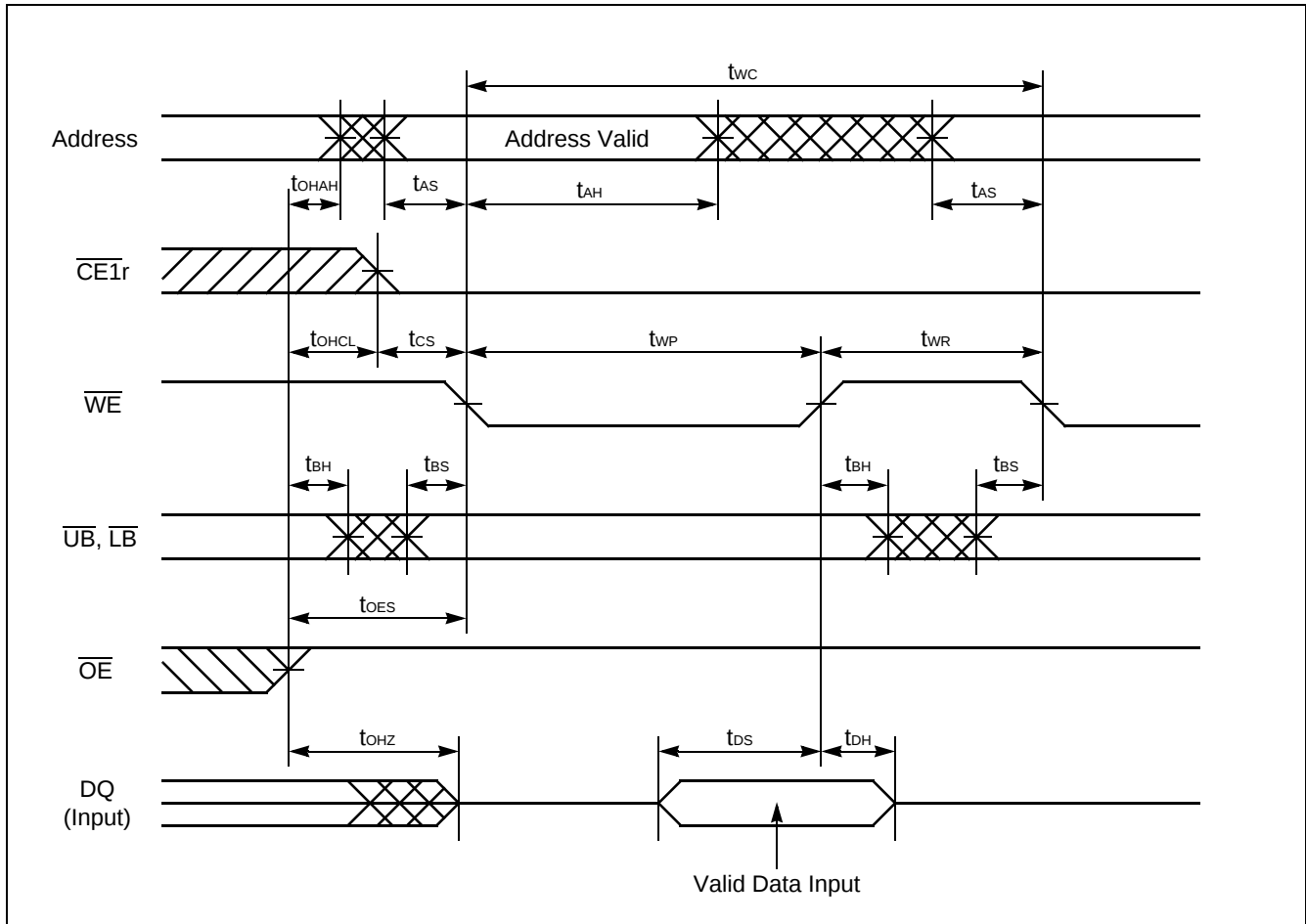
# MB84VF5F4J1-70

- WRITE Timing #2-1 ( $\overline{\text{WE}}$  Control, Single Write Operation) (FCRAM)



Note :  $\overline{\text{CE2r}}$  and  $\overline{\text{PE}}$  must be High for write cycle.

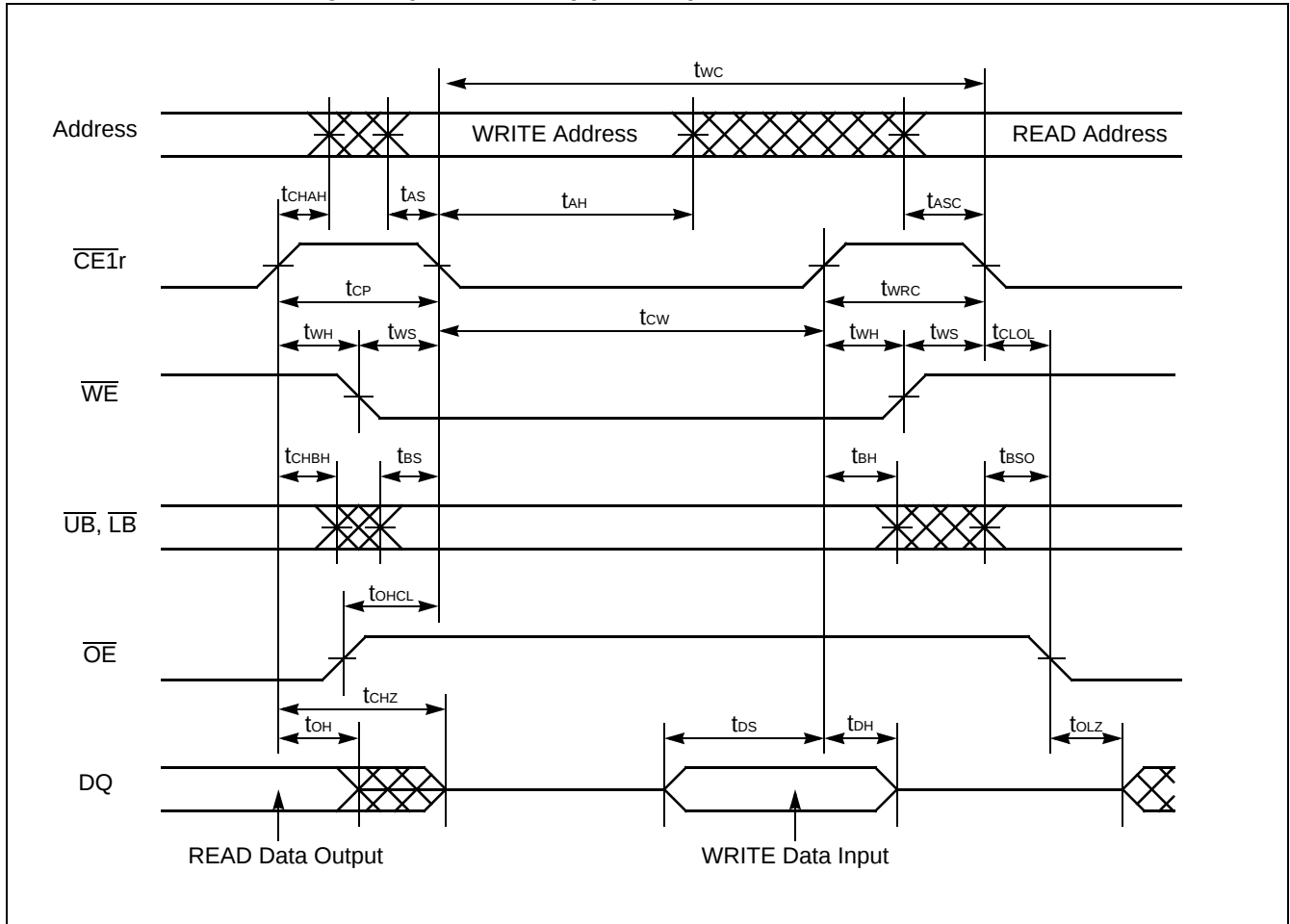
• WRITE Timing #2-2 ( $\overline{\text{WE}}$  Control, Continuous Write Operation) (FCRAM)



Note :  $\overline{\text{CE2r}}$  and  $\overline{\text{PE}}$  must be High for write cycle.

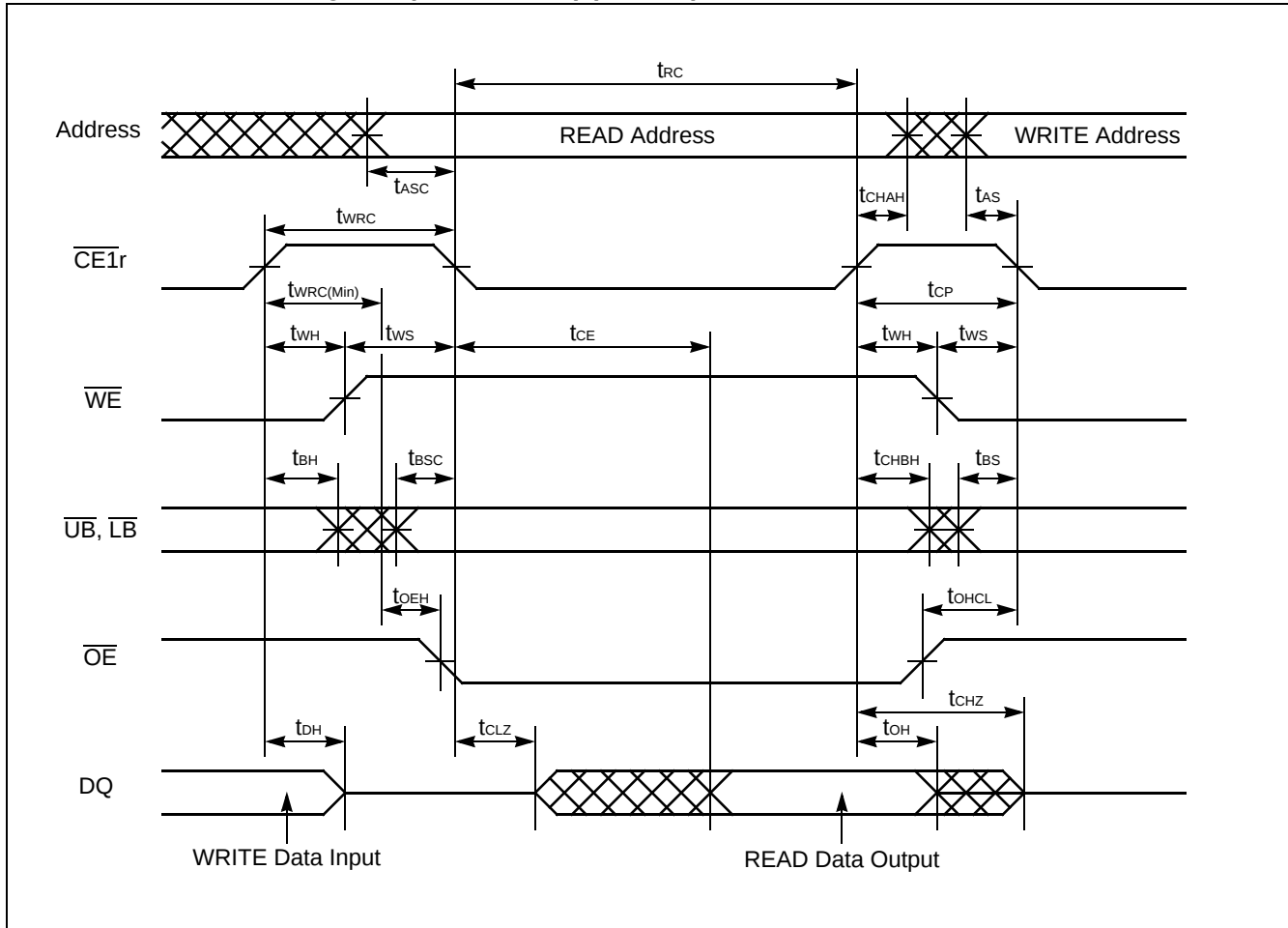
# MB84VF5F4J1-70

## • READ / WRITE Timing #1-1 ( $\overline{\text{CE1r}}$ Control) (FCRAM)



Note : Write address is valid from either  $\overline{\text{CE1r}}$  or  $\overline{\text{WE}}$  of last falling edge.

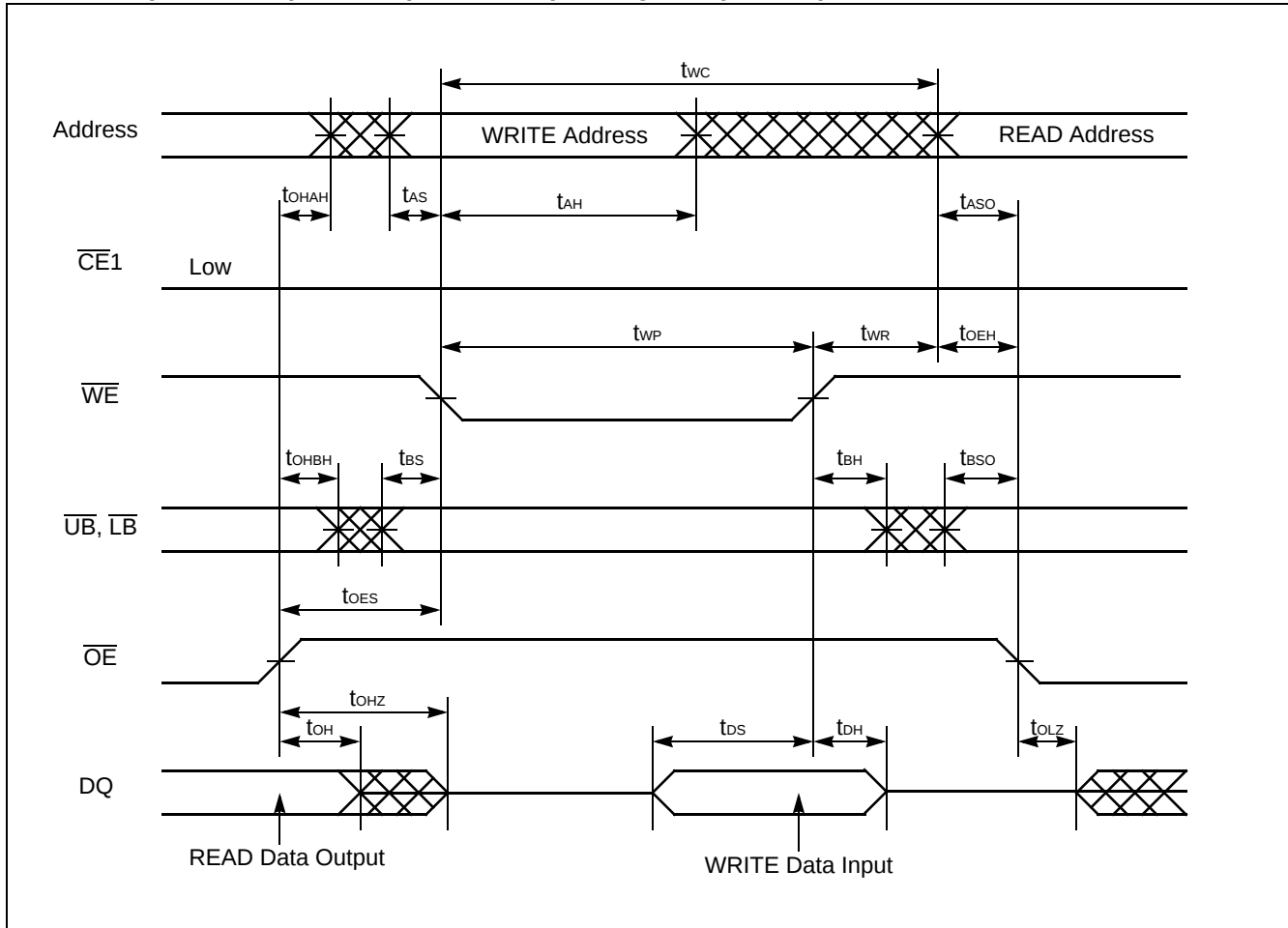
## • READ / WRITE Timing #1-2 ( $\overline{\text{CE1r}}$ Control) (FCRAM)



Note : The  $t_{\text{OEH}}$  is specified from the time satisfied both  $t_{\text{WRC}}$  and  $t_{\text{WRC(Min)}}$ .

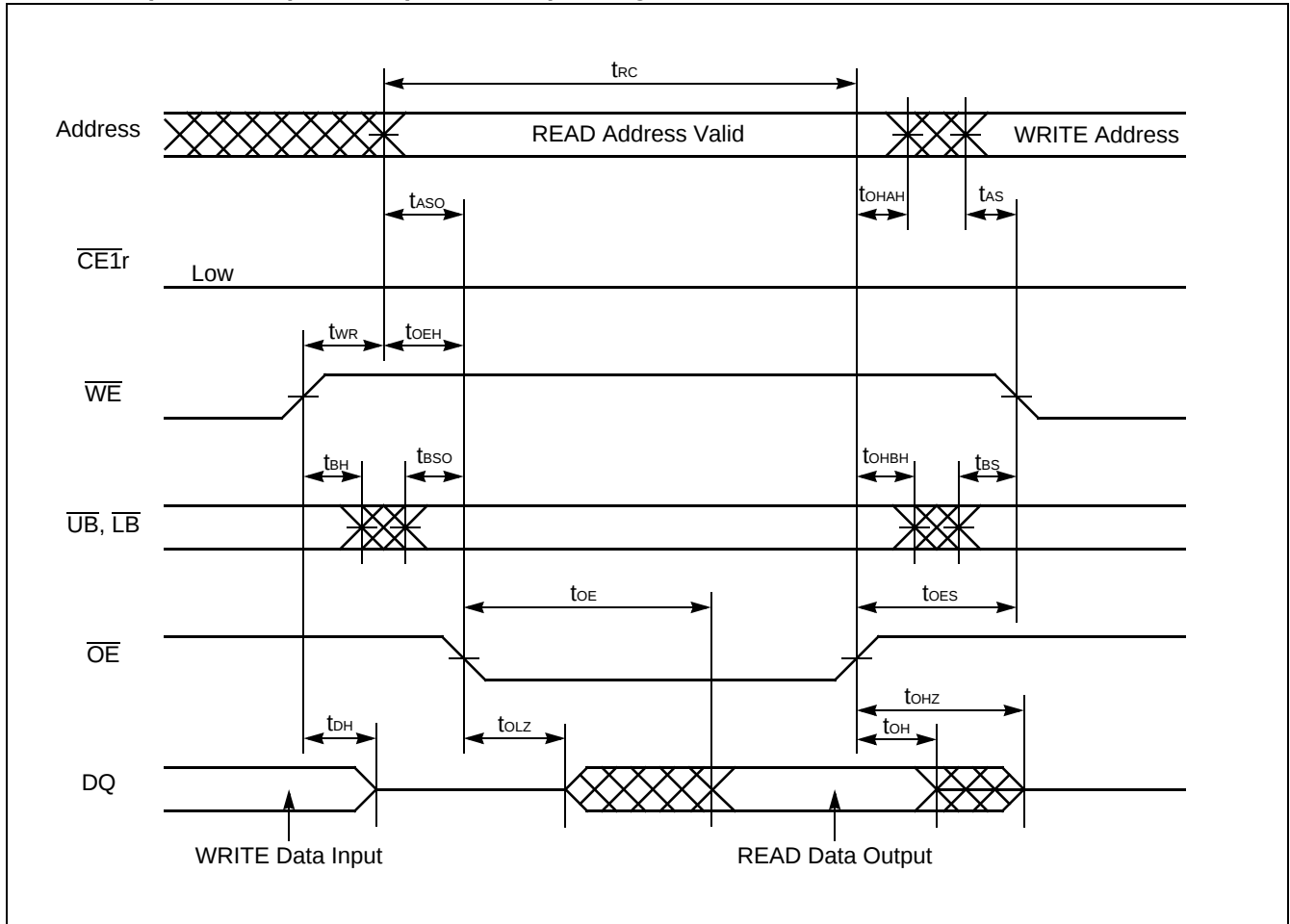
# MB84VF5F4J1-70

## • READ( $\overline{\text{OE}}$ Control) / WRITE( $\overline{\text{WE}}$ Control) Timing #2-1 (FCRAM)



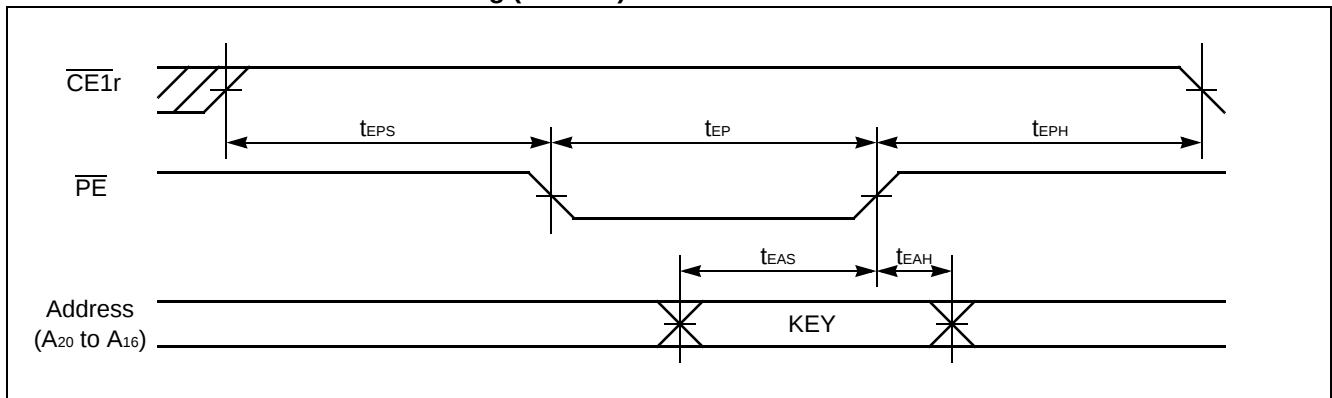
Note :  $\overline{\text{CE1r}}$  can be tied to Low for  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$  controlled operation.  
When  $\overline{\text{CE1r}}$  is tied to Low, output is exclusively controlled by  $\overline{\text{OE}}$ .

## • READ( $\overline{\text{OE}}$ Control) / WRITE( $\overline{\text{WE}}$ Control) Timing #2-2



Note :  $\overline{\text{CE1r}}$  can be tied to Low for  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$  controlled operation.  
When  $\overline{\text{CE1r}}$  is tied to Low, output is exclusively controlled by  $\overline{\text{OE}}$ .

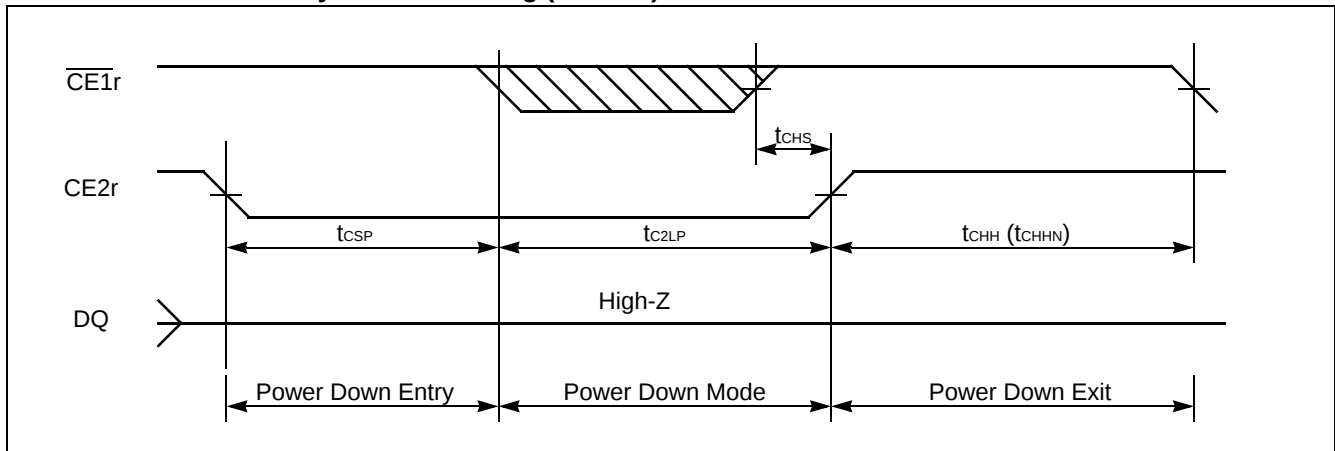
## • POWER DOWN PROGRAM Timing (FCRAM)



Note:  $\overline{\text{CE2r}}$  must be High for Power Down Programming.  
Any other inputs not specified above can be either High or Low.

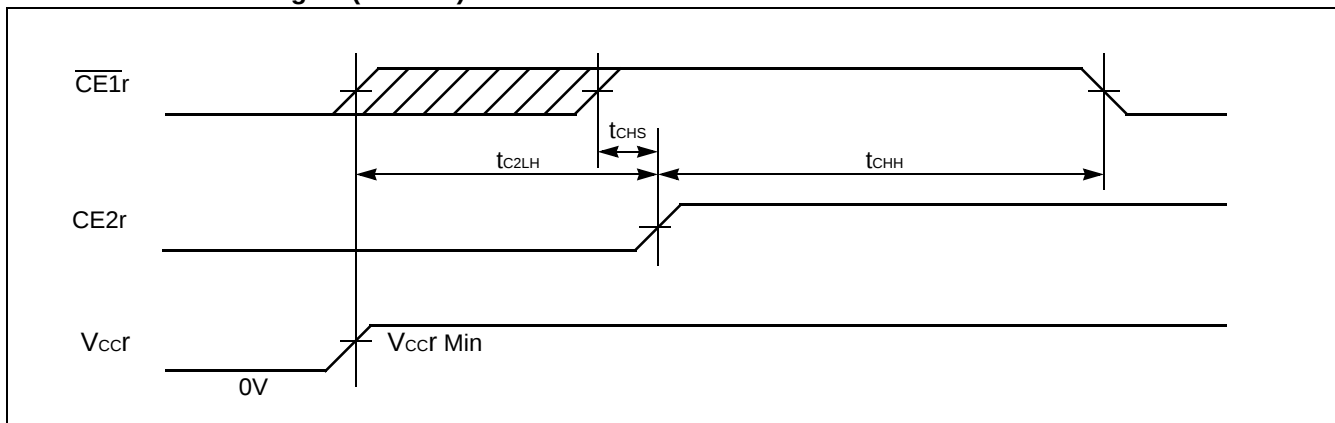
# MB84VF5F4F4J1-70

## • POWER DOWN Entry and Exit Timing (FCRAM)



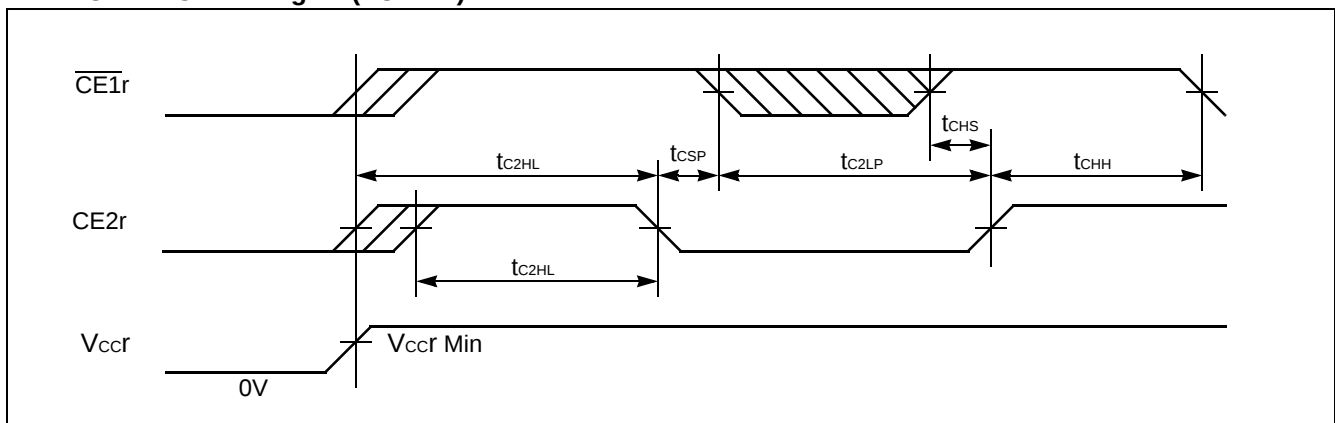
Note: This Power Down mode can be also used for Power-up #2 below except that  $t_{CHHN}$  can not be used at Power-up timing.

## • POWER-UP Timing #1 (FCRAM)



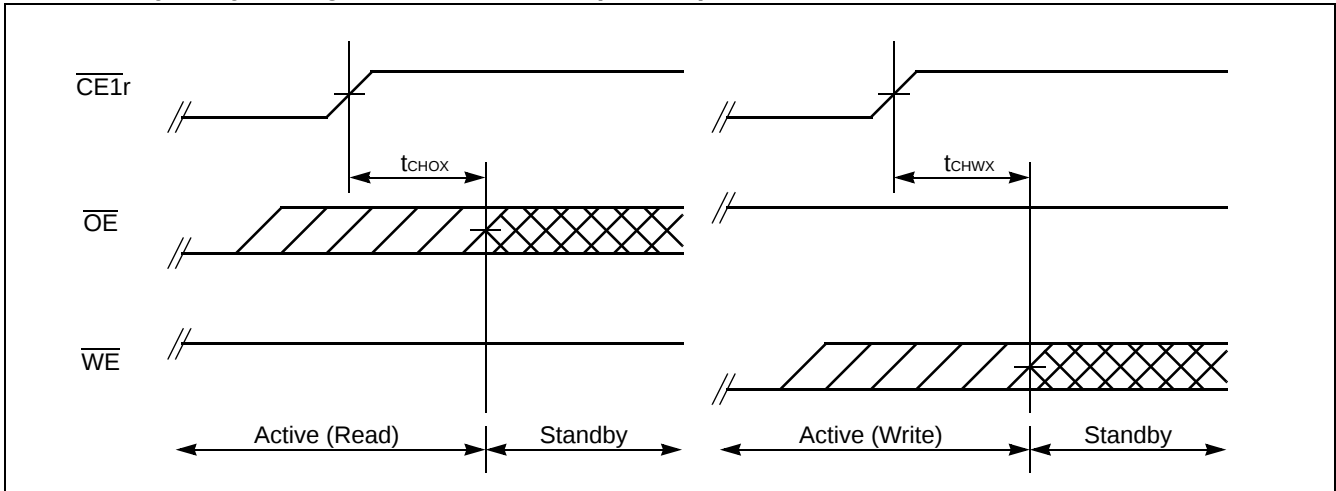
Note: The  $t_{C2LH}$  specifies after  $V_{CCr}$  reaches specified minimum level.

## • POWER-UP Timing #2 (FCRAM)



Note: The  $t_{C2HL}$  specifies from  $CE2r$  Low to High transition after  $V_{CCr}$  reaches specified minimum level.  $\overline{CE1r}$  must be brought to High prior to or together with  $CE2r$  Low to High transition.

## • Standby Entry Timing after Read or Write (FCRAM)



Note : Both  $t_{CHOX}$  and  $t_{CHWX}$  define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes  $t_{RC (Min)}$  period from either last address transition of  $A_1$  and  $A_0$ , or  $\overline{CE1r}$  Low to High transition.

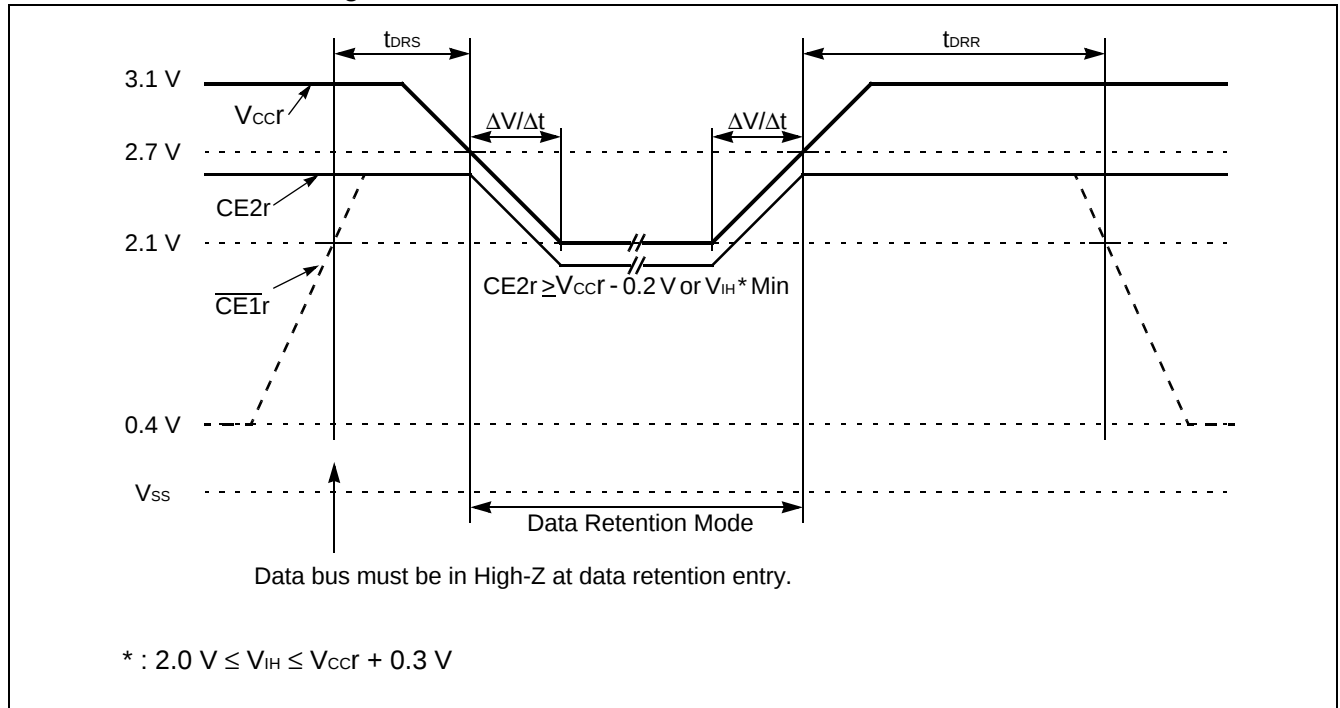
# MB84VF5F4F4J1-70

## 3. Data Retention Low $V_{CCr}$ Characteristics (FCRAM)

| Parameter                               | Symbol              | Test Conditions                                                                                                                                                                                                 | Value |     | Unit             |
|-----------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|------------------|
|                                         |                     |                                                                                                                                                                                                                 | Min   | Max |                  |
| $V_{CCr}$ Data Retention Supply Voltage | $V_{DR}$            | $\overline{CE1r} = CE2r \geq V_{CCr} - 0.2 \text{ V}$ or,<br>$\overline{CE1r} = CE2r = V_{IH}$                                                                                                                  | 2.1   | 3.1 | V                |
| $V_{CCr}$ Data Retention Supply Current | $I_{DR}$            | $2.1 \text{ V} \leq V_{CCr} \leq 2.7 \text{ V}$ ,<br>$V_{IN} = V_{IH}^*$ or $V_{IL}$ ,<br>$\overline{CE1r} = CE2r = V_{IH}^*$ , $I_{OUT} = 0 \text{ mA}$                                                        | —     | 1.5 | mA               |
|                                         | $I_{DR1}$           | $2.1 \text{ V} \leq V_{CCr} \leq 2.7 \text{ V}$ ,<br>$V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CCr} - 0.2 \text{ V}$ ,<br>$\overline{CE1r} = CE2r \geq V_{CCr} - 0.2 \text{ V}$ , $I_{OUT} = 0 \text{ mA}$ | —     | 100 | $\mu\text{A}$    |
| Data Retention Setup Time               | $t_{DRS}$           | $2.7 \text{ V} \leq V_{CCr} \leq 3.1 \text{ V}$ at data retention entry                                                                                                                                         | 0     | —   | ns               |
| Data Retention Recovery Time            | $t_{DRR}$           | $2.7 \text{ V} \leq V_{CCr} \leq 3.1 \text{ V}$ after data retention                                                                                                                                            | 200   | —   | ns               |
| $V_{CCr}$ Voltage Transition Time       | $\Delta V/\Delta t$ | —                                                                                                                                                                                                               | 0.2   | —   | V/ $\mu\text{s}$ |

\* :  $2.0 \text{ V} \leq V_{IH} \leq V_{CCr} + 0.3 \text{ V}$

### • Data Retention Timing



## ■ PIN CAPACITANCE

| Parameter               | Symbol           | Condition            | Value |     |      | Unit |
|-------------------------|------------------|----------------------|-------|-----|------|------|
|                         |                  |                      | Min   | Typ | Max  |      |
| Input Capacitance       | C <sub>IN</sub>  | V <sub>IN</sub> = 0  | —     | —   | 20.0 | pF   |
| Output Capacitance      | C <sub>OUT</sub> | V <sub>OUT</sub> = 0 | —     | —   | 25.0 | pF   |
| Control Pin Capacitance | C <sub>IN2</sub> | V <sub>IN</sub> = 0  | —     | —   | 25.0 | pF   |

Note: Test conditions T<sub>A</sub> = + 25°C, f = 1.0 MHz

## ■ HANDLING OF PACKAGE

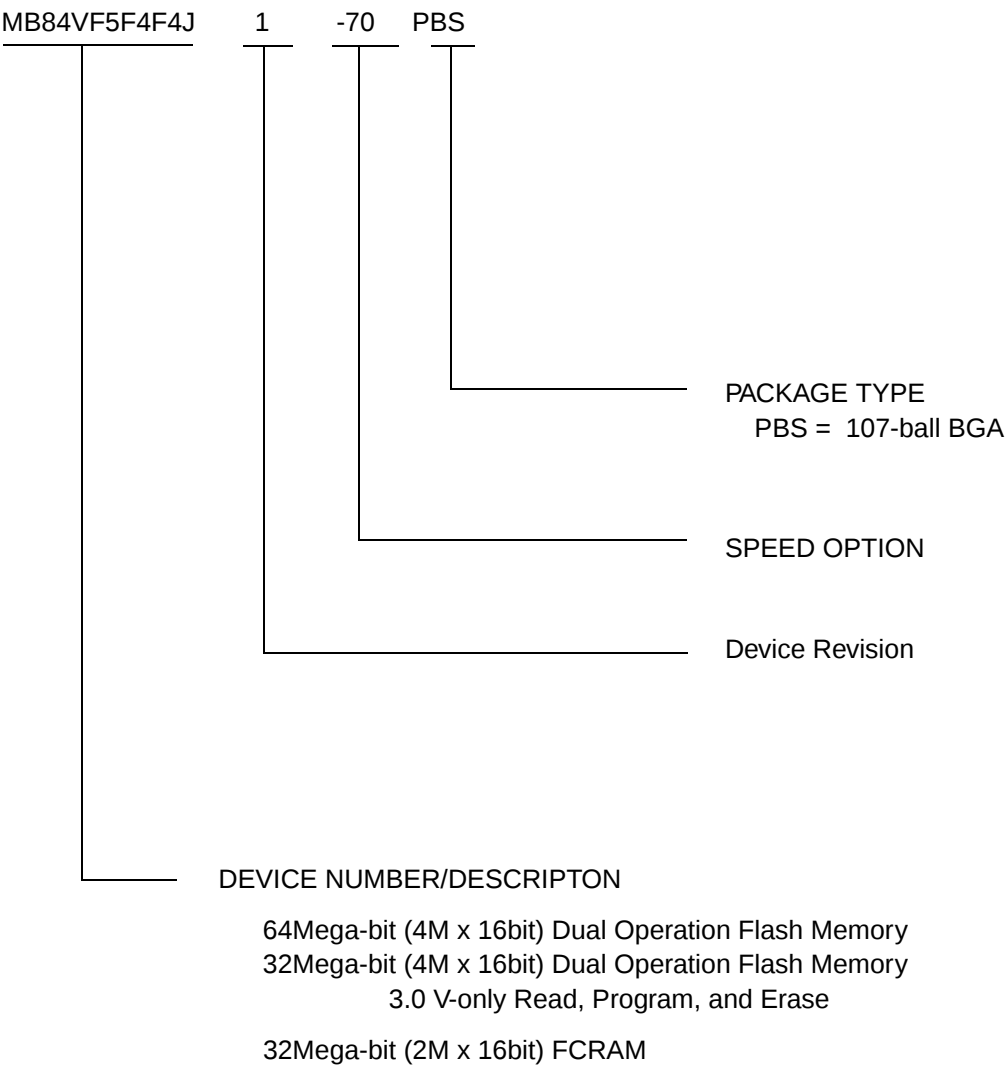
Please handle this package carefully since the sides of package create acute angles.

## ■ CAUTION

- The high voltage (V<sub>ID</sub>) cannot apply to address pins and control pins except RESET. Exception is when autoselect and sector group protect function are used, then the high voltage (V<sub>ID</sub>) can be applied to RESET.
- Without the high voltage (V<sub>ID</sub>) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

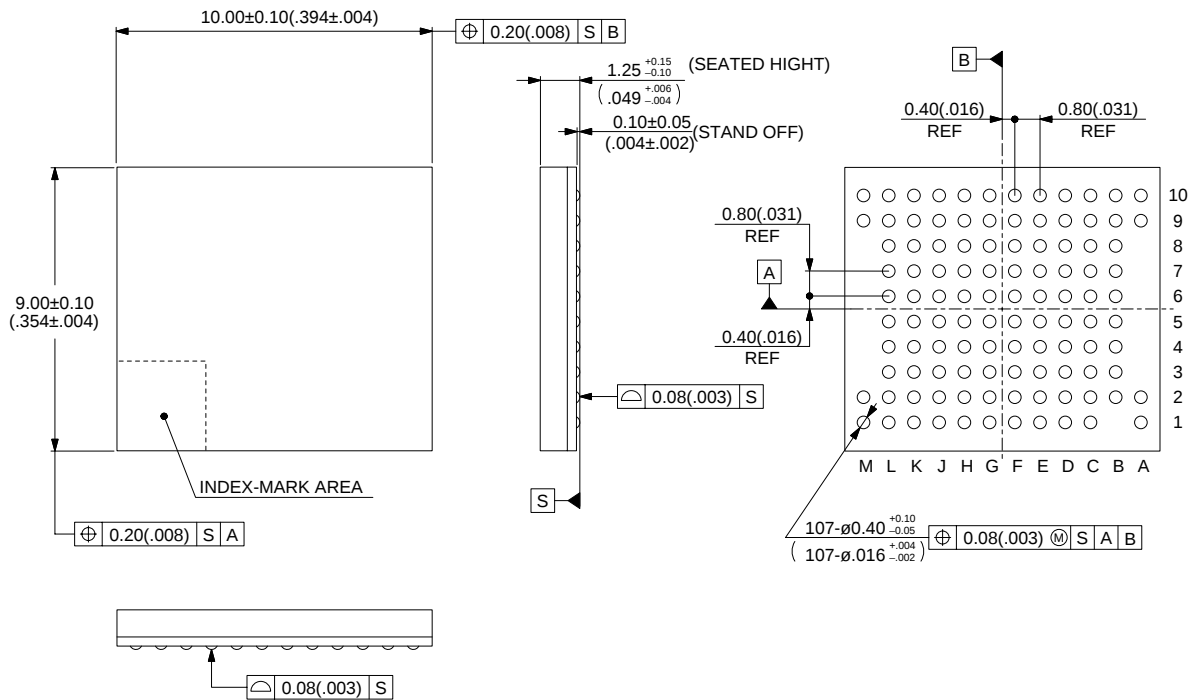
# MB84VF5F4F4J1-70

## ■ ORDERING INFORMATION



## ■ PACKAGE DIMENSION

107-ball plastic FBGA  
(BGA-107P-M01)



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Dimensions in mm (inches).

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