Semicustom

CMOS

Standard cell

CS86 Series

■ DESCRIPTION

The CS86 series of 0.18 µm standard cells is a line of CMOS ASICs based on higher integration implemented by introducing wiring pitch reduction technology and on I/O pad placement technology to the conventional CS81 series.

The CS86 series has three types of cell sets (CS86MN, CS86MZ, and CS86ML), covering a variety of applications, from portable devices requiring low power consumption to image processors requiring large-scale circuitry and high speed.The three types of cell sets can be contained on one chip, allowing those system LSIs to be implemented which require low power consumption as well as high-speed operation for certain types of processing.

■ FEATURES

- Technology : 0.18 µm silicon-gate CMOS, 4- to 6-layer wiring
  The same chip can therefore incorporate the standard transistor cell and the ultrahigh-speed or low-leakage process cell together.
- Supply voltage : +1.8 V ± 0.15 V (normal) to +1.1 V ± 0.1 V
- Junction temperature range : –40 °C to +125 °C
- Cell set
  - CS86MN : Offers standard transistor characteristics. Designed as a library for products requiring higher throughputs.
  - CS86MZ : Offers transistor characteristics suited for ultra high-speed operation, although the current leakage is larger than that of the CS86MN. Designed as a library for products requiring ultra high-speed processing.
  - CS86ML : Offers transistor charactersistics with decreased leak currents. Designed as a library for mobile devices and other products requiring lower power consumption.
- Cell Specifications :

Cell set name	CS86MZ	CS86MN	CS86ML
Delay time*1	65 ps	84 ps	132 ps
Power consumption*2	29.5 nW/MHz	21.2 nW/MHz	16.0 nW/MHz
Leak power*2	3.97 nW	0.0264 nW	0.0007 nW
Supply Voltage	1.1 V to 1.8 V		1.8 V

*1 : 2 input NAND cell (high-power type) , F/O = 2, normal load, Power supply voltage 1.8 V, Temperature = +25 °C

*2 : 2 input NAND cell (low-power type) , F/O = 1, non load, Power supply voltage 1.8 V, Temperature = +25 °C

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- Output buffer cells with noise reduction circuits
- Input buffer cells and bidirectional buffer cells with on-chip input pull-up/pull-down resistors
- Buffer cells for crystal oscillation circuits
- Special interfaces : SSTL2, PCI, P-CML, T-LVTTL, USB 2.0, IEEE1394, and others.
- IP macros : CPU (ARM9, FR-V, and others) , DSP, PCI, IEEE1394, USB 2.0, IrDA, PLL, DAC, ADC, and others.
- Capable of incorporating compiled cells (RAM/ROM/Register file/Delay line)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using Physical Synthesis tool
- Low power consumption using Low Power Synthesis tool
- Short-term development using a timing driven layout tool
- Hierarchical design environment for supporting large-scale circuits
- Support for Signal-Integrity
- Support for Memory (RAM, ROM) SCAN
- Support for Memory (RAM) BIST
- Support for Boundary SCAN
- Support for path delay test
- A variety of package options : QFP, TQFP, LQFP, HQFP, PBGA, FBGA, FLGA, EBGA

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- OR-AND
- Scan Flip Flop
- ENOR
- Boundary Scan Register
- Bus Driver
- AND-OR
- Decoder
- NON-Scan Flip Flop
- Inverter
- Buffer
- OR-AND Inverter
- OR
- Delay Buffer
- Selector
- EOR
- Dummy Clock Buffer
- Others

2. IP macro

CPU	FR-V, ARM9, and others.
DSP	Communications DSP, DSP for Digital AV, and others.
Peripheral Macro	Interval timer, Interruption controller, DMA controller, RTC, Calender, UART, and others.
Interface macro	PCI, IEEE1394, USB 2.0, IrDA, and others.
Multimedia processing macros	JPEG, MPEG 4.0, and others.
Mixed signal macros	ADC, DAC, OPAMP, and others.
Compiled macros	RAM (1 port, 2 port) , ROM, Delay Line, Register file, and others.
PLL	Analog PLL
I/O macro	Compatible with various interface levels between 1.1 V and 5 V; SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others.

■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS86 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 RW)

- High density type/High density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

- Super high density type/Super high density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	64 to 144 K	32 to 2 K	2 to 72	bit

- Large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	24 to 1152 K	4K to 16 K	6 to 72	bit

- Super high density large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	2 to 1152 K	512 to 16 K	4 to 72	bit

- High speed type

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 144 K	64 to 2 K	4 to 72	bit

2. Clock synchronous dual-port RAM (2 addresses : 1 RW, 1 R)

- High density type/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

3. Clock synchronous register file (3 addresses : 1 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

4. Clock synchronous register file (4 addresses : 2 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

5. Clock synchronous ROM (1 addresses : 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 1024 K	128 to 8 K	2 to 128	bit
64	1 to 1024 K	512 to 32 K	2 to 32	bit

6. Clock synchronous delay line memory (2 addresses : 1 W, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 32 K	32 to 1 K	8 to 32	bit
16	384 to 32 K	64 to 2 K	6 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage	V_{DD}	– 0.5	2.5 *1	V
			4.0 *2	
Input voltage	V_I	– 0.5	V_{DD}+0.5 (≤ 2.5 V) *1	V
			V_{DD}+0.5 (≤ 4.0 V) *2	
Output voltage	V_O	– 0.5	V_{DD}+0.5 (≤ 2.5 V) *1	V
			V_{DD}+0.5 (≤ 4.0 V) *2	
Storage temperature	Tst	–55	+125	°C
Junction temperature	T_j	–40	+125	°C
Output current*3	I_O	±10 (3.3 VCMOS, 2.5 VCMOS)		mA
		± 7.5 (1.8 VCMOS)		
Input signal transmitting rate	R_I	—	Clock input*4 : 200 Normal input : 100	Mbps*5
Output signal transmitting rate	R_O	—	100	Mbps*5
Output load capacitance	C_O	—	3000/R_O	pF
Supply pin current*6	I_D	For one V_{DD}/GND pin*6		mA

*1 : Internal gate part in case of single power supply or dual power supply

*2 : I/O part in case 3.3 V I/F or 2.5 V I/F is used by dual power supply.

*3 : DC current which continues more than 10 ms, or average DC current

*4 : in case of I/O cell for clock input

*5 : bps = bit per second

*6 : Supply pin current for one V_{DD}/GND pin (mA)

Source type	Maximum current [mA]		Number of layer
	Standard source	Additional source	
V_{DDE}	30	30	4, 5, 6
V_{DDI}, V_{DD}, V_{SS}	34	34	4, 5
	59	59	6

- How to calculate the number of needed supply pin
  Frame with 6-layer wiring (2 power supplies)
  Maximum current for one V_{DD}/GND pin : V_{DDE} = 30 mA/pin, V_{DDI} = V_{SS} = 59 mA/pin
  Needed supply pin count (internal power supply/external power supply/V_{SS}) : Ni/Ne/Ns
  DC internal maximum power-supply current : Iimax, DC external maximum power-supply current : Iemax

Ni = Iimax/59   Ne = Iemax/30   Ns = Iimax/59 + Iemax/30

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

- **Single power supply** (V_{DD} = 1.8 V ± 0.15 V)

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{DD}	1.65	1.8	1.95	V
“H” level input voltage	V_{IH}	$V_{DD} \times 0.65$	—	$V_{DD} + 0.3$	V
“L” level input voltage	V_{IL}	–0.3	—	$V_{DD} \times 0.35$	V
Junction temperature	T_j	–40	—	+125	°C

- **Dual power supply** (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V/V_{DDI} = 1.1 V ± 0.1 V*)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.65	1.8	1.95	
			1.4	1.5	1.6	
			1.0	1.1	1.2	
“H” level input voltage	1.8 V CMOS	V_{IH}	$V_{DDI} \times 0.65$	—	$V_{DDI} + 0.3$	V
	3.3 V CMOS		2.0	—	$V_{DDE} + 0.3$	
“L” level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	$V_{DDI} \times 0.35$	V
	3.3 V CMOS		–0.3	—	0.8	
Junction temperature		T_j	–40	—	+125	°C

* : V_{DDI} = 1.1 V±0.1 V is being prepared.

- **Dual power supply** (V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V/V_{DDI} = 1.1 V ± 0.1 V*)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	1.65	1.8	1.95	
			1.4	1.5	1.6	
			1.0	1.1	1.2	
“H” level input voltage	1.8 V CMOS	V_{IH}	$V_{DDI} \times 0.65$	—	$V_{DDI} + 0.3$	V
	2.5 V CMOS		1.7	—	$V_{DDE} + 0.3$	
“L” level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	$V_{DDI} \times 0.35$	V
	2.5 V CMOS		–0.3	—	0.7	
Junction temperature		T_j	–40	—	+125	°C

* : V_{DDI} = 1.1 V±0.1 V is being prepared.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC characteristics

- Single power supply : V_{DD} = 1.8 V standard

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
“H” level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD}–0.2	—	V_{DD}	V
“L” level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
“H” level output V-I characteristics	—	1.8 V V_{DD} = 1.8 V±0.15 V	*			—
“L” level output V-I characteristics	—	1.8 V V_{DD} = 1.8 V±0.15 V	*			—
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	Pull up V_{IL} = 0, Pull down V_{IH} = V_{DD}	8	18	40	kΩ

* : Refer to “ (1) 1.8 V” in ■V-I CHARACTERISTICS.

- Dual power supply : V_{DDE} = 3.3 V, V_{DDI} = 1.8 V/1.5 V/1.1 V

(V_{DDE} = 3.3 V±0.3 V/V_{DDI} = 1.8 V ± 0.15 V, V_{DDI} = 1.5 V ± 0.1 V, V_{DDI} = 1.1 V ± 0.1 V,
V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
“H” level output voltage	V_{OH4}	3.3 V Output I_{OH} = –100 µA	V_{DDE}–0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI}–0.2	—	V_{DDI}	
“L” level output voltage	V_{OL4}	3.3 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	
“H” level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V	*1			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	*2			
“L” level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V	*1			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	*2			
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	3.3 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	10	33	80	kΩ
		1.8 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	8	18	40	

*1 : Refer to “ (2) 3.3 V” in ■V-I CHARACTERISTICS.

*2 : Refer to “ (1) 1.8 V” in ■V-I CHARACTERISTICS.

- Dual power supply : V_{DDE} = 2.5 V, V_{DDI} = 1.8 V/1.5 V/1.1 V

(V_{DDE} = 2.5 V±0.2 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V/V_{DDI} = 1.1 V ± 0.1 V,
V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
“H” level output voltage	V_{OH3}	2.5 V Output I_{OH} = –100 µA	V_{DDE}–0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI}–0.2	—	V_{DDI}	
“L” level output voltage	V_{OL3}	2.5 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	
“H” level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V±0.2 V	—			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	*			
“L” level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V±0.2 V	—			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	*			
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	2.5 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDE}	—	25	—	kΩ
		1.8 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	8	18	40	

* : Refer to “ (1) 1.8 V” in ■V-I CHARACTERISTICS.

2. AC CHARACTERISTICS

V_{SS} = 0 V, T_j = – 40 °C to +125 °C. (Standard specification)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	t_{pd}*1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

*1 : Delay time = propagation delay time, enable time, disable time.

*2 : “typ” is calculated based on the cell specifications.

*3 : Measurement conditions

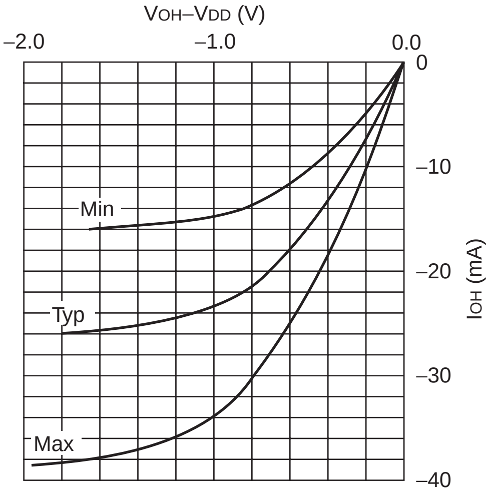
Measurement condition	tmin	ttyp	tmax
V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.62	1.00	1.88
V_{DD} = 1.5 V ± 0.10 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.76	1.25	2.42
V_{DD} = 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	1.08	2.14	6.22

Note : AC characteristics are determined based on junction temperature, voltage conditions, and process variation.

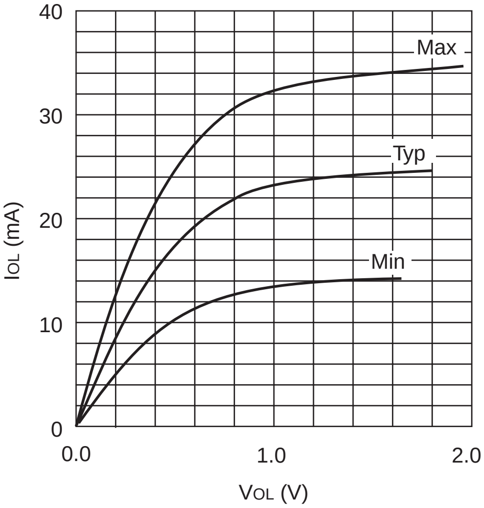
■ V - I CHARACTERISTICS

(1) 1.8 V

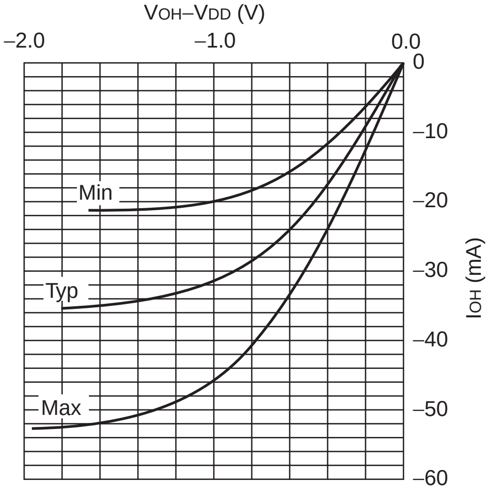
Conditions
Min : Process = Slow, T_j = +125 °C, V_{DD} = 1.65 V
Typ : Process = Typical, T_j = +25 °C, V_{DD} = 1.80 V
Max : Process = Fast, T_j = –40 °C, V_{DD} = 1.95 V



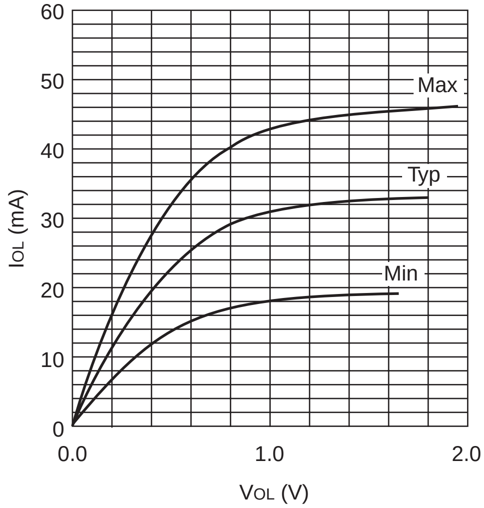
1.8 V CMOS “H” level output
(L, M type)



1.8 V CMOS “L” level output
(L, M type)



1.8 V CMOS “H” level output
(H, V type)

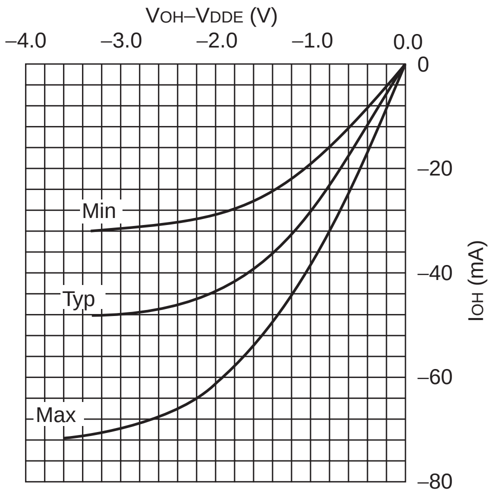


1.8 V CMOS “L” level output
(H, V type)

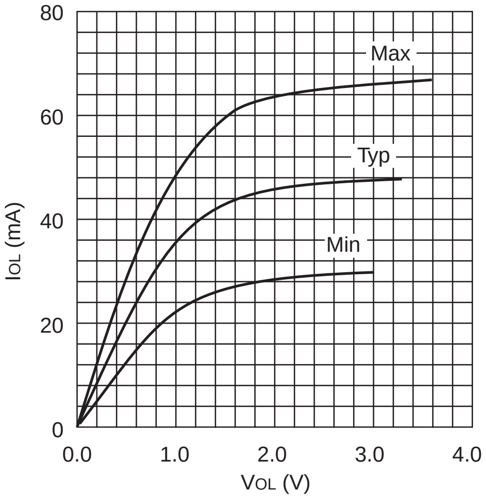
(2) 3.3 V

Conditions

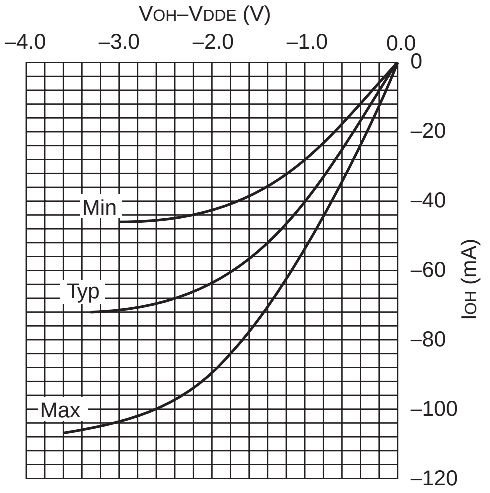
Min : Process = Slow, T_j = +125 °C, V_{DDE} = 3.0 V
Typ : Process = Typical, T_j = +25 °C, V_{DDE} = 3.3 V
Max : Process = Fast, T_j = –40 °C, V_{DDE} = 3.6 V



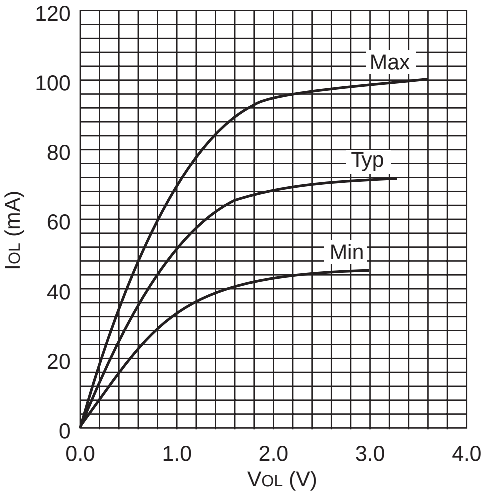
3.3 V CMOS “H” level output
(L, M type)



3.3 V CMOS “L” level output
(L, M type)



3.3 V CMOS “H” level output
(H, V type)



3.3 V CMOS “L” level output
(H, V type)

■ INPUT/OUTPUT PIN CAPACITANCE

(T_j = +25 °C, V_{DD} = VI = 0 V, f = 1 MHz)

Parameter		Symbol	Requirements	Unit
Input pin	—	CIN	Max 16	pF
Output pin	L, M, H, V type	COUT	Max 16	pF
I/O pin	L, M, H, V type	CI/O	Max 16	pF

Note : Capacitance varies according to the package and the location of the pin.

■ DESIGN METHOD

The integrated standard-cell design environment, SCCAD2, provided for conventional models now supports the CS86 series. This allows you to design ASICs that operate at up to 500 MHz with up to 40 million gates and to halve the layout design period. The Fujitsu's tool GLOSCAD also supports the satandard cell design for CS86 series.

- Physical Synthesis

Physical Synthesis tool support is provided on a consulting business basis. A conventional style of ASIC development has a problem that iterations between logic synthesis and layout processing are caused by wiring congestion and the difference between actual and estimated wiring capacities. Supporting logic synthesis based on physical information reduces such iterations and contributes to convergence of ASIC design within the scheduled development period.

- Low Power Synthesis

The Low Power Synthesis tool is supported, which enables the use of gated clock buffers of hard macro type incorporating sequential cells, such as latches. The use of gated clock buffers of hard macro type provides low power consumption by the clock line. It also provides reliable operation, reduction in script complexity, and shorter turnaround time (TAT) for processing.

- Timing Driven Layout

Performing automatic placement and wiring based on chip-level timing constraints. This prevents post-layout timing problems from developing, which are prominent in particular in the field of deep submicron designs. In addition, all of remaining timing errors are automatically corrected by the Fujitsu's automatic timing correction system. This shortens the development time from the end of creating a net list to the beginning of the prototyping stage.

- Hierarchical Design

A top-down hierarchical design approach is taken consistently from logic design to physical design to support larger-scale circuit integration based on deep submicron designing. This enables multiple blocks to be designed logically and physically at the same time and timing convergence to be attained in a short period, providing a design environment capable of easily supporting ultra-large-scale integration of circuits.

- Support for Signal Integrity

Automated power wiring enables layout satisfying the design specifications within a short period.
The power width automatic adjustment function designed taking account of internal power consumption and clock frequencies can produce chips satisfying the current density and voltage drop restrictions without human intervention. Also, a verification system is prepared to check the signal noise or delay penalty owing to capacitive coupling between signal conductors and the voltage drop caused by simultaneous local switching.

■ PACKAGES

Package	Pin count	Material
QFP	176, 208, 240	Plastic
TQFP	100, 120	Plastic
LQFP	144, 176, 208, 256	Plastic
HQFP	208, 240, 256, 304	Plastic
PBGA	256, 352, 420	Plastic
FBGA	112, 144, 168, 176, 192, 224, 240, 272, 288, 304, 368	Plastic
FLGA	144, 176, 208, 224, 288	Plastic
EBGA	660	Plastic

Note : Consult Fujitsu for the combination of each package and the time of availability.

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