TOSHIBA TC7SZU04AFE

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T C 7 S Z U 0 4 A F E

INVERTER

FEATURES

: ± 16 mA (Typ.) High Output Drive

 $@V_{CC} = 4.5 V$

: $I_{CC} < 2 \mu A \text{ (Max.)}$ Low Quiescent Power

 $@V_{CC} = 5.5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}$

: $V_{CC(opr)} = 1.8 \sim 5.5 V$ Operation Voltage Range

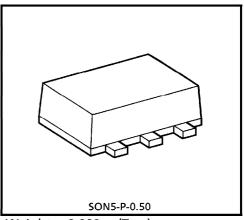
Supply Voltage Data Retention : $V_{CC} = 1.5 \sim 5.5 \text{ V}$

Latch-up Performance : ±500 mA

ESD Performance: Human Body Model > ±2000 V

Machine Model > ±200 V

Power Down Protection is provided on all inputs.



Weight: 0.003 g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~6	V
DC Input Voltage	VIN	-0.5~6	V
DC Output Voltage	Vout	-0.5~V _{CC} + 0.5	٧
Input Diode Current	IK	± 20	mA
Output Diode Current	^I ОК	± 20	mA
DC Output Current	IOUT	± 50	mA
DC V _{CC} / Ground Current	ICC	± 50	mA
Power Dissipation	PD	150	mW
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10 s)	TL	260	°C

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DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC SYMBOL		TECT	TECT COMPLETION .		Ta = 25°C		Ta = −40~85°C			
CHARACTERISTIC	SAMBOL	TEST CONDITION		Vcc (V)	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High-Level Input				1.8	0.85 × V _C C	1	_	0.85 × V _{CC}	_	,,
Voltage	V _{IH}			2.3 – 5.5	0.8 × V _C C		_	0.8 × V _{CC}	_	V
Low-Level Input	vel Input V. VIN = VIH			1.8			0.15 × V _{CC}	_	0.15 × V _{CC}	V
Voltage	or V _{IL}		2.3 – 5.5			0.2 × V _{CC}	_	0.2 × V _{CC}		
				1.8	1.6	1.8	_	1.6	_	
		 Vini	l _{OH} = -100 μA	2.3	2.1	2.3	_	2.1	_	
High-Level		VIN	ΙΟΗ = - 100 μΑ	3.0	2.7	3.0	_	2.7	_	V
	VOH			4.5	4.0	4.4	_	4.0	_	
Output Voltage	VOH	V _{IN} = GND	$I_{OH} = -4 \text{mA}$	2.3	1.9	2.14	_	1.9	_	
			$I_{OH} = -8 \text{mA}$	3.0	2.4	2.75	_	2.4	_	
			IOH = -12 mA	3.0	2.3	2.61	_	2.3	_	
			$I_{OH} = -16 \text{mA}$	4.5	3.8	4.13	_	3.8	_	
		V _{IN} = V _{IH}	I _{OL} = 100 μA	1.8	_	0	0.2	_	0.2	-
				2.3	_	0	0.2	_	0.2	
				3.0		0	0.3	_	0.3	
Low-Level Output Voltage			4.5	_	0	0.5	_	0.5	- v	
		$I_{OL} = 4 \text{ mA}$	2.3	_	0.1	0.3	_	0.3		
		$V_{IN} = V_{CC}$	I _{OL} = 8 mA	3.0	_	0.17	0.4	_	0.4	↓
		"1" = 66	$I_{OL} = 12 \text{ mA}$	3.0	_	0.25	0.55	_	0.55	
		$I_{OL} = 16 \text{mA}$	4.5	_	0.26	0.55	_	0.55		
Input Leakage Current	I _{IN}	$V_{IN} = 5.5 V$ or GND		0 – 5.5	_	_	± 1	_	± 10	μΑ
Quiescent Supply Current	ICC	V _{IN} = V _{CC} or GND		5.5	_	_	2	_	20	μΑ

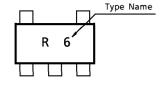
AC ELECTRICAL CHARA	ACTERISTICS (Input	$t_r = t_f = 3 \text{ns})$
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CHARACTERISTIC	HARACTERISTIC SYMBOL TEST CONDITION			Ta = 25°C			Ta = -4	UNIT		
CHARACTERISTIC	VISTIC STIVIBUL	TEST CONDITION	V _C C (V)	MIN.	TYP.	MAX.	MIN.	MAX.	OIVII	
			1.8	1.0	_	8.5	1.0	9.0		
		$C_L = 15 pF$,	2.5 ± 0.2	0.8		6.2	0.8	6.5		
Propagation	t _{PLH}	$R_L = 1 M\Omega$	3.3 ± 0.3	0.5	_	4.5	0.5	4.8]	
Delay Time	t _{PHL}		5.0 ± 0.5	0.5	_	3.9	0.5	4.1	ns	
		$C_L = 50 pF$,	3.3 ± 0.3	1.0	_	6.0	1.0	6.5		
		$R_L = 500 \Omega$	5.0 ± 0.5	0.8	_	5.0	0.8	5.5		
Input Capacitance	C _{IN}		0 - 5.5	_	5	_	_	_	pF	
Power Dissipation	C _{PD}	ower Dissipation	(Note 1)	3.3	_	9	_	_	_	
Capacitance		(Note i)	5.5	_	25	_	_	_	pF	

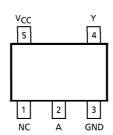
(Note 1): CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$ICC(opr) = CPD \cdot VCC \cdot fIN + ICC$$

MARKING



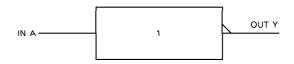
PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

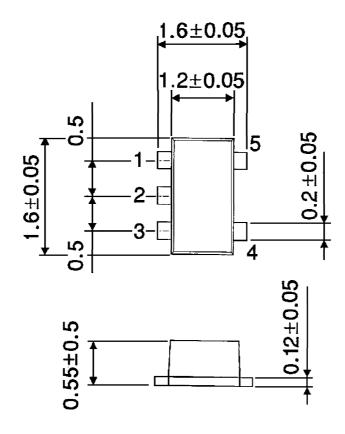
Α	Υ
L	Н
Н	L

LOGIC DIAGRAM



PACKAGE DIMENSIONS SON5-P-0.50

 $\mathsf{Unit}:\mathsf{mm}$



Weight: 0.003 g (Typ.)