TOSHIBA CMOS DIGITAL INTEGRATED CIRCUITS   SILICON MONOLITHIC

T6L37A

SOURCE DRIVER FOR TFT LCD PANELS

The T6L37A is a 64 gray-level, 300 / 309-channel-output source driver for TFT LCD panels. To meet the need for large-sized LCD panels, it allows a maximum operating frequency of 55 MHz. The device accepts 6-bit digital data inputs which, combined with the internal DA converter and 11 reference voltage input pins, allows display of up to 260,000 colors.
Based on high-speed CMOS, the T6L37A offers both low power consumption and high-speed operation. The T6L37A allows configuration of an XGA- or SVGA- compatible, high-performance TFT LCD module.

Unit : mm

T6L37A	USER AREA PITCH	
	IN	OUT

Please contact Toshiba or an authorized Toshiba for the latest TCP specification and product lineup.

TCP (Tape Carrier Package)

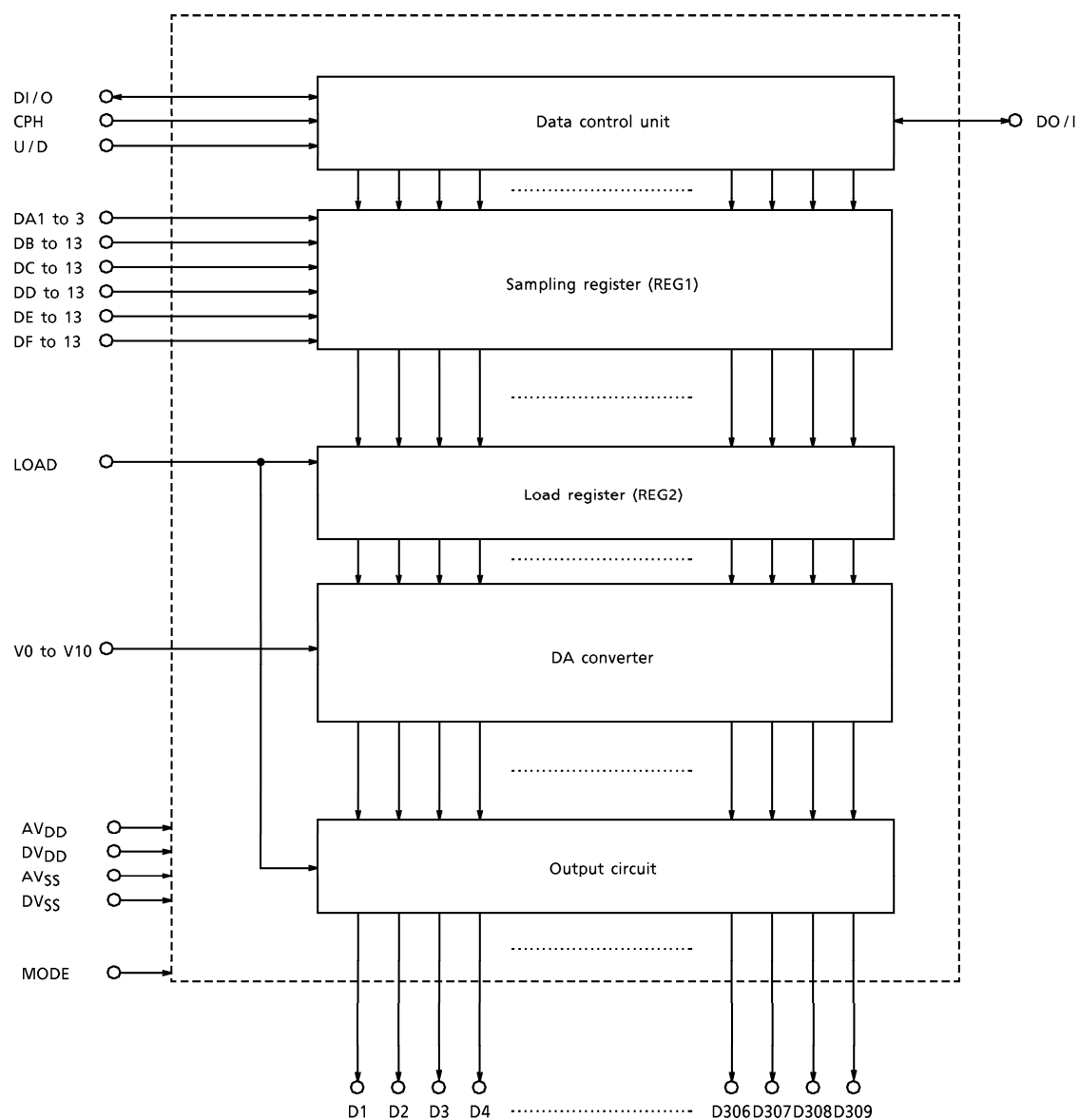## FEATURES

- Grayscale data   : 18-bit digital (3 outputs × 6 bits) parallel transfer method, selectable write direction

- Panel drive outputs   : 300 / 309 outputs, 64 gray levels, DAC system, 11 reference analog voltage inputs

- Fast operation   : Max 55 MHz

- Power supply voltage   : Digital power supply voltage ..... 3.0 to 3.6 V
                               Analog power supply voltage ..... 4.5 to 5.5 V

- Operating temperature : − 20 to 75°C

- Package   : Tape carrier package (TCP)

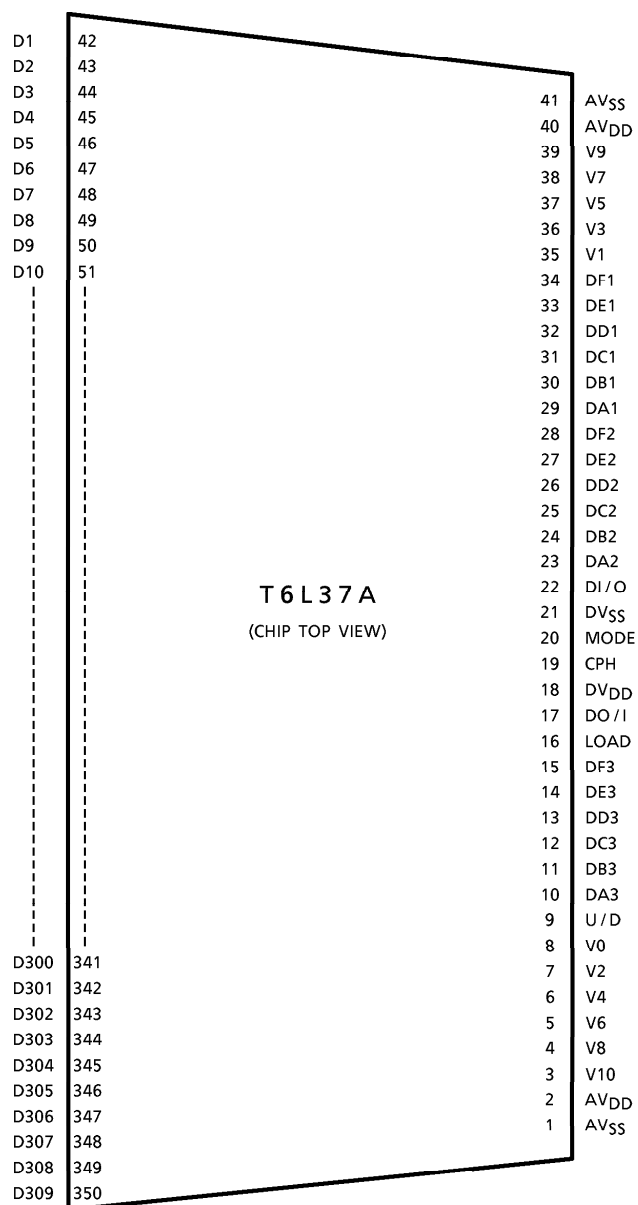- Cascading multiple devices

BLOCK DIAGRAM

PIN ASSIGNMENT

```
D1    42
D2    43
D3    44                                          41  AVSS
D4    45                                          40  AVDD
D5    46                                          39  V9
D6    47                                          38  V7
D7    48                                          37  V5
D8    49                                          36  V3
D9    50                                          35  V1
D10   51                                          34  DF1
                                                  33  DE1
                                                  32  DD1
                                                  31  DC1
                                                  30  DB1
                                                  29  DA1
                                                  28  DF2
                                                  27  DE2
                                                  26  DD2
                                                  25  DC2
                                                  24  DB2
                                                  23  DA2
              T6L37A                              22  DI/O
                                                  21  DVSS
            (CHIP TOP VIEW)                       20  MODE
                                                  19  CPH
                                                  18  DVDD
                                                  17  DO/I
                                                  16  LOAD
                                                  15  DF3
                                                  14  DE3
                                                  13  DD3
                                                  12  DC3
                                                  11  DB3
                                                  10  DA3
                                                   9  U/D
                                                   8  V0
D300  341                                          7  V2
D301  342                                          6  V4
D302  343                                          5  V6
D303  344                                          4  V8
D304  345                                          3  V10
D305  346                                          2  AVDD
D306  347                                          1  AVSS
D307  348
D308  349
D309  350
```

The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributor for the latest TCP specification.

PIN FUNCTION

PIN NAME	I / O	FUNCTION

DI / O
DO / I
	I / O	Data transfer enable pin
		 These pins, become active at the high signal, initiated the transferred data into the sampling register of the device.
		 One is configured as an input and the other is configured as an output of which directions are determined by U / D as shown below.
		
		         | U / D | DI / O | DO / I |
		         | H | Input | Output |
		         | L | Output | Input |
		
		When set for input
		  A high on DI / O or DO / I is latched into the internal logic synchronously with the rising edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data. The grayscale data is latched in sequentially, starting at the next rise of CPH.
		When set for output
		  The pin is used to transfer the enable signal to the T6L37A at the next stage of the LCD driver.
		  The pin enters standby state after outputting a high.

U / D	I	Transfer direction select pin
		  This pin controls the direction in which the data is transferred into the sampling register. Data is transferred synchronously with each rising edge of CPH in one of the following sequences :
		    When U / D is high, data is transferred in the order D1 to D3, D4 to D6, D7 to D9, ·····
		    When U / D is low, the direction is reversed to give D307 to D309, D304 to D306, D301 to D303, ·····
		  The voltage applied to this pin must be a DC-level voltage that is either high or low.

CPH	I	Sampling clock input This clock input is used to transfer grayscale data.

DA1 to 3
DB1 to 3
DC1 to 3
DD1 to 3
DE1 to 3
DF1 to 3
	I	Grayscale data bus
		  The data inputs consist of 6-bit word for each three channel that are transferred in parallel at the rising edge of CPH. The relationship between the grayscale data and the weight of each bit is as follows :
		    Grayscale data
		      $= 32 \times DF_n + 16 \times DE_n + 8 \times DD_n + 4 \times DC_n + 2 \times DB_n + DA_n$
		  (*) where n = 1 to 3
		    The relationship between the grayscale data and the output pins is as follows :
		      DA1, DB1, DC1, DD1, DE1, DF1 ····· D (3m-2)
		      DA2, DB2, DC2, DD2, DE2, DF2 ····· D (3m-1)
		      DA3, DB3, DC3, DD3, DE3, DF3 ····· D (3m) *where m = 1 to 103

PIN NAME	I / O	FUNCTION
MODE	I	Output select pin This signal selects either 300-pin mode or 309-pin mode for the LCD panel driver. When MODE = high, 300-output-pin mode is selected, in which case D151 through D159 are not used. (Voltages appearing at D151 through D159 are indeterminate.) When MODE = low, 309-output-pin mode is selected. This pin is internally pulled up in the chip.
LOAD	I	Data load input pin When a high voltage supplys to the load input, the data is transferred from the Sampling register to the Load register synchronously at the rising edge of CPH. All 300 or 309 LCD panel drive pin outputs are simultaneously updated. The selected analog voltage corresponding to the data are send the LCD.
V_0 to V_{10}		Reference analog input pins These pins are used to input the voltage used for the DAC. Conditions : $AV_{SS} < V0 \leq V1 \leq V2 \leq V3 \leq V4 \leq V5 \leq V6 \leq V7 \leq V8 \leq V9 \leq V10 < AV_{DD}$ or $AV_{SS} < V10 \leq V9 \leq V8 \leq V7 \leq V6 \leq V5 \leq V4 \leq V3 \leq V2 \leq V1 \leq V0 < AV_{DD}$
D_1 to D_{309}	O	LCD panel drive pins
AV_{DD}		Analog power supply pin
AV_{SS}		Analog GND pin This pin must be at the same potential level as the digital GND pin.
DV_{DD}		Digital power supply pin.
DV_{SS}		Digital GND pin This pin must be at the same potential level as the analog GND pin.

DEVICE OPERATION

(1) Starting data transfer

A high input to the data transfer enable pin (DI/O or DO/I) is latched into the internal logic synchronously with the rising edge of CPH, setting the device ready to transfer data. Data transfer starts at the next rise of CPH (see Fig.1-1 and 2-1).
This enable pin must not be held for more than one CPH period.

(2) Data transfer method

The data is latched in from the grayscale bus to the sampling register (REG1) synchronously with each rising edge of CPH.
Grayscale data for three outputs are latched into the device simultaneously in one transfer.
Therefore, the data is latched in 300-output mode by performing 100 transfers, and data is latched in 309-output mode by performing 103 transfers. When the data loading is completed, the device enters a standby state.

(3) Terminating data transfer

The data transfer enable pin (DO/I or DI/O) output goes high synchronously with the rising edge of CPH one clock period before the last data is latched in. It is held high until the next rise of CPH (see Fig.1-1 and 2-1).
The output from this pin can be connected directly as input to the data transfer enable pin (DI/O or DO/I) of the next stage LCD driver. In this way, multiple devices can be easily cascaded to drive a large screen.

(4) Panel drive output

When a high voltage supplies to the load input, the data in the sampling register (REG1) is transferred to the load register (REG2) and the device starts updating output to the LCD panel drive pins.
CPH must be held at the DC level for the duration from three CPH periods after a high input to LOAD is latched in until one clock period before CPH goes high after a high on the data transfer enable pin is latched in following a 1H period (see Fig.1-2).

(5) Reference power supply circuit

The connection between the device and the external reference power supply for Reference analog supply is configured with 7 or 8 resistors of the same specification in series (total of 64 resistor ladders).
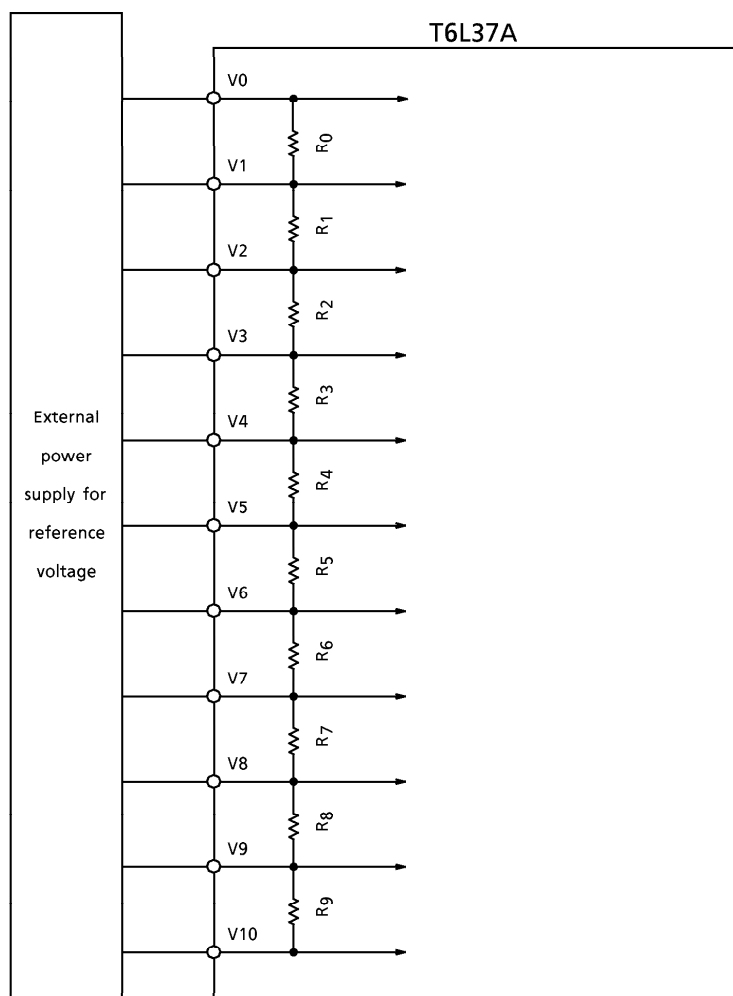
(6) Grayscale data and output voltages

The LCD drive output voltages are determined by the grayscale values and the 11 reverence analog inputs line voltages (V0 to V10).
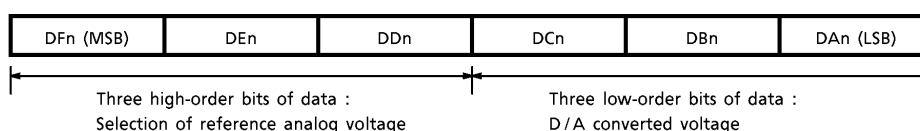
The three high-order data bits select a pair of reference analog voltages. Calculation of the output voltage involves multiplying a value derived from the selected reference analog values by a factor determined by the values of the three low-order bits and dividing by either seven or eight.

DFn (MSB)	DEn	DDn	DCn	DBn	DAn (LSB)

Three high-order bits of data :
Selection of reference analog voltage

Three low-order bits of data :
D / A converted voltage

*n = 1, 2, 3

● Three high-order data bits

DFn	DEn	DDn	SELECTED REFERENCE VOLTAGES
0	0	0	V0 or V1 and V2
0	0	1	V2 and V3
0	1	0	V3 and V4
0	1	1	V4 and V5
1	0	0	V5 and V6
1	0	1	V6 and V7
1	1	0	V7 and V8
1	1	1	V8 and V9 or V10

● Three low-order data bits

(DFn, DEn, DDn) = (0, 0, 0)

(DCn, DBn, DAn)

(DFn, DEn, DDn) = (0, 0, 1) ~ (1, 1, 0)

(DCn, DBn, DAn)
* d = 2 to 7

(DFn, DEn, DDn) = (1, 1, 1)
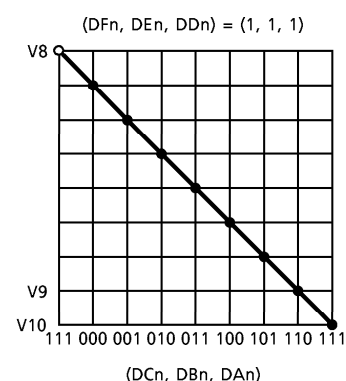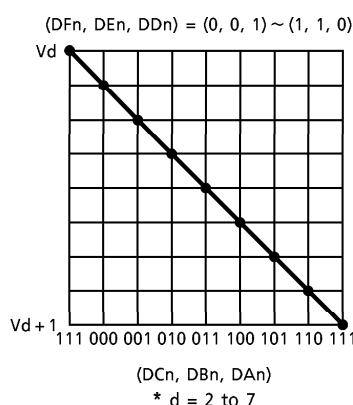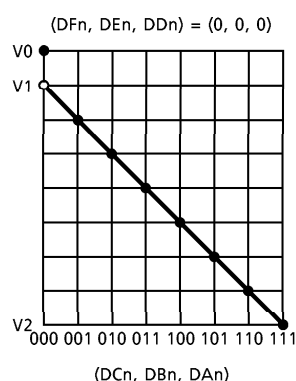
(DCn, DBn, DAn)

● Grayscale data and output voltages

(*) n = 1 to 3

GRAY-SCALE DATA	DFn	DEn	DDn	DCn	DBn	DAn	OUTPUT VOLTAGE
00H	0	0	0	0	0	0	V0
01H	0	0	0	0	0	1	V2 + (V1 − V2) × 6 / 7
02H	0	0	0	0	1	0	V2 + (V1 − V2) × 5 / 7
03H	0	0	0	0	1	1	V2 + (V1 − V2) × 4 / 7
04H	0	0	0	1	0	0	V2 + (V1 − V2) × 3 / 7
05H	0	0	0	1	0	1	V2 + (V1 − V2) × 2 / 7
06H	0	0	0	1	1	0	V2 + (V1 − V2) × 1 / 7
07H	0	0	0	1	1	1	V2
08H	0	0	1	0	0	0	V3 + (V2 − V3) × 7 / 8
09H	0	0	1	0	0	1	V3 + (V2 − V3) × 6 / 8
0AH	0	0	1	0	1	0	V3 + (V2 − V3) × 5 / 8
0BH	0	0	1	0	1	1	V3 + (V2 − V3) × 4 / 8
0CH	0	0	1	1	0	0	V3 + (V2 − V3) × 3 / 8
0DH	0	0	1	1	0	1	V3 + (V2 − V3) × 2 / 8
0EH	0	0	1	1	1	0	V3 + (V2 − V3) × 1 / 8
0FH	0	0	1	1	1	1	V3
10H	0	1	0	0	0	0	V4 + (V3 − V4) × 7 / 8
11H	0	1	0	0	0	1	V4 + (V3 − V4) × 6 / 8
12H	0	1	0	0	1	0	V4 + (V3 − V4) × 5 / 8
13H	0	1	0	0	1	1	V4 + (V3 − V4) × 4 / 8
14H	0	1	0	1	0	0	V4 + (V3 − V4) × 3 / 8
15H	0	1	0	1	0	1	V4 + (V3 − V4) × 2 / 8
16H	0	1	0	1	1	0	V4 + (V3 − V4) × 1 / 8
17H	0	1	0	1	1	1	V4
18H	0	1	1	0	0	0	V5 + (V4 − V5) × 7 / 8
19H	0	1	1	0	0	1	V5 + (V4 − V5) × 6 / 8
1AH	0	1	1	0	1	0	V5 + (V4 − V5) × 5 / 8
1BH	0	1	1	0	1	1	V5 + (V4 − V 5) × 4 / 8
1CH	0	1	1	1	0	0	V5 + (V4 − V5) × 3 / 8
1DH	0	1	1	1	0	1	V5 + (V4 − V5) × 2 / 8
1EH	0	1	1	1	1	0	V5 + (V4 − V5) × 1 / 8
1FH	0	1	1	1	1	1	V5

GRAY-SCALE DATA	DFn	DEn	DDn	DCn	DBn	DAn	OUTPUT VOLTAGE
20H	1	0	0	0	0	0	V6 + (V5 − V6) × 7 / 8
21H	1	0	0	0	0	1	V6 + (V5 − V6) × 6 / 8
22H	1	0	0	0	1	0	V6 + (V5 − V6) × 5 / 8
23H	1	0	0	0	1	1	V6 + (V5 − V6) × 4 / 8
24H	1	0	0	1	0	0	V6 + (V5 − V6) × 3 / 8
25H	1	0	0	1	0	1	V6 + (V5 − V6) × 2 / 8
26H	1	0	0	1	1	0	V6 + (V5 − V6) × 1 / 8
27H	1	0	0	1	1	1	V6
28H	1	0	1	0	0	0	V7 + (V6 − V7) × 7 / 8
29H	1	0	1	0	0	1	V7 + (V6 − V7) × 6 / 8
2AH	1	0	1	0	1	0	V7 + (V6 − V7) × 5 / 8
2BH	1	0	1	0	1	1	V7 + (V6 − V7) × 4 / 8
2CH	1	0	1	1	0	0	V7 + (V6 − V7) × 3 / 8
2DH	1	0	1	1	0	1	V7 + (V6 − V7) × 2 / 8
2EH	1	0	1	1	1	0	V7 + (V6 − V7) × 1 / 8
2FH	1	0	1	1	1	1	V7
30H	1	1	0	0	0	0	V8 + (V7 − V8) × 7 / 8
31H	1	1	0	0	0	1	V8 + (V7 − V8) × 6 / 8
32H	1	1	0	0	1	0	V8 + (V7 − V8) × 5 / 8
33H	1	1	0	0	1	1	V8 + (V7 − V8) × 4 / 8
34H	1	1	0	1	0	0	V8 + (V7 − V8) × 3 / 8
35H	1	1	0	1	0	1	V8 + (V7 − V8) × 2 / 8
36H	1	1	0	1	1	0	V8 + (V7 − V8) × 1 / 8
37H	1	1	0	1	1	1	V8
38H	1	1	1	0	0	0	V9 + (V8 − V9) × 6 / 7
39H	1	1	1	0	0	1	V9 + (V8 − V9) × 5 / 7
3AH	1	1	1	0	1	0	V9 + (V8 − V9) × 4 / 7
3BH	1	1	1	0	1	1	V9 + (V8 − V9) × 3 / 7
3CH	1	1	1	1	0	0	V9 + (V8 − V9) × 2 / 7
3DH	1	1	1	1	0	1	V9 + (V8 − V9) × 1 / 7
3EH	1	1	1	1	1	0	V9
3FH	1	1	1	1	1	1	V10

● Reference analog resistance rate (R0 = 2.31 kΩ)

R0	R1	R2	R3	R4	R5	R6	R7	R8	R9
1.00	2.00	2.77	1.50	0.90	0.84	0.66	0.84	1.42	1.05

TIMING DIAGRAMS

● In 300-output mode

(*) D1 / D307 ; D1 →U / D = high
D307 →U / D = low
(See pin description (U / D) on page 4.)
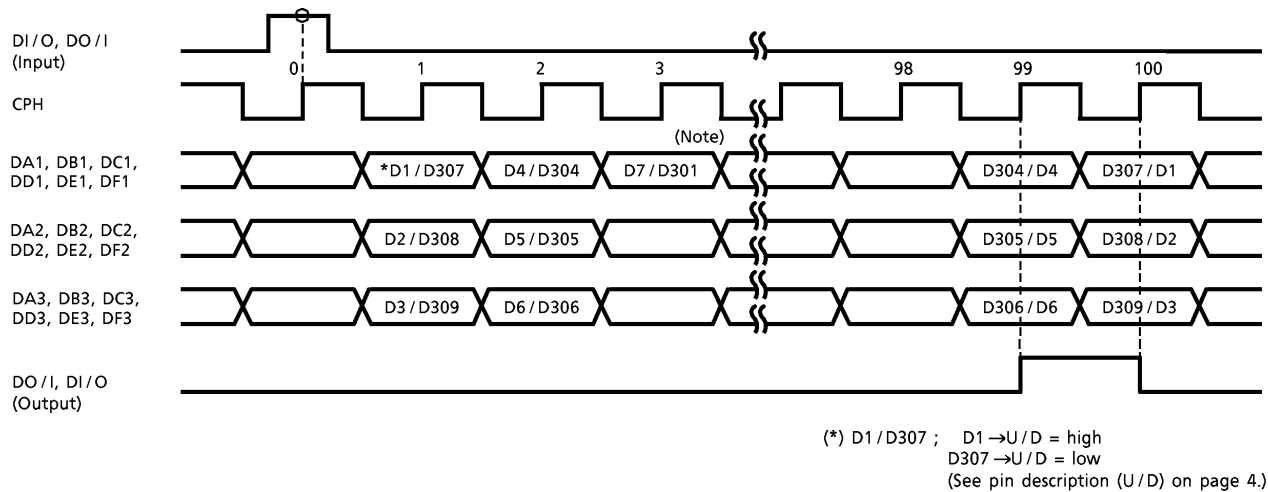
Fig.1-1
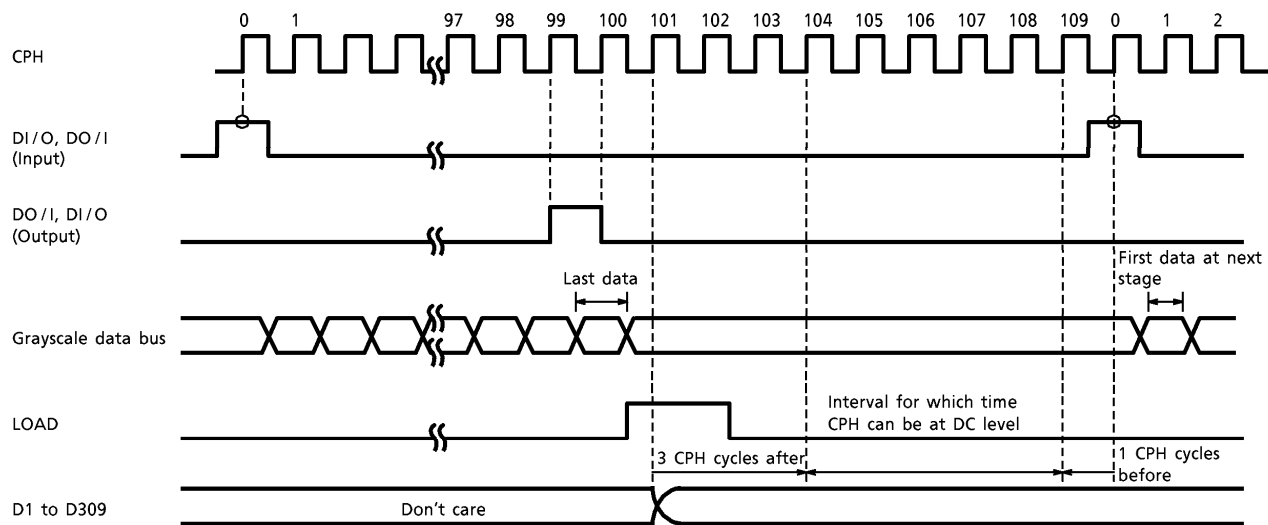
Fig.1-2

(Note) : Except for D151 to D159

● In 309 output mode

(*) D1 / D307 ;   D1 →U / D = high
D307 →U / D = low
(See pin description (U / D) on
page 4.)
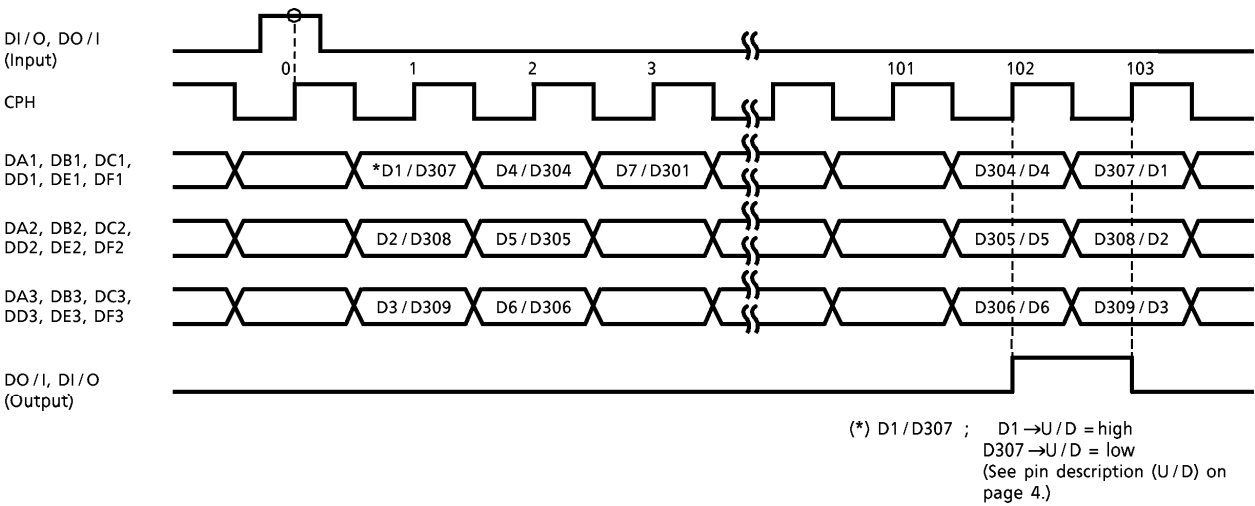
Fig.2-1

Fig.2-2

ABSOLUTE MAXIMUM RATINGS (AV$_{SS}$ = DV$_{SS}$ = 0 V)

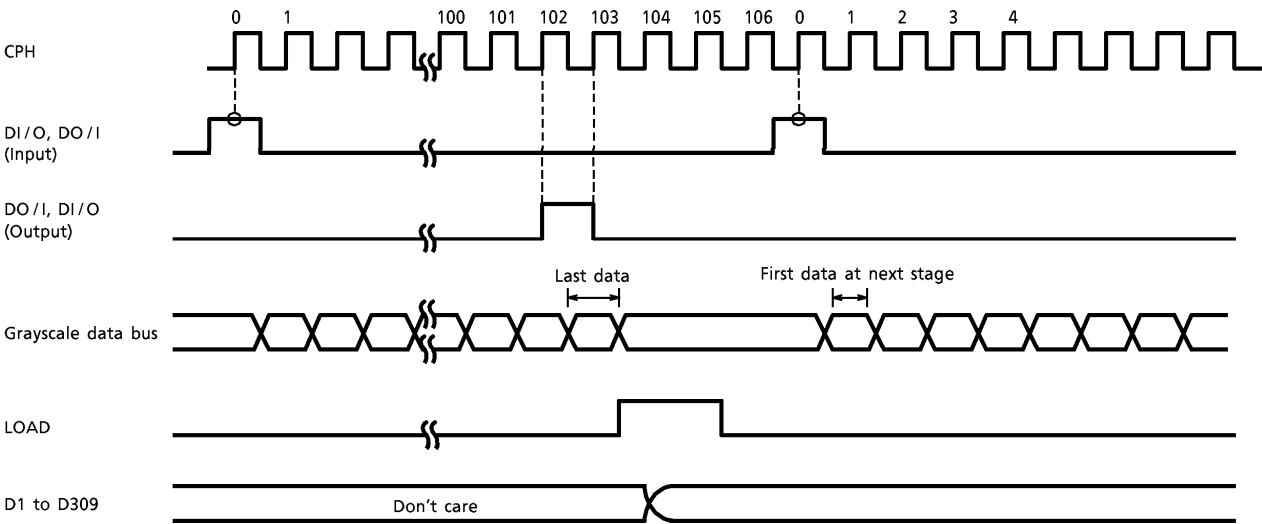| CHARACTERISTICS	SYMBOL	RATING	UNIT	RELEVANT PIN
Analog Supply Voltage	AV$_{DD}$	− 0.3 to 6.5	V	—
Digital Supply Voltage	DV$_{DD}$	− 0.3 to AV$_{DD}$ + 0.3	V	—
Input Voltage	V$_{IN}$	− 0.3 to DV$_{DD}$ + 0.3	V	—
Reference Analog Voltage	V (0 : 10)	− 0.3 to AV$_{DD}$ + 0.3	V	V0 to V10
Storage Temperature	T$_{stg}$	− 55 to 125	°C	—

RECOMMENDED OPERATING CONDITIONS (AV$_{SS}$ = DV$_{SS}$ = 0 V)

CHARACTERISTICS	SYMBOL	TEST CONDITION	RATING	UNIT	RELEVANT PIN
Analog Supply Voltage	AV$_{DD}$	—	4.5 to 5.5	V	—
Digital Supply Voltage	DV$_{DD}$	—	3.0 to 3.6	V	—
Reference Analog Voltage-1 (Note 1)	V1 to V9	—	AV$_{SS}$ + 0.1 to AV$_{DD}$ − 0.1	V	—
Reference Analog Voltage-2 (Note 1)	V0	Case 1	V1 to AV$_{DD}$	V	—
		Case 2	AV$_{SS}$ to V1		
	V10	Case 1	AV$_{SS}$ to V9		
		Case 2	V9 to AV$_{DD}$		
Driver Unit Output Voltage	V$_{OUT}$	—	AV$_{SS}$ + 0.1 to AV$_{DD}$ − 0.1	V	D1 to D309
Operating Temperature	T$_{opr}$	—	− 20 to 75	°C	—
Operating Frequency	f$_{CPH}$	—	DC to 55	MHz	CPH
Output Load Capacitance	C$_L$	—	150 (max)	pF / PIN	D1 to D309

(Note 1) : The following shows the relative magnitude of each reference analog voltage :
- For case 1
  AV$_{SS}$ < V10, Vd $\leqq$ Vd − 1, V0 < AV$_{DD}$ (where d = 9 to 1)
- For case 2
  AV$_{SS}$ < V0, Vd $\leqq$ Vd + 1, V10 < AV$_{DD}$ (where d = 1 to 9)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS $\left(\begin{array}{l}\text{Referenced to } AV_{DD} = 4.5 \text{ to } 5.5 \text{ V}, DV_{DD} = 3.0 \text{ to } 3.6 \text{ V}, AV_{SS} = DV_{SS} = 0 \text{ V}, \\ Ta = -20 \text{ to } 75°C \text{ unless otherwise noted}\end{array}\right)$

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	RELEVANT PIN
Input Voltage	Low Level	V_{IL}	—	—	0	—	$0.3 \times DV_{DD}$	V	Logic input
	High Level	V_{IH}		—	$0.7 \times DV_{DD}$	—	DV_{DD}		
Output Voltage	Low Level	V_{OL}	—	$I_{OL} = 1.0 \text{ mA}$	DV_{SS}	—	$DV_{SS} + 0.5$	V	Logic output
	High Level	V_{OH}		$I_{OH} = -1.0 \text{ mA}$	$DV_{DD} - 0.5$	—	DV_{DD}		
Output Current (Note 2)		Ichg	—	$V_{OUT} = AV_{DD} = 5 \text{ V}$ $V_X = 4 \text{ V}$	—	—	-0.15	mA	D1 to D309
		Idis		$V_{OUT} = 0 \text{ V}$ $AV_{DD} = 5 \text{ V}$ $V_X = 1 \text{ V}$	0.5	—	—		
Resistance between Reference Analog Voltage Pins		R_{GMA}	—	—	—	30	—	$k\Omega$	V0 to V10
Output Voltage Deviation		V_{DO}	—	—	—	± 20	—	mV	D1 to D309
Leakage Current		I_{IN}	—	—	-1.0	—	1.0	μA	Logic input
Standby Current		ID_{STB}	—	$fCPH = DC$	-5.0	0.0	5.0	μA	DV_{DD}
Current Consumption (1)		AI_{DD}	—	$fCPH = 30 \text{ MHz}$ $1H = 30 \mu s,$ non-load Checkerboard pattern $AV_{DD} = 5.5 \text{ V}$	—	4.0	7.0	mA	AV_{DD}
		DI_{DD}		$fCPH = 30 \text{ MHz}$ $1H = 30 \mu s,$ non-load Checkerboard pattern $DV_{DD} = 3.6 \text{ V}$	—	6.0	8.0		DV_{DD}
Current Consumption (2)		AI_{DD}	—	$fCPH = 20 \text{ MHz}$ $1H = 26.4 \mu s,$ non-load Checkerboard pattern $AV_{DD} = 5.0 \text{ V}$	—	3.5	6.0	mA	AV_{DD}
		DI_{DD}		$fCPH = 20 \text{ MHz}$ $1H = 26.4 \mu s,$ non-load Checkerboard pattern $DV_{DD} = 3.0 \text{ V}$	—	2.5	5.5		DV_{DD}

(Note 2) : V_X denotes the voltage applied to the LCD panel drive pin.
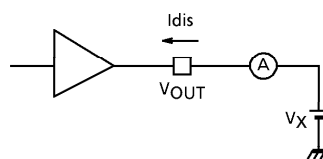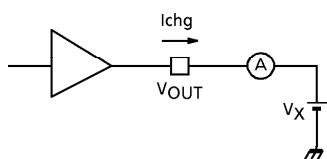
AC CHARACTERISTICS (Referenced to AV_{DD} = 4.5 to 5.5 V, DV_{DD} = 3.0 to 3.6 V, DV_{SS} = AV_{SS} = 0 V, Ta = −20 to 75°C unless otherwise noted)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
CPH Pulse Width H	tCWH	—	—	4.0	—	—	ns
CPH Pulse Width L	tCWL	—	—	4.0	—	—	ns
Enable Setup Time	tsDI	—	—	4.0	—	—	ns
Enable Hold Time	thDI	—	—	0	—	—	ns
Enable Pulse Width H	tDWH	—	—	—	1.0	—	CPH period
Data Setup Time	tsDD	—	—	4.0	—	—	ns
Data Hold Time	thDD	—	—	0	—	—	ns
Output Delay Time 1	tpdDO	—	C_L = 35 pF	—	—	14.0	ns
Output Delay Time 2	tpdDE	—	C_L = 2 kΩ + 75 pF × 2 Target output voltage ± AV_{DD} × 0.1	—	—	3.0	μs
Output Delay Time 3	tpdDX	—	C_L = 2 kΩ + 75 pF × 2 Target output voltage	—	—	10.0	μs
LOAD Setup Time 1	tsLD1	—	—	1.0	—	—	CPH period
LOAD Setup Time 2	tsLD2	—	—	7.0	—	—	ns
LOAD Pulse Width H	tLWH	—	—	2.0	—	—	CPH period

tCWH

tCWL

CPH

0.7 × DV$_{DD}$

0.7 × DV$_{DD}$ 0.3 × DV$_{DD}$ 0.3 × DV$_{DD}$

DI/O, DO/I
(Input)

0.7 × DV$_{DD}$

tsDI   thDI

0.7 × DV$_{DD}$

CPH

0.7 × DV$_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

tsDD   thDD

0.7 × DV$_{DD}$ / 0.3 × DV$_{DD}$

CPH

0.7 × DV$_{DD}$

tpdDO   tDWH

DO/I, DI/O
(Output)

0.7 × DV$_{DD}$

0.7 × DV$_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

VALID   LAST VALID   INVALID

CPH

0.7 × DV$_{DD}$

DI/O, DO/I
(Input)

0.7 × DV$_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

VALID   VALID   LAST VALID   INVALID

tsLD2   tsLD1

LOAD

0.7 × DV$_{DD}$

0.7 × DV$_{DD}$

tLWH

tpdDE

D1 to D309

90%
10%

tpdDX   Target output voltage