

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX162835FT**LOW-VOLTAGE 18-BIT UNIVERSAL BUS DRIVER
WITH 3.6 V TOLERANT INPUTS AND OUTPUTS**

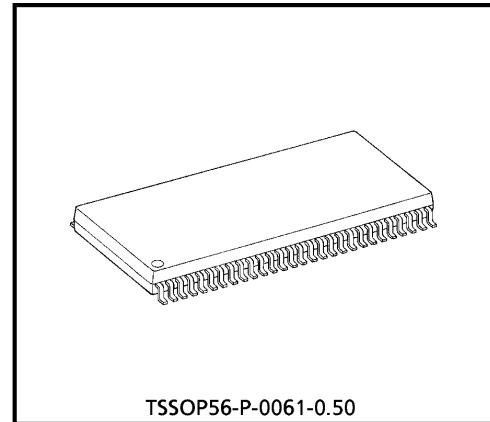
The TC74VCX162835FT is a high performance CMOS 18-bit UNIVERSAL BUS DRIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch / flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

The $26\text{-}\Omega$ series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.



Weight : 0.25 g (Typ.)

FEATURES

- 26- Ω Series Resistors on Outputs.
- Low Voltage Operation : $V_{CC} = 1.8\sim 3.6\text{ V}$
- High Speed Operation : $t_{pd} = 3.9\text{ ns (max)} \text{ at } V_{CC} = 3.0\sim 3.6\text{ V}$
: $t_{pd} = 5.0\text{ ns (max)} \text{ at } V_{CC} = 2.3\sim 2.7\text{ V}$
: $t_{pd} = 9.8\text{ ns (max)} \text{ at } V_{CC} = 1.8\text{ V}$
- 3.6 V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 12\text{ mA (min)} \text{ at } V_{CC} = 3.0\text{ V}$
: $I_{OH}/I_{OL} = \pm 8\text{ mA (min)} \text{ at } V_{CC} = 2.3\text{ V}$
: $I_{OH}/I_{OL} = \pm 4\text{ mA (min)} \text{ at } V_{CC} = 1.8\text{ V}$
- Latch-up Performance : $\pm 300\text{mA}$
- ESD Performance : Human Body Model $> \pm 2000\text{ V}$
: Machine Model $> \pm 200\text{ V}$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) : To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

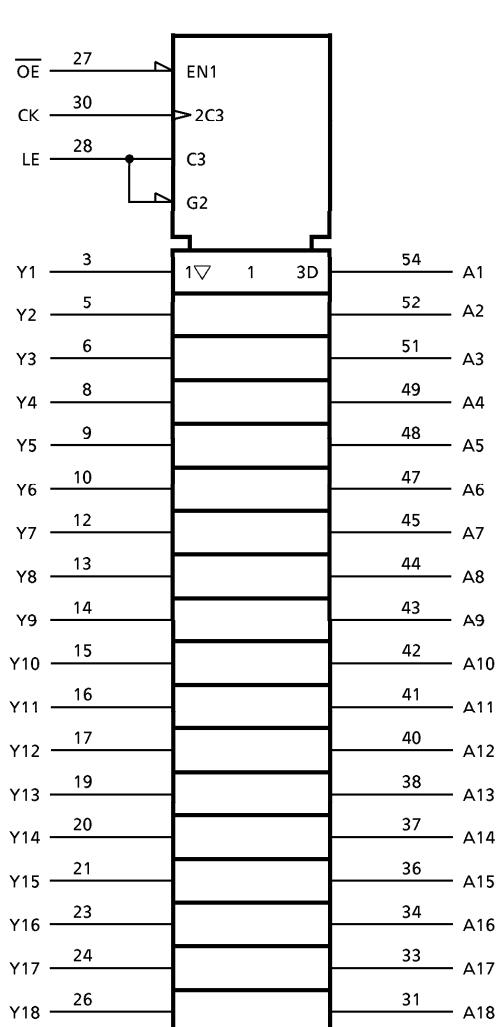
980910EBA2

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN ASSIGNMENT

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
V _{CC}	7	50	V _{CC}
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
V _{CC}	22	35	V _{CC}
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
\overline{OE}	27	30	CK
LE	28	29	GND

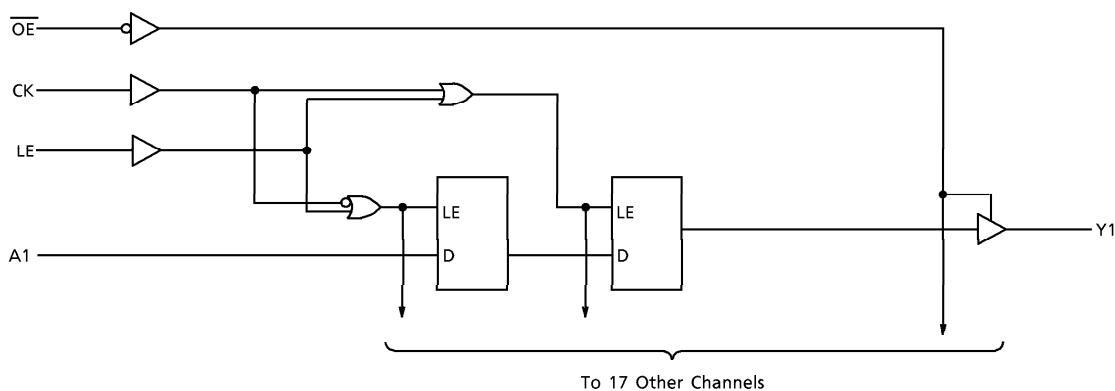
(TOP VIEW)

SYMBOL

TRUTH TABLE

INPUTS				OUTPUTS Y
\overline{OE}	LE	CK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0^*
L	L	L	X	Y_0^*

* Output level before the indicated steady-state input conditions were established, provided that CK was high or low before LE went low.

SYSTEM DIAGRAM

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~4.6	V
DC Input Voltage	V_{IN}	-0.5~4.6	V
DC Output Voltage	V_{OUT}	-0.5~4.6 (Note 2)	V
		-0.5~ V_{CC} + 0.5 (Note 3)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 4)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{stg}	-65~150	°C

(Note 2) : Off-State

(Note 3) : High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 4) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ **RECOMMENDED OPERATING RANGE**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 5)	
Input Voltage	V_{IN}	-0.3~3.6	V
Output Voltage	$V_{I/O}$	0~3.6 (Note 6)	V
		0~ V_{CC} (Note 7)	
Output Current	I_{OH}/I_{OL}	± 12 (Note 8)	mA
		± 8 (Note 9)	
		± 4 (Note 10)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 11)	ns/V

(Note 5) : Data Retention Only

(Note 6) : Off-State

(Note 7) : High or Low State

(Note 8) : $V_{CC} = 3.0\sim 3.6$ V(Note 9) : $V_{CC} = 2.3\sim 2.7$ V(Note 10) : $V_{CC} = 1.8$ V(Note 11) : $V_{IN} = 0.8\sim 2.0$ V, $V_{CC} = 3.0$ V

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.7 V < V_{CC} \leq 3.6 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT		
Input Voltage	"H" Level	V_{IH}				2.7~3.6	2.0	—		
	"L" Level	V_{IL}				2.7~3.6	—	0.8		
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	2.7~3.6	$V_{CC} - 0.2$	—	V		
				$I_{OH} = -6 mA$	2.7	2.2	—			
				$I_{OH} = -8 mA$	3.0	2.4	—			
				$I_{OH} = -12 mA$	3.0	2.2	—			
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.7~3.6	—	0.2			
				$I_{OL} = 6 mA$	2.7	—	0.4			
				$I_{OL} = 8 mA$	3.0	—	0.55			
				$I_{OL} = 12 mA$	3.0	—	0.8			
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim3.6 V$		2.7~3.6		—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL}		$V_{OUT} = 0\sim3.6 V$		2.7~3.6	—	± 10.0	μA	
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0		—	10.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		2.7~3.6		—	20.0	μA		
		$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		2.7~3.6		—	± 20.0			
Increase In I_{CC} Per Input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6 V$		2.7~3.6		—	750	μA		

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.3 V \leq V_{CC} \leq 2.7 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT		
Input Voltage	"H" Level	V_{IH}				2.3~2.7	1.6	—		
	"L" Level	V_{IL}				2.3~2.7	—	0.7		
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	2.3~2.7	$V_{CC} - 0.2$	—	V		
				$I_{OH} = -4 mA$	2.3	2.0	—			
				$I_{OH} = -6 mA$	2.3	1.8	—			
				$I_{OH} = -8 mA$	2.3	1.7	—			
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.3~2.7	—	0.2			
				$I_{OL} = 6 mA$	2.3	—	0.4			
				$I_{OL} = 8 mA$	2.3	—	0.6			
				0		—	10.0	μA		
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim3.6 V$		2.3~2.7		—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL}		$V_{OUT} = 0\sim3.6 V$		2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0		—	10.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		2.3~2.7		—	20.0	μA		
		$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		2.3~2.7		—	± 20.0			

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $1.8 V \leq V_{CC} < 2.3 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	$0.7 \times V_{CC}$	—	V
	"L" Level	V_{IL}			1.8~2.3	—	$0.2 \times V_{CC}$	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	1.8	$V_{CC} - 0.2$	—	V
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	1.8	—	0.2	
Input Leakage Current		I_{IN}	$V_{IN} = 0\sim3.6 V$		1.8	—	± 5.0	μA
3-State Output Off-State Current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim3.6 V$		1.8	—	± 10.0	μA
Power Off Leakage Current		I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND $V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		1.8	—	20.0	μA
					1.8	—	± 20.0	

AC characteristics ($T_a = -40\sim85^\circ C$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	MIN	MAX	UNIT
			1.8	100	—	
Maximum Clock Frequency	f_{MAX}	(Fig.1, 3)	2.5 ± 0.2	200	—	MHz
			3.3 ± 0.3	250	—	
			1.8	1.5	9.8	
Propagation Delay Time (An-Yn)	t_{pLH} t_{pHL}	(Fig.1, 2)	2.5 ± 0.2	0.8	5.0	ns
			3.3 ± 0.3	0.6	3.9	
			1.8	2.0	9.2	
Propagation Delay Time (CK-Yn)	t_{pLH} t_{pHL}	(Fig.1, 3)	2.5 ± 0.2	1.5	5.2	ns
			3.3 ± 0.3	1.4	4.2	
			1.8	1.5	9.8	
Propagation Delay Time (LE-Yn)	t_{pLH} t_{pHL}	(Fig.1, 4)	2.5 ± 0.2	0.8	5.8	ns
			3.3 ± 0.3	0.6	4.7	
			1.8	1.5	9.8	
Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 5)	2.5 ± 0.2	0.8	5.9	ns
			3.3 ± 0.3	0.6	4.3	
			1.8	1.5	7.9	
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 5)	2.5 ± 0.2	0.8	4.7	ns
			3.3 ± 0.3	0.6	4.2	
			1.8	4.0	—	
Minimum Pulse Width	$t_w (\text{H})$ $t_w (\text{L})$	(Fig.1, 3, 4)	2.5 ± 0.2	1.5	—	ns
			3.3 ± 0.3	1.5	—	
			1.8	2.5	—	
Minimum Set-up Time (An-CK, An-LE)	t_s	(Fig.1, 3, 4)	2.5 ± 0.2	1.5	—	ns
			3.3 ± 0.3	1.5	—	
			1.8	1.0	—	
Minimum Hold Time (An-CK, An-LE)	t_h	(Fig.1, 3, 4)	2.5 ± 0.2	0.7	—	ns
			3.3 ± 0.3	0.7	—	
			1.8	—	0.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 12)	2.5 ± 0.2	—	0.5	ns
			3.3 ± 0.3	—	0.5	
			1.8	—	0.5	

(Note 12) : Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

AC characteristics ($T_a = 0\sim 85^\circ C$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 0 \text{ pF}$, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	MIN	MAX	UNIT
Propagation Delay Time (An-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 2)	3.3 ± 0.15	0.9	2.0	ns
Propagation Delay Time (CK-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 3)	3.3 ± 0.15	1.4	2.9	ns
Propagation Delay Time (LE-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 4)	3.3 ± 0.15	0.7	3.4	ns
Output Enable Time (Note 13)	t_{pZL} t_{pZH}	(Fig.1, 5)	3.3 ± 0.15	0.7	3.0	ns
Output Disable Time (Note 13)	t_{pLZ} t_{pHZ}	(Fig.1, 5)	3.3 ± 0.15	0.7	2.9	ns
Minimum Set-up Time (An-CK, An-LE) (Note 13)	t_s	(Fig.1, 3, 4)	3.3 ± 0.15	1.5	—	ns
Minimum Hold Time (An-CK, An-LE) (Note 13)	t_h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7	—	ns

(Note 13) : TOSHIBA SPICE simulation data.

AC characteristics ($T_a = 0\sim 85^\circ C$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	MIN	MAX	UNIT
Propagation Delay Time (An-Yn)	t_{pLH} t_{pHL}	(Fig.1, 2)	3.3 ± 0.15	1.0	4.2	ns
Propagation Delay Time (CK-Yn)	t_{pLH} t_{pHL}	(Fig.1, 3)	3.3 ± 0.15	1.9	4.5	ns
Propagation Delay Time (LE-Yn)	t_{pLH} t_{pHL}	(Fig.1, 4)	3.3 ± 0.15	1.0	5.0	ns
Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 5)	3.3 ± 0.15	1.0	4.6	ns
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 5)	3.3 ± 0.15	1.0	4.5	ns
Minimum Set-up Time (An-CK, An-LE)	t_s	(Fig.1, 3, 4)	3.3 ± 0.15	1.5	—	ns
Minimum Hold Time (An-CK, An-LE)	t_h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7	—	ns

Dynamic switching characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	1.8	0.25	V
		$V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	2.5	0.35	
		$V_{IH} = 3.3 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	3.3	0.45	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	1.8	-0.25	V
		$V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	2.5	-0.35	
		$V_{IH} = 3.3 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	3.3	-0.45	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	1.8	1.35	V
		$V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	2.5	1.85	
		$V_{IH} = 3.3 \text{ V}$, $V_{IL} = 0 \text{ V}$ (Note 14)	3.3	2.45	

(Note 14) : Parameter guaranteed by design.

Capacitive characteristics ($T_a = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	TYP.	UNIT
Input Capacitance	C_{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	$C_{I/O}$		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10 \text{ MHz}$ (Note 15)	1.8, 2.5, 3.3	20	pF

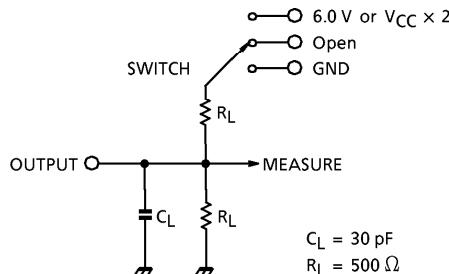
(Note 15) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

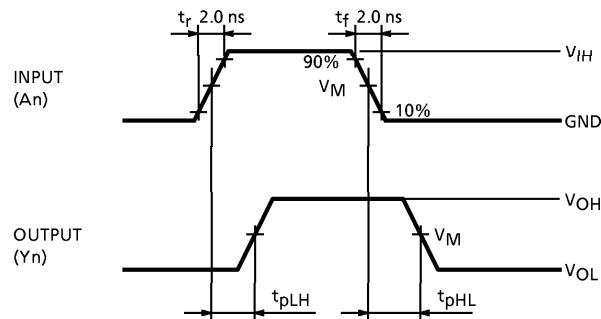
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 18 \text{ (per bit)}$$

TEST CIRCUIT

Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	$6.0 \text{ V} @ V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} \times 2 @ V_{CC} = 2.5 \pm 0.2 \text{ V}$ $@ V_{CC} = 1.8 \text{ V}$
t_{pHZ}, t_{pZH}	GND

AC WAVEFORMFig.2 t_{pLH}, t_{pHL} 

SYMBOL	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC} / 2$	$V_{CC} / 2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

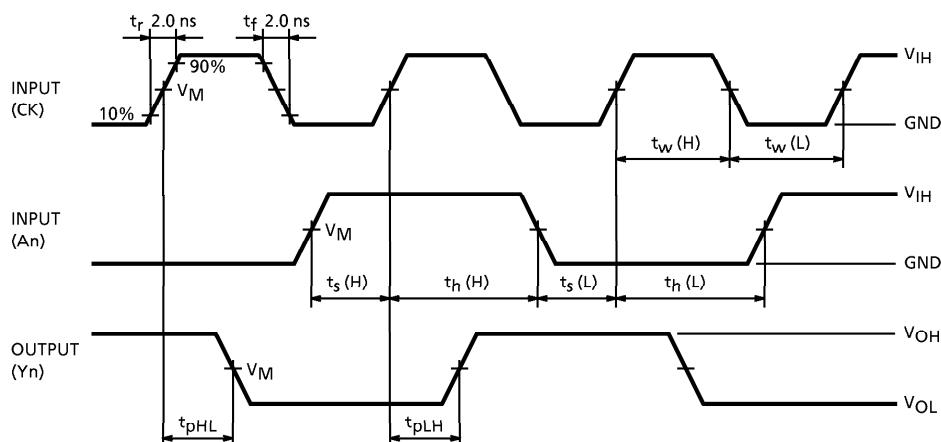
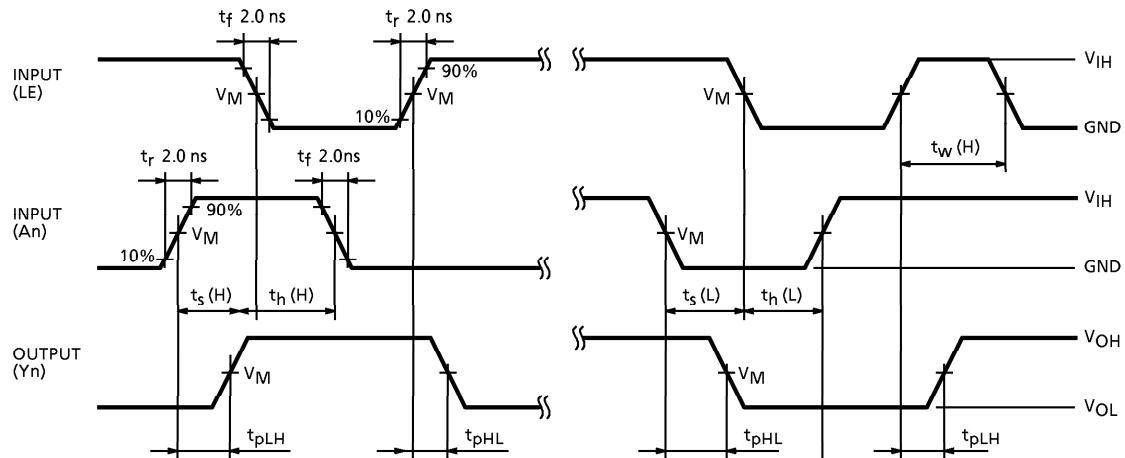
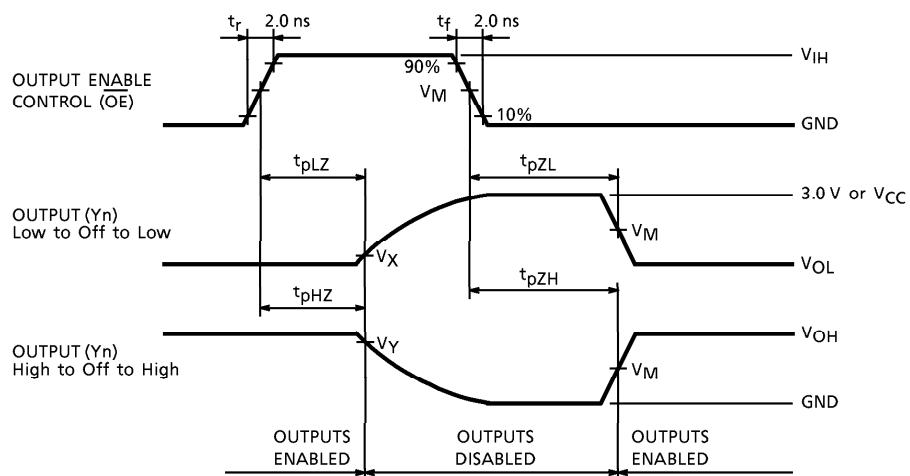
Fig.3 $t_{pLH}, t_{pHL}, t_w, t_s, t_h$ 

Fig.4 t_{PLH} , t_{PHL} , t_w , t_s , t_h Fig.5 t_{PLZ} , t_{PHZ} , t_{pzL} , t_{pzH} 

IBIS CHARACTERISTICS (Typ.)

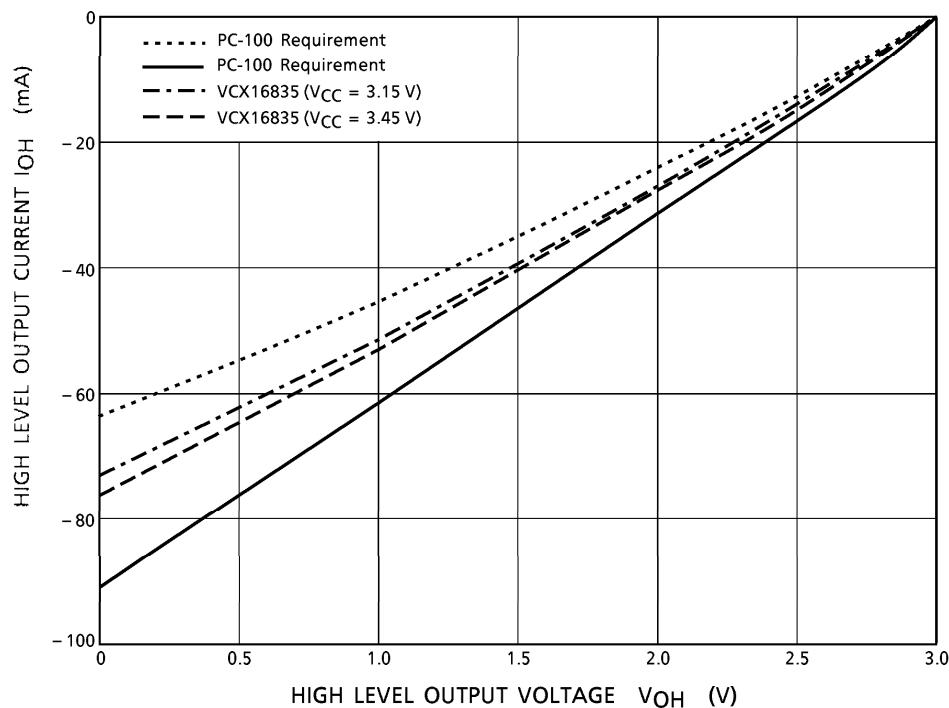


Fig.6 I/V Characteristics-Pullup

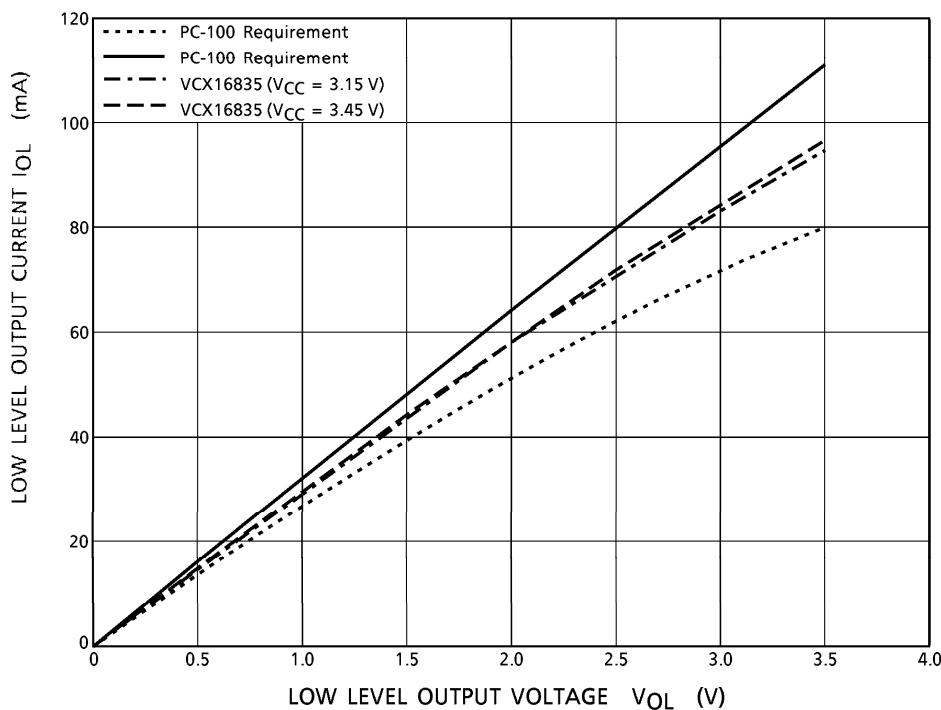
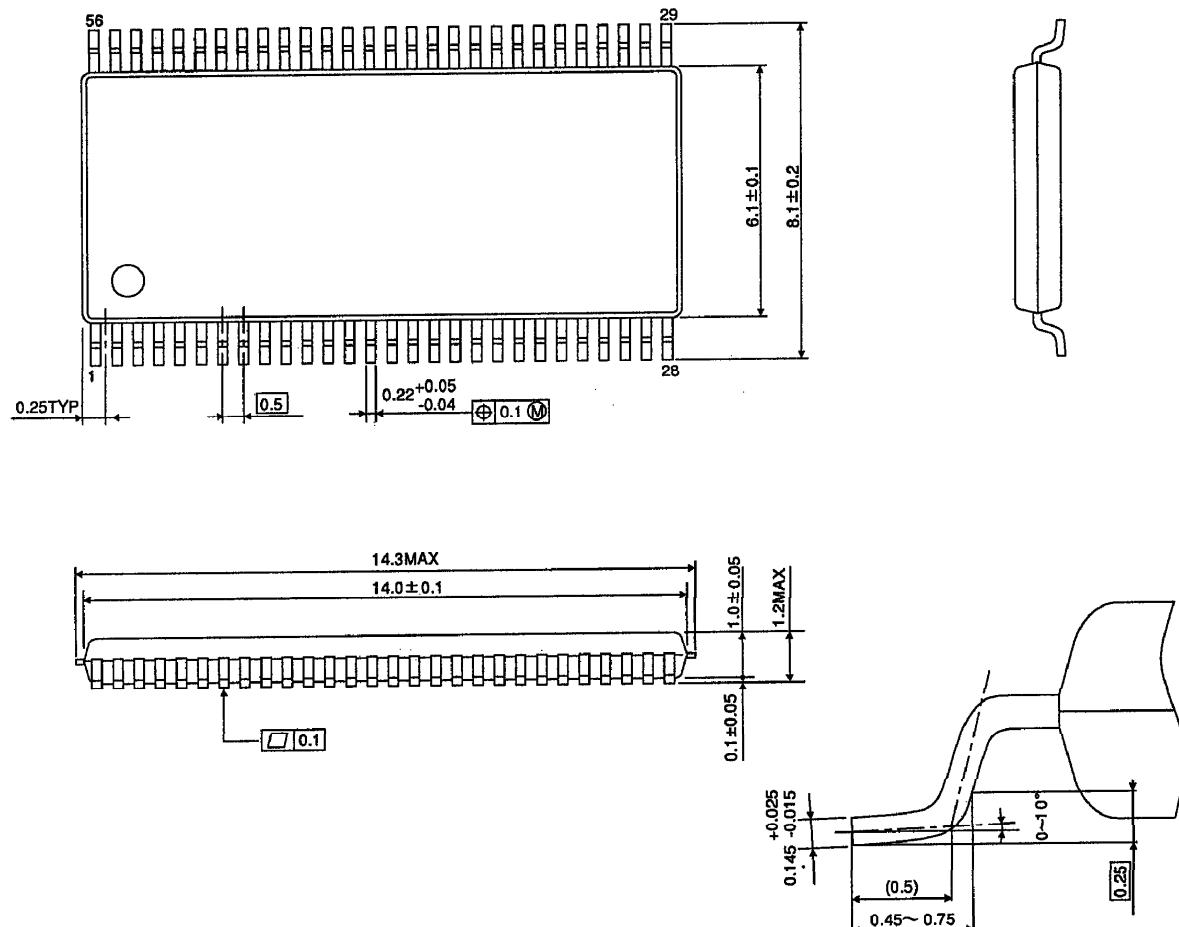


Fig.7 I/V Characteristics-Pulldown

PACKAGE DIMENSIONS

TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)