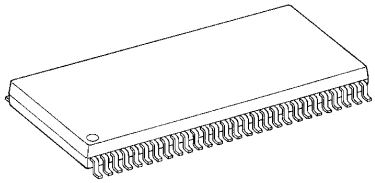
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX162835FT

LOW-VOLTAGE 18-BIT UNIVERSAL BUS DRIVER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCX162835FT is a high performance CMOS 18-bit UNIVERSAL BUS DRIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.
Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch / flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.
The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25 g (Typ.)

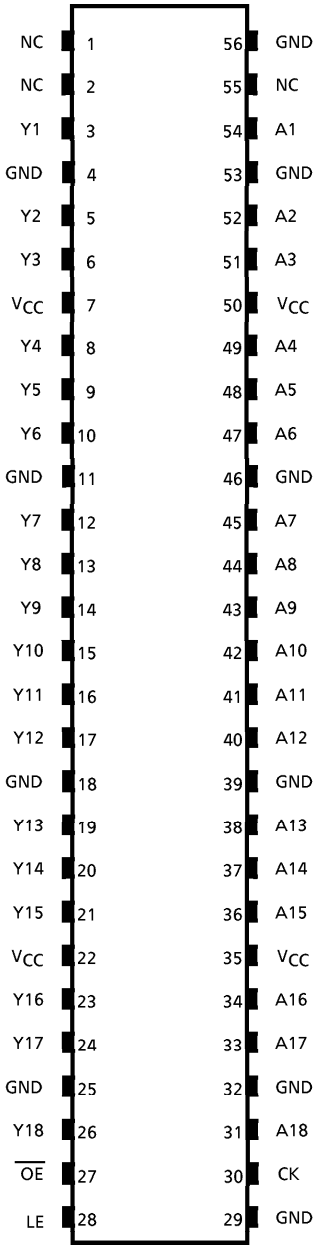
FEATURES

- 26-Ω Series Resistors on Outputs.
- Low Voltage Operation : V_{CC} = 1.8~3.6 V
- High Speed Operation : t_{pd} = 3.9 ns (max) at V_{CC} = 3.0~3.6 V
  : t_{pd} = 5.0 ns (max) at V_{CC} = 2.3~2.7 V
  : t_{pd} = 9.8 ns (max) at V_{CC} = 1.8 V
- 3.6 V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±12 mA (min) at V_{CC} = 3.0 V
  : I_{OH} / I_{OL} = ±8 mA (min) at V_{CC} = 2.3 V
  : I_{OH} / I_{OL} = ±4 mA (min) at V_{CC} = 1.8 V
- Latch-up Performance : ±300mA
- ESD Performance : Human Body Model > ±2000 V
  : Machine Model > ±200 V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) : To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

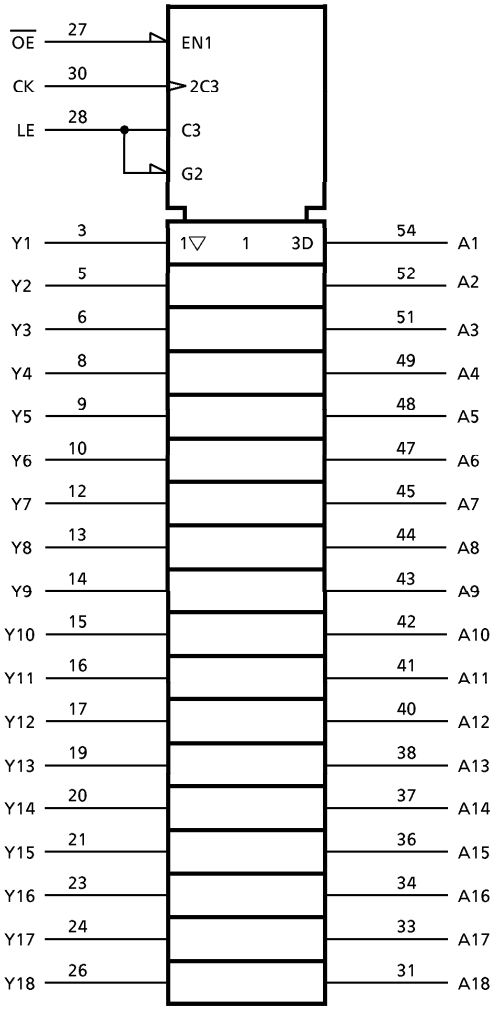
980910EBA2

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL

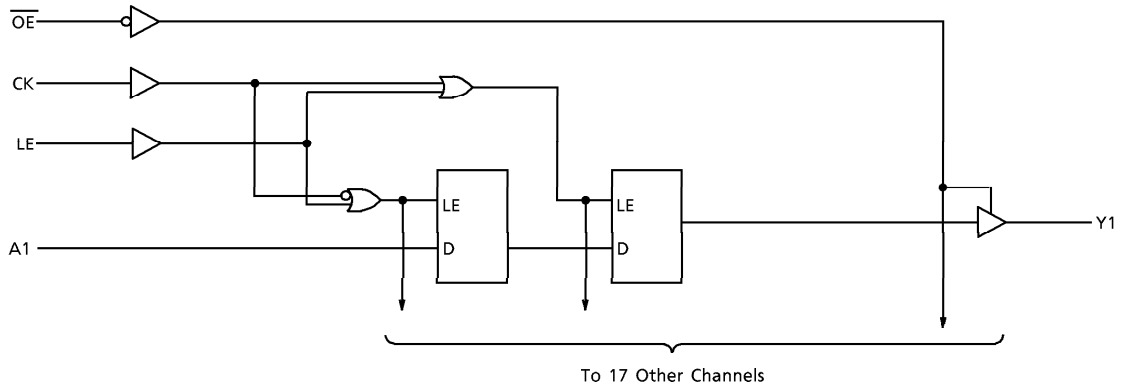


TRUTH TABLE

INPUTS				OUTPUTS
$\overline{OE}$	LE	CK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y0 *
L	L	L	X	Y0 *

* Output level before the indicated steady-state input conditions were established, provided that CK was high or low before LE went low.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	−0.5~4.6	V
DC Input Voltage	V_{IN}	−0.5~4.6	V
DC Output Voltage	V_{OUT}	−0.5~4.6 (Note 2)	V
		−0.5~V_{CC} + 0.5 (Note 3)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 4)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 2) : Off-State
(Note 3) : High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 4) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 5)	
Input Voltage	V_{IN}	−0.3~3.6	V
Output Voltage	$V_{I/O}$	0~3.6 (Note 6)	V
		0~V_{CC} (Note 7)	
Output Current	I_{OH} / I_{OL}	±12 (Note 8)	mA
		±8 (Note 9)	
		±4 (Note 10)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 11)	ns / V

(Note 5) : Data Retention Only
(Note 6) : Off-State
(Note 7) : High or Low State
(Note 8) : V_{CC} = 3.0~3.6 V
(Note 9) : V_{CC} = 2.3~2.7 V
(Note 10) : V_{CC} = 1.8 V
(Note 11) : V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 2.7 V < V_{CC} ≦ 3.6 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7~3.6	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	2.7	2.2	—	
				I_{OH} = −8 mA	3.0	2.4	—	
				I_{OH} = −12 mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	
				I_{OL} = 6 mA	2.7	—	0.4	
				I_{OL} = 8 mA	3.0	—	0.55	
				I_{OL} = 12 mA	3.0	—	0.8	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.7~3.6	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		2.7~3.6	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.7~3.6	—	±20.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7~3.6	—	750	μA

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.3~2.7	1.6	—	V
	"L" Level	V_{IL}			2.3~2.7	—	0.7	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.3~2.7	V_{CC} − 0.2	—	V
				I_{OH} = −4 mA	2.3	2.0	—	
				I_{OH} = −6 mA	2.3	1.8	—	
				I_{OH} = −8 mA	2.3	1.7	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3~2.7	—	0.2	
				I_{OL} = 6 mA	2.3	—	0.4	
				I_{OL} = 8 mA	2.3	—	0.6	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		2.3~2.7	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		2.3~2.7	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.3~2.7	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.3~2.7	—	±20.0	

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C, 1.8 V ≦ V_{CC} < 2.3 V)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			1.8~2.3	0.7 × V_{CC}	—	V
	"L" Level	V_{IL}			1.8~2.3	—	0.2 × V_{CC}	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	1.8	V_{CC} − 0.2	—	V
				I_{OH} = −4 mA	1.8	1.4	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	
				I_{OL} = 4 mA	1.8	—	0.3	
Input Leakage Current		I_{IN}	V_{IN} = 0~3.6 V		1.8	—	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~3.6 V		1.8	—	±10.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}, V_{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA
			V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		1.8	—	±20.0	

AC characteristics (Ta = −40~85°C, Input $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	(Fig.1, 3)	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (An-Yn)	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.0	
			3.3 ± 0.3	0.6	3.9	
Propagation Delay Time (CK-Yn)	t_{pLH} t_{pHL}	(Fig.1, 3)	1.8	2.0	9.2	ns
			2.5 ± 0.2	1.5	5.2	
			3.3 ± 0.3	1.4	4.2	
Propagation Delay Time (LE-Yn)	t_{pLH} t_{pHL}	(Fig.1, 4)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.7	
Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 5)	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 5)	1.8	1.5	7.9	ns
			2.5 ± 0.2	0.8	4.7	
			3.3 ± 0.3	0.6	4.2	
Minimum Pulse Width	t_w (H) t_w (L)	(Fig.1, 3, 4)	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time (An-CK, An-LE)	t_s	(Fig.1, 3, 4)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Hold Time (An-CK, An-LE)	t_h	(Fig.1, 3, 4)	1.8	1.0	—	ns
			2.5 ± 0.2	0.7	—	
			3.3 ± 0.3	0.7	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 12)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

(Note 12) : Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

AC characteristics (Ta = 0~85°C, Input $t_r = t_f$ = 2.0 ns, C_L = 0 pF, R_L = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Propagation Delay Time (An-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 2)	3.3 ± 0.15	0.9	2.0	ns
Propagation Delay Time (CK-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 3)	3.3 ± 0.15	1.4	2.9	ns
Propagation Delay Time (LE-Yn) (Note 13)	t_{pLH} t_{pHL}	(Fig.1, 4)	3.3 ± 0.15	0.7	3.4	ns
Output Enable Time (Note 13)	t_{pZL} t_{pZH}	(Fig.1, 5)	3.3 ± 0.15	0.7	3.0	ns
Output Disable Time (Note 13)	t_{pLZ} t_{pHZ}	(Fig.1, 5)	3.3 ± 0.15	0.7	2.9	ns
Minimum Set-up Time (An-CK, An-LE) (Note 13)	t_s	(Fig.1, 3, 4)	3.3 ± 0.15	1.5	—	ns
Minimum Hold Time (An-CK, An-LE) (Note 13)	t_h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7	—	ns

(Note 13) : TOSHIBA SPICE simulation data.

AC characteristics (Ta = 0~85°C, Input $t_r = t_f$ = 2.0 ns, C_L = 50 pF, R_L = 500 Ω)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Propagation Delay Time (An-Yn)	t_{pLH} t_{pHL}	(Fig.1, 2)	3.3 ± 0.15	1.0	4.2	ns
Propagation Delay Time (CK-Yn)	t_{pLH} t_{pHL}	(Fig.1, 3)	3.3 ± 0.15	1.9	4.5	ns
Propagation Delay Time (LE-Yn)	t_{pLH} t_{pHL}	(Fig.1, 4)	3.3 ± 0.15	1.0	5.0	ns
Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 5)	3.3 ± 0.15	1.0	4.6	ns
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 5)	3.3 ± 0.15	1.0	4.5	ns
Minimum Set-up Time (An-CK, An-LE)	t_s	(Fig.1, 3, 4)	3.3 ± 0.15	1.5	—	ns
Minimum Hold Time (An-CK, An-LE)	t_h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7	—	ns

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f$ = 2.0 ns, C_L = 30 pF)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 14)	1.8	0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 14)	2.5	0.35	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 14)	3.3	0.45	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 14)	1.8	−0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 14)	2.5	−0.35	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 14)	3.3	−0.45	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note 14)	1.8	1.35	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note 14)	2.5	1.85	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note 14)	3.3	2.45	

(Note 14) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

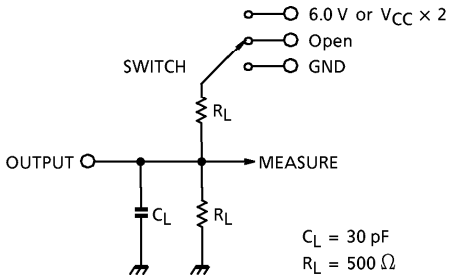
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Input Capacitance	C_{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	$C_{I/O}$		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10 MHz (Note 15)	1.8, 2.5, 3.3	20	pF

(Note 15) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 18 \text{ (per bit)}$$

TEST CIRCUIT

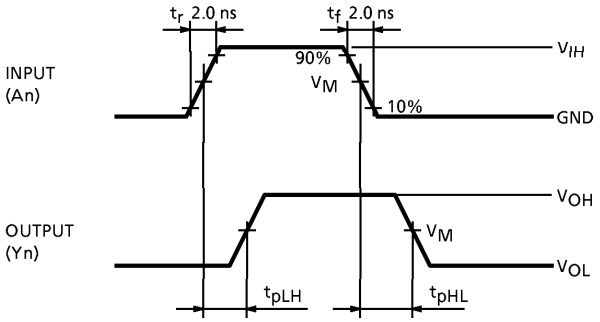
Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @V_{CC} = 3.3 ± 0.3 V V_{CC} x 2 @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}



SYMBOL	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Fig.3 t_{pLH}, t_{pHL}, t_w, t_s, t_h

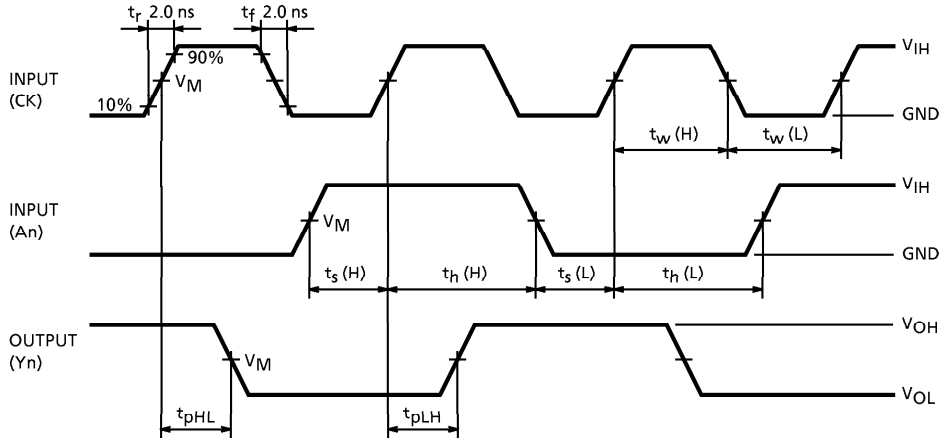


Fig.4 t_{pLH}, t_{pHL}, t_w, t_s, t_h

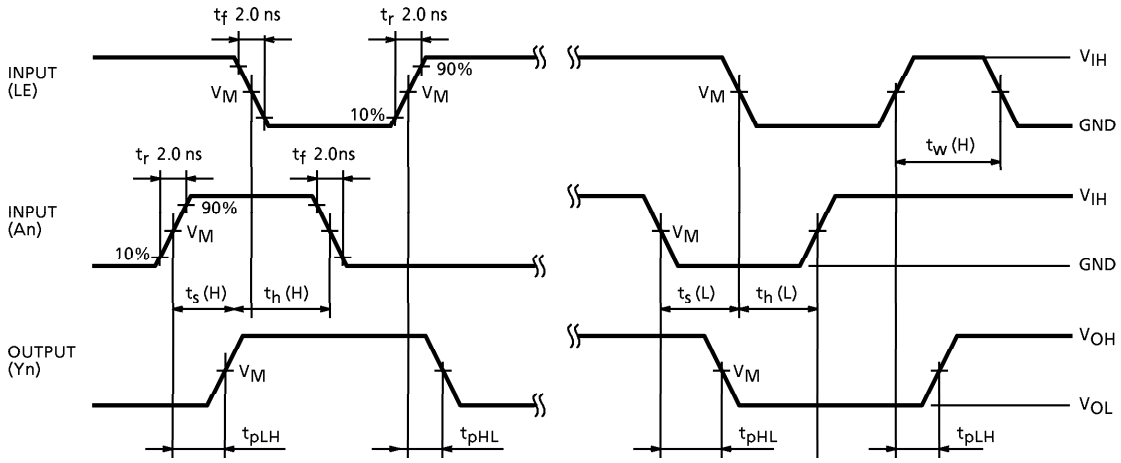
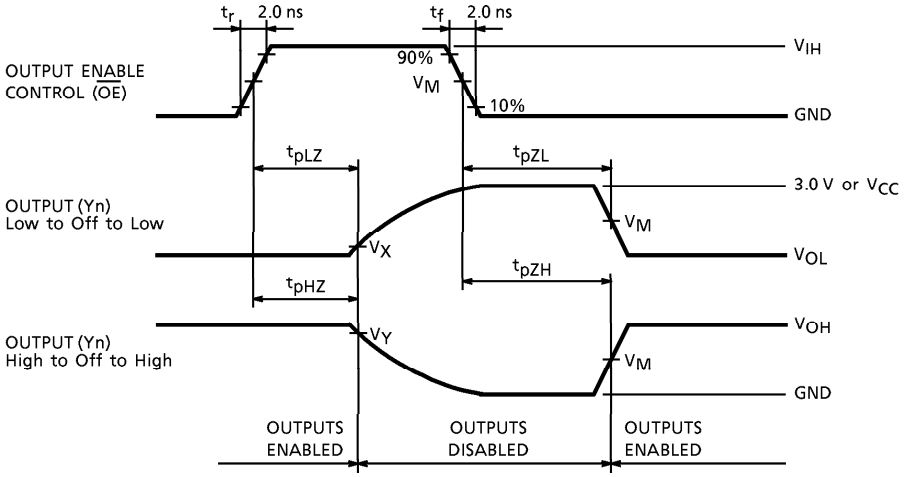


Fig.5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



IBIS CHARACTERISTICS (Typ.)

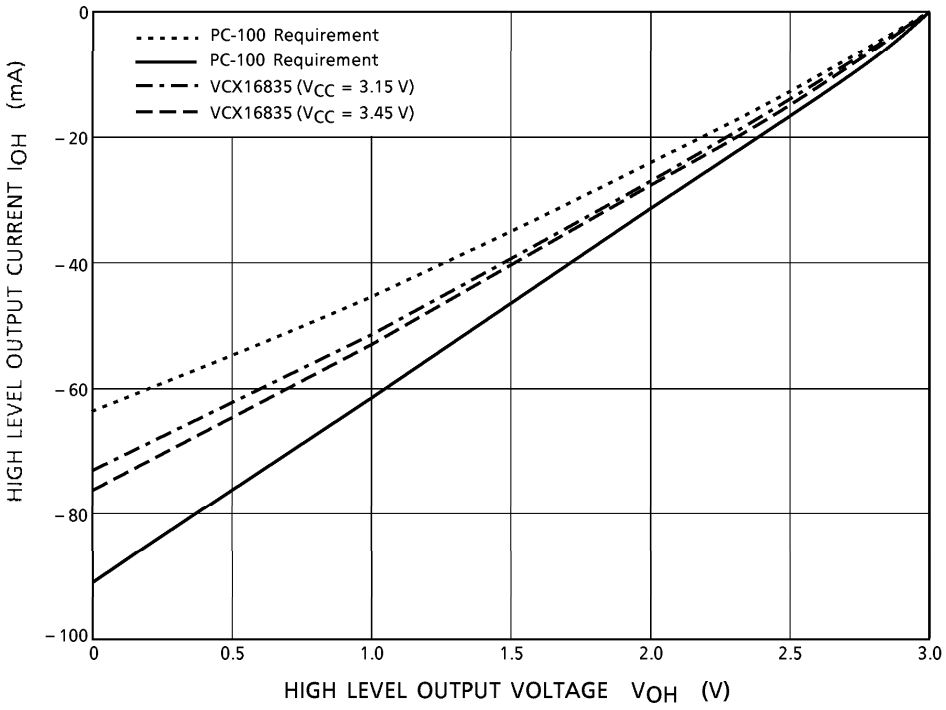


Fig.6 I / V Characteristics-Pullup

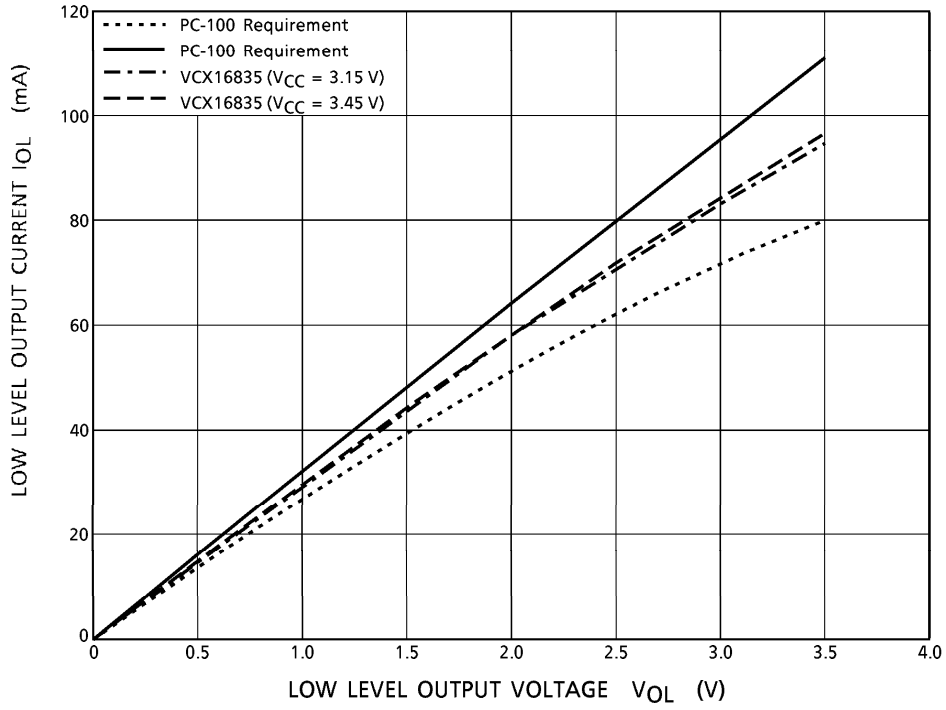
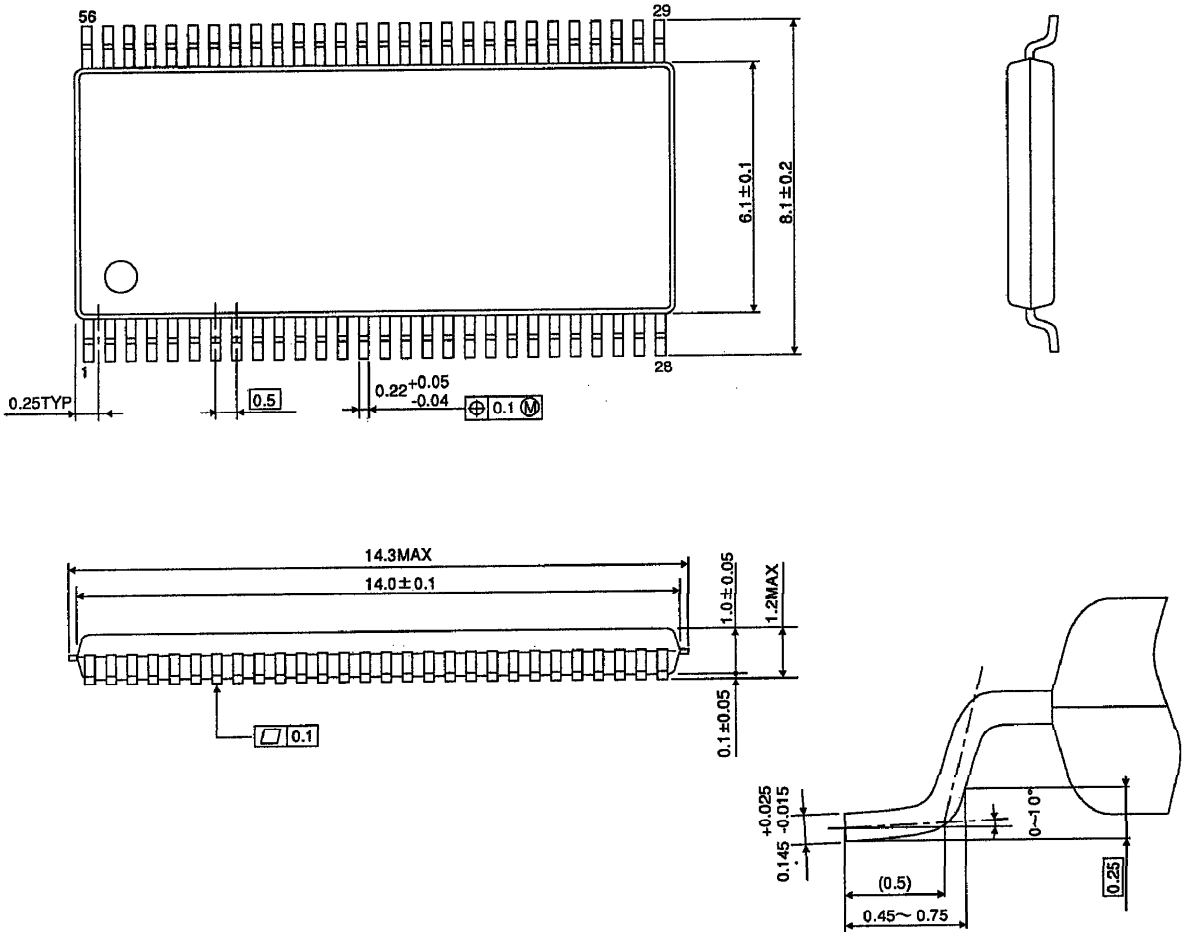


Fig.7 I / V Characteristics-Pulldown

PACKAGE DIMENSIONS

TSSOP56-P-0061-0.50 Unit : mm



Weight : 0.25 g (Typ.)