07/07/99

Errata: CS8420-CS Rev. B Performance Update

(Reference CS8420 Data Sheet revision DS245PP1 dated Oct '98)

In this text 'register' refers to the control port register file described on pages 27-40 of the datasheet.

1. Performance characteristics are specified with VA and VD at 5V plus or minus 5%.

2. Power consumption at 48 kHz Fsi and Fso is typically 375 mW. Power consumption at 96 kHz Fsi and Fso is typically 725 mW.

3. In power down mode, the analog power consumption is 1.25 mW, and the digital power consumption is 6.8 mW.

4. The /RST and H/S inputs have 14 uA of leakage current, which exceeds the 10 uA specification in the data sheet.

5. More reliable operation of the PLL can be achieved by meeting the following conditions:
   a. Use the fast filter components recommended on page 18 of the data sheet.
   b. Connect a 3 Meg ohm resistor from the FILT pin to AGND.
   c. Write the following values to the specified registers of the control port in the order given:

Register #	Value
0	10011001
81	01000000

   The receiver will not lock to input sampling rates lower than 32 kHz, as this requires the 'slow' or 'medium' filter components. The software data flow modes affected are shown in figures 5, 6, 7, 8, 9, and 10 of the datasheet. The hardware modes affected are 1, 3, 4, and 5.

   Note: these conditions are unnecessary when using ONLY the input serial port to generate the input time base and supply data to the part.

6. The falling edge of SCLK is used to latch the data in the left justified and AES3 serial formats of the hardware modes. Rev. C parts will use the rising edge and the data sheet will be modified to reflect the change.

7. In hardware modes 1, 3, and 4 the Validity bit affects the state of the RERR output. For the Rev. C part this will not occur and the data sheet will be modified to reflect the change.

8. The cycle-to-cycle jitter performance of the CS8420 is as good as the CS8412's. The time deviation jitter performance which is the integral of the cycle-to-cycle performance will cause the SRC to intermittently indicate that it is tracking a vari-speed event (gradual slew of the input or output time base) by setting the REUNLOCK interrupt bit. This interrupt can be ignored or left masked since the jitter has very little effect on the final audio data output of the part.

9. Some register bits need to be set through the control port to enable vari-speed operation. The consequence is that vari-speed is not available in the hardware modes that use the SRC (modes 1, 2, and 3). To enable vari-speed, the following data values have to be written to the following registers in the order specified:

Register #	Value
0	10011001
86	00000010

10. An IEC60958 stream in Professional mode uses bits 0, 1, and 2 of byte 2 to encode the use of the auxiliary sample bits. It uses bits 3, 4, and 5 of byte 2 to indicate the length of the audio word. In Consumer mode, bit 0 of byte 4 indicates whether maximum sample word length is 20 bits or 24 bits. Bits 1, 2, and 3 then indicate the maximum word length relative to 20 or 24 bits. The AES receiver logic that decodes these channel status bits to produce the AUX[3:0] bits of register 15 has a bug. The bug results in the max 20 bit audio/20 bit source word length case of channel status being incorrectly decoded as AUX[3:0]=0000. The correct decoding for this case is AUX[3:0]=0100.

11. When the previously mentioned AUX[3:0] field has non-zero length, the AES receiver replaces the AUX field portion of the audio data with zeros, effectively doing truncation. It then sends the resulting 24 bit data to the block (SRC, output serial port, AES transmitter) that it is connected to. The datasheet says that this truncation will only be done on input to the SRC.

12. It is possible that an AES source may set the pro or consumer AUX field inappropriately. Then the CS8420 receiver will truncate the received audio data without the user having any control. This is most likely for older equipment made before the changes to the AES standard that defined an AUX field for consumer mode. Such older equipment most likely sets the field to all zeros, which the CS8420 interprets as 20 bits of data according to the new AES standards. This situation happens for the default setting of the Audio Precision System 2 for consumer mode. This will cause the output from the CS8420 to have a THD+N of no better than -122 dB.

13. In Transmitter Mono Mode, right channel data appears on consecutive sub-frame outputs instead of left channel data when MMTLR=0. Left channel data instead of right channel data appears when MMTLR=1.

14. Two-byte mode access of the Channel Status and User buffers works only in the auto-increment mode of the SPI or I2C port. The auto-increment feature, however, is unreliable reading in both one and two byte modes. To reliably read the Channel status and User buffers, the MAP should be written before each read. The auto-increment mode has no problem when writing or when reading the control registers.

15. Access to the User Buffer does not default to the two-byte mode. To read the U buffer in two-byte mode, the Channel Status buffer must be set to two-byte mode.

16. The AES transmitter does not satisfy items b and c of p. 20 of the datasheet, i.e. the phase of AES TX output when TCBL is an output is uncontrolled.

17. The PLL bypass mode with the AES receiver still active, RXD[1:0]=2'b11 in register 4, is being removed from the data sheet. It is now a reserved mode.

18. The RSTB input lacks sufficient hysteresis to be used with an external RC reset network. A slowly rising RSTB input may cause misinterpretation of the desired settings indicated by any 47K pull-up/pull-down resistors.

19. The rev code (VER[3:0] of register #127) has not been updated to Rev B.

20. The Mono mode of the receiver only works if the Run bit is set in register 4 before the MMR bit is set in register 2.

21. The maximum frequency of the CCLK in the SPI control port mode is 6 MHz.

22. The Confidence bit in the Receiver Error register does not reliably indicate the described error condition.

23. The TSLIP and OSLIP interrupts do not work correctly.

24. The SRC may clip under certain conditions when a signal greater than -0.03 dBFS input is applied. Toggling the RUN bit, or in hardware mode, resetting the part after the clocks have settled, will stop the clipping.

25. The output current from TXP and TXN is 21 mA instead of the 30 mA indicated in the data sheet.

26. IEC Mode 1 of the U buffer outputs all zeros for data instead of the received U data. IEC Mode 2 works and may be used as a substitute for Mode 1. See Register 19 on page 39.

If there are any questions concerning this information,
Please contact: Stuart Dudley Dimond III 512.912.3621