FM3204/16/64/256

Integrated Processor Companion with Memory

Features

High Integration Device Replaces Multiple Parts
- Serial Nonvolatile Memory
- Low VDD Reset
- Watchdog Timer
- Voltage Comparator/NMI
- Event Counters
- Serial Number with Write-lock for Security

Processor Companion
- Active-low Reset Output for VDD and Watchdog
- Programmable Low VDD Reset Thresholds
- Manual Reset Filtered and De-bounced
- Programmable Watchdog Timer
- Dual Battery-backed Event Counter Tracks System Intrusions or other Events
- Comparator for Power-fail Interrupt or Other Use
- 64-bit Programmable Serial Number with Lock

Ferroelectric Nonvolatile RAM
- 4Kb, 16Kb, 64Kb, and 256Kb versions
- Unlimited Read/Write Endurance
- 10 year Data Retention
- NoDelay™ Writes

Fast Two-wire Serial Interface
- Up to 1 MHz Maximum Bus Frequency
- Supports Legacy Timing for 100 kHz & 400 kHz
- Device Select Pins for up to 4 Memory Devices
- Supervisor Controlled via 2-wire Interface

Easy to Use Configurations
- Operates from 2.7 to 5.5V
- Small Footprint 14-pin SOIC (-S)
  - "Green" 14-pin SOIC (-G)
- Pin Compatible with FM31xx Series
- Low Operating Current, 150µA Standby Current
- -40°C to +85°C Operation

Description

The FM32xx is a family of integrated devices that include the most commonly needed functions for processor-based systems. Major features include nonvolatile memory available in various sizes, low-VDD reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or other purpose. The family operates from 2.7 to 5.5V.

The FM32xx family is software and pinout compatible with the FM31xx family which also includes a real-time clock. The common features allow a system design that easily can be assembled with or without timekeeping by simply selecting the FM31xx or FM32xx, respectively.

Each FM32xx provides nonvolatile RAM available in sizes including 4Kb, 16Kb, 64Kb, and 256Kb versions. Fast write speed and unlimited endurance allow the memory to serve as extra RAM or conventional nonvolatile storage. This memory is truly nonvolatile rather than battery backed.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low VDD condition or a watchdog timeout. /RST goes active when VDD drops below a programmable threshold and remains active for 100 ms after VDD rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A general-purpose comparator compares an external input pin to the onboard 1.2V reference. This is useful for generating an early warning power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable.

Additionally the FM32xx offers a dual event counter that tracks the number of rising or falling edges detected on dedicated input pins. The counter can optionally be battery backed and even battery operated by attaching a backup power source to the VBAK pin. If VBAK is connected to a battery or capacitor, then events will be counted even in the absence of VDD.

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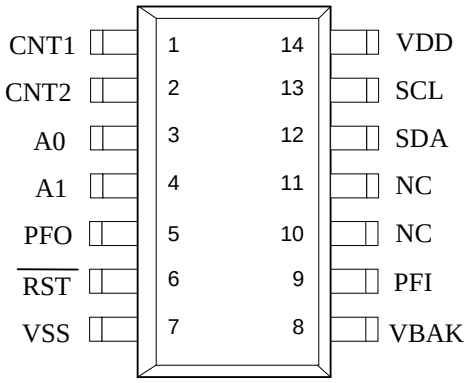
Pin Configuration



Pin Name	Function
CNT1, CNT2	Event Counter Inputs
A0, A1	Device Select Inputs
PFO	Early Power-fail Output
/RST	Reset Input/Output
PFI	Early Power-fail Input
SDA	Serial Data
SCL	Serial Clock
VBAK	Battery-Backup Supply
VDD	Supply Voltage

Ordering Information				
Base Configuration	Memory Size	Operating Voltage	Reset Threshold	Ordering Part Number
FM32256	256Kb	2.7-5.5V	2.6V, 2.9, 3.9, 4.4V	FM32256-S
				FM32256-G
FM3264	64Kb	2.7-5.5V	2.6V, 2.9, 3.9, 4.4V	FM3264-S
				FM3264-G
FM3216	16Kb	2.7-5.5V	2.6V, 2.9, 3.9, 4.4V	FM3216-S
				FM3216-G
FM3204	4Kb	2.7-5.5V	2.6V, 2.9, 3.9, 4.4V	FM3204-S
				FM3204-G

Other memory configurations may be available. Please contact the factory for more information.

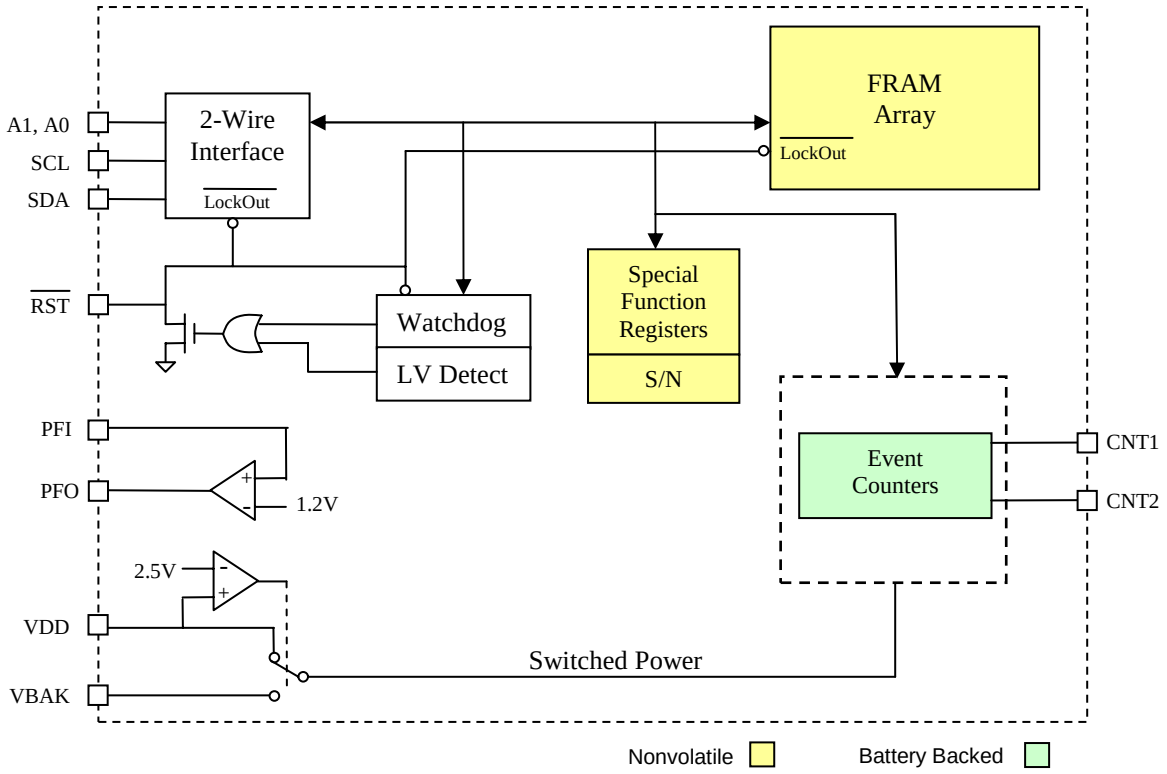


Figure 1. Block Diagram

Pin Descriptions

Pin Name	Type	Pin Description
A0, A1	Input	Device select inputs are used to address multiple memories on a serial bus. To select the device the address value on the two pins must match the corresponding bits contained in the device address. The device select pins are pulled down internally.
CNT1, CNT2	Input	Event Counter Inputs: These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable.
PFO	Output	Power Fail Output: This is the early power-fail output.
/RST	I/O	Active low reset output with weak pull-up. Also input for manual reset.
SDA	I/O	Serial Data & Address: This is a bi-directional line for the two-wire interface. It is open-drain and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. A pull-up resistor is required.
SCL	Input	Serial Clock: The serial clock line for the two-wire interface. Data is clocked out of the part on the falling edge, and in on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
PFI	Input	Early Power-fail Input: Typically connected to an unregulated power supply to detect an early power failure. This pin should not be left floating.
VBAK	Supply	Backup supply voltage: A 3V battery or a large value capacitor. If V_{DD}<3.6V and no backup supply is used, this pin should be tied to V_{DD}. If V_{DD}>3.6V and no backup supply is used, this pin should be left floating and the VBC bit should be set.
VDD	Supply	Supply Voltage.
VSS	Supply	Ground

Overview

The FM32xx family combines a serial nonvolatile RAM with a processor companion. The companion is a highly integrated peripheral including a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM32xx integrates these complementary but distinct functions that share a common interface in a single package. Although monolithic, the product is organized as two logical devices, the FRAM memory and the companion. From the system perspective they appear to be two separate devices with unique IDs on the serial bus.

The FM32xx provides the same functions as the FM31xx with the exception of the real-time clock. This makes it easy to develop a common design that can either include timekeeping by using the FM31xx or exclude it by using the FM32xx. All other features are identical. The register address map is even preserved so that software can be identical.

The memory is organized as a stand-alone 2-wire nonvolatile memory with a standard device ID value. The companion functions are accessed under their own 2-wire device ID. This allows the companion functions to be read while maintaining the most recently used memory address. The companion functions are controlled by 16 special function registers. The event counter circuits and related registers are maintained by the power source on the VBAK pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Operation

The FM32xx is a family of products available in different memory sizes including 4Kb, 16Kb, 64Kb, and 256Kb. The family is software compatible, all versions use consistent two-byte addressing for the memory device. This makes the lowest density device different from its stand-alone memory counterparts but makes them compatible within the entire family.

Memory is organized in bytes, for example the 4Kb memory is 512 x 8 and the 256Kb memory is 32,768 x 8. The memory is based on FRAM technology. Therefore it can be treated as RAM and is read or written at the speed of the two-wire bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The 2-wire interface protocol is described further on page 11.

The memory array can be write-protected by software. Two bits in the processor companion area (WP0, WP1 in register 0Bh) control the protection setting as shown in the following table. Based on the setting, the protected addresses cannot be written and the 2-wire interface will not acknowledge any data to protected addresses. The special function registers containing these bits are described in detail below.

Write protect addresses	WP1	WP0
None	0	0
Bottom 1/4	0	1
Bottom 1/2	1	0
Full array	1	1

Processor Companion

In addition to nonvolatile RAM, the FM32xx family incorporates a highly integrated processor companion. It includes a low voltage reset, a programmable watchdog timer, battery-backed event counters, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. All FM32xx devices have a reset pin (/RST) to drive the processor reset input during power faults (and power-up) and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the /RST pin. When V_{DD} is above the programmed trip point, /RST output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}) the /RST pin will be driven low. It will remain low until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, /RST will continue to drive low for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the /RST pin will return to the weak high state. While /RST is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

The bits VTP1 and VTP0 control the trip point of the low VDD reset. They are located in register 0Bh, bits 1 and 0. The figure below illustrates the reset operation in response to Low VDD.

VTP	VTP1	VTP0
2.6V	0	0
2.9V	0	1
3.9V	1	0
4.4V	1	1

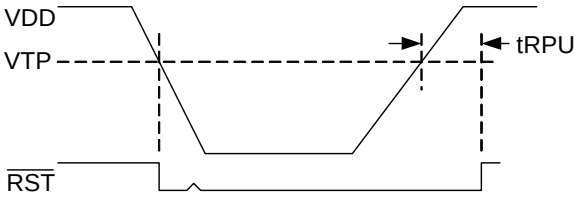


Figure 2. Low VDD Reset

The watchdog timer can also be used to assert the reset signal (/RST). The watchdog is a free running programmable timer. The period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must timeout in order to drive /RST active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If not enabled, the watchdog timer runs but has no effect on /RST. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4-0, and the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when V_{DD} is below V_{TP}. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog timeout	WDT4.0	0Ah, D4-0
Watchdog enable	WDE	0Ah, D7
Watchdog restart	WR3-0	09h, D3-0

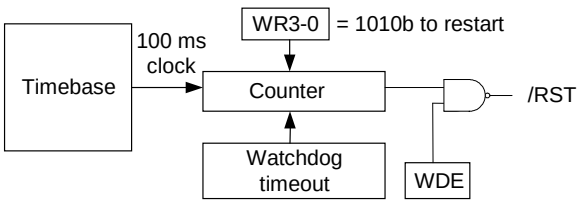


Figure 3 Watchdog Timer

Manual Reset

The /RST pin is bi-directional and allows the FM32xx to filter and de-bounce a manual reset switch. The /RST input detects an external low condition and responds by driving the /RST signal low for 100 ms.

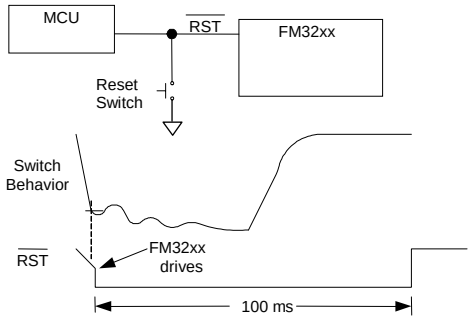


Figure 4 Manual Reset

Note that an internal weak pull-up on /RST eliminates the need for additional external components.

Reset Flags

In case of a reset condition, a flag will be set to indicate the source of the reset. A low V_{DD} reset is indicated by the POR flag, register 09h bit 6. A watchdog reset is indicated by the WTR flag, register 09h bit 7. A manual reset will result in no flag being set, so the absence of a flag is a manual reset. Note that the flags are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below. The voltage on the PFI input pin is compared to an onboard 1.2V reference. When the PFI input voltage drops below this threshold, the comparator will drive the PFO pin to a low state. The comparator has 350 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

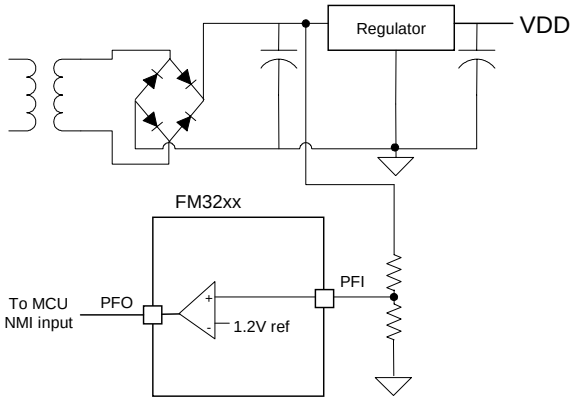


Figure 5. Comparator as a Power-fail Warning

The comparator is a general purpose device and its application is not limited to the NMI function.

Note: The maximum voltage on the comparator input PFI is limited to 3.75V under normal operating conditions.

Event Counter

The FM32xx offers two battery-backed event counters. Input pins CNT1 and CNT2 are programmable edge detectors. Each clocks a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1 is located in registers 0Dh and 0Eh, Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime VDD is above VTP, and they will be incremented as long as a valid VBAK source is provided. To read, set the RC bit register 0Ch bit 3 to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode.

The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0; Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC bit 3.

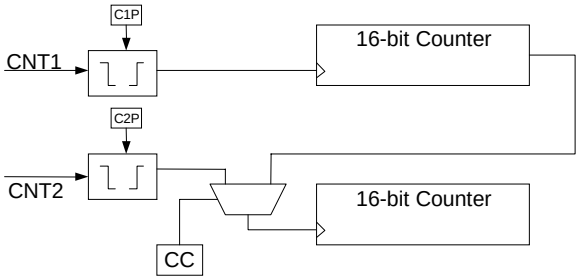


Figure 6. Event Counter

The VBAK pin provides an option to battery- or capacitor-back the event counters. As long as a voltage source is supplied on VBAK, the counters will respond to CNT edges and maintain their count values regardless of VDD.

Serial Number

A 64-bit serial number area is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via the device ID for the processor companion. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However once the lock bit is set the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL, register 0Bh bit 7. Setting the SNL bit to a 1 disables writes to the serial number registers, and the SNL bit cannot be cleared.

Backup Power

The event counters and some watchdog settings are retained by a backup power source. When the primary system power fails, the voltage on the VDD pin will drop. When VDD drops below 2.5V, power to the event counters and watchdog settings will switch to the backup power supply on VBAK.

Trickle Charger

To facilitate capacitor backup, the VBAK pin can optionally provide a trickle charge current. When the VBC bit, register 0Bh bit 2, is set to 1 the VBAK pin will source approximately 4 µA until VBAK reaches VDD or 3.75V whichever is less. In 3V systems this charges the capacitor to VDD without an external diode and resistor charger. In 5V systems it provides the same convenience and also prevents the user from exceeding the VBAK maximum voltage specification.

Note: systems using lithium batteries should clear the VBC bit to 0 to prevent battery charging. The VBAK circuitry includes an internal 1 KΩ series resistor as a safety element.

Register Map

Register Map Summary Table

Nonvolatile = Battery-backed =

Address	Data D7	D6	D5	D4	D3	D2	D1	D0	Function	Range
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch	-	-	-	-	RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	-	-	WP1	WP0	VBC	VTP1	VTP0	Companion Control	
0Ah	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	-	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
00-08h	DO NOT USE								RESERVED	

The processor companion functions are accessed via 16 special function registers that are mapped to a separate 2-wire device ID. The interface protocol is described below. The registers contain control bits, or information flags. A description of each register follows.

**Note that the usable address range starts at address 09h to preserve software compatibility with the FM31xx device family, which includes a real-time clock in registers 00-08h.*

Register Description

Address Description

18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
	Byte 6 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
16h	**Serial Number Byte 5**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL=0, read-only when SNL=1. Nonvolatile.							

10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC=1. Battery-backed, read/write .							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1 MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							

0Ch	Event Counter Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	-	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to 1 takes a snapshot of the four counter bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared .							
CC	Counter Cascade. When CC=0, the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC=1, the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P has no effect when CC=1. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = 0, rising edges when C2P = 1. C2P has no effect when CC=1. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = 0, rising edges when C1P = 1. Battery-backed, read/write.							

0Bh	Companion Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	SNL	-	-	WP1	WP0	VBC	VTP1	VTP0
SNL	Serial Number Lock. Setting to a 1 makes registers 11h to 18h and SNL permanently read-only. **SNL cannot be cleared once set to 1.** Nonvolatile, read/write.							
WP1-0	Write Protect. These bits control the write protection of the memory array. Nonvolatile, read/write. Write protect addresses — WP1 — WP0 None — 0 — 0 Bottom 1/4 — 0 — 1 Bottom 1/2 — 1 — 0 Full array — 1 — 1							
VBC	VBAK Charger Control. Setting VBC to 1 causes a 4 µA trickle charge current to be supplied on VBAK. Clearing VBC to 0 disables the charge current. Nonvolatile, read/write.							
VTP1-0	VTP select. These bits control the reset trip point for the low VDD reset function. Nonvolatile, read/write. VTP — VTP1 — VTP0 2.6V — 0 — 0 2.9V — 0 — 1 3.9V — 1 — 0 4.4V — 1 — 1							

0Ah	Watchdog Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0
WDE	Watchdog Enable. When WDE=1 the watchdog timer can cause the /RST signal to go active. When WDE = 0 the timer runs but has no effect on /RST. Note as the timer is free-running, users should restart the timer using WR3-0 prior to setting WDE=1. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.							
WDT4-0	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR3-0. Nonvolatile, read/write. Watchdog timeout — WDT4 — WDT3 — WDT2 — WDT1 — WDT0 Invalid – default 100 ms — 0 — 0 — 0 — 0 — 0 100 ms — 0 — 0 — 0 — 0 — 1 200 ms — 0 — 0 — 0 — 1 — 0 300 ms — 0 — 0 — 0 — 1 — 1 ⋮ 2000 ms — 1 — 0 — 1 — 0 — 0 2100 ms — 1 — 0 — 1 — 0 — 1 2200 ms — 1 — 0 — 1 — 1 — 0 ⋮ 2900 ms — 1 — 1 — 1 — 0 — 1 3000 ms — 1 — 1 — 1 — 1 — 0 Disable count — 1 — 1 — 1 — 1 — 1							

09h	Watchdog Restart & Flags							
	D7	D6	D5	D4	D3	D2	D1	D0
	WTR	POR	LB	-	WR3	WR2	WR1	WR0
WTR	Watchdog Timer Reset Flag: When the /RST signal is activated by the watchdog the WTR bit will be set to 1. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can only clear this bit).							
POR	Power-on Reset Flag: When the /RST signal is activated by VDD < VTP, the POR bit will be set to 1. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can only clear this bit).							
LB	Low Backup Flag: On power up, if the VBAK source is below the minimum voltage to operate the event counters, this bit will be set to 1. The user should clear it to 0 when initializing the system. Battery-backed. Read/Write (internally set, user can only clear this bit).							
WR3-0	Watchdog Restart: Writing a pattern 1010b to WR3-0 restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR3-0 has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Write-only.							

00-08h	Reserved – DO NOT USE THIS ADDRESS SPACE

Two-wire Interface

The FM32xx employs an industry standard two-wire bus that is familiar to many users. This product is unique since it incorporates two logical devices in one chip. Each logical device can be accessed individually. Although monolithic, it appears to the system software to be two separate products. One is a memory device. It has a Slave Address (Slave ID = 1010b) that operates the same as a stand-alone memory device. The second device is a processor companion which has a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM32xx is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions: Start, Stop, Data bit, and Acknowledge. The figure below illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications.

Start Condition

A Start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All read and write transactions begin with a Start condition. An operation in progress can be aborted by asserting a Start condition at any time. Aborting an operation using the Start condition will ready the FM32xx for a new operation.

If the power supply drops below the specified VTP during operation, any 2-wire transaction in progress will be aborted and the system must issue a Start condition prior to performing another operation.

Stop Condition

A Stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations must end with a Stop condition. If an operation is pending when a stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a Stop condition.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high.

Acknowledge

The Acknowledge (ACK) takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter must release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a No-Acknowledge (NACK) and the operation is aborted.

The receiver might NACK for two distinct reasons. First is that a byte transfer fails. In this case, the NACK ends the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not send an ACK to deliberately terminate an operation. For example, during a read operation, the FM32xx will continue to place data onto the bus as long as the receiver sends ACKs (and clocks). When a read operation is complete and no more data is needed, the receiver must NACK the last byte. If the receiver ACKs the last byte, this will cause the FM32xx to attempt to drive the bus on the next clock while the master is sending a new command such as a Stop.

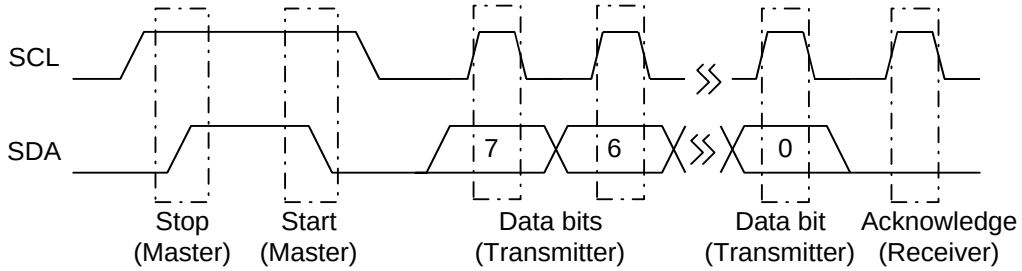


Figure 7. Data Transfer Protocol

Slave Address

The first byte that the FM32xx expects after a Start condition is the slave address. The slave address contains the Slave ID, Device Select address, and a bit that specifies if the transaction is a read or a write. The FM32xx has two Slave Addresses (Slave IDs) associated with two logical devices. To access the memory device, bits 7-4 should be set to 1010b. The other logical device within the FM32xx is the Companion. To access this device, bits 7-4 of the slave address should be set to 1101b. A bus transaction with this slave address will not affect the memory in any way. The figures below illustrate the two Slave Addresses.

The Device Select bits allow multiple devices of the same type to reside on the 2-wire bus. The device select bits (bits 2-1) select one of four parts on a two-wire bus. They must match the corresponding value on the external address pins in order to select the device. Bit 0 is the read/write bit. A "1" indicates a read operation, and a "0" indicates a write operation.

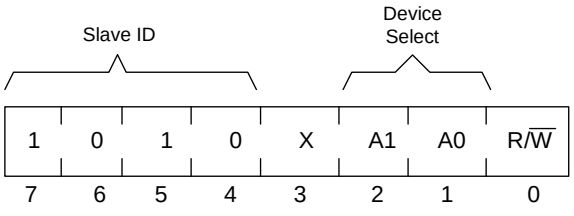


Figure 8. Slave Address - Memory

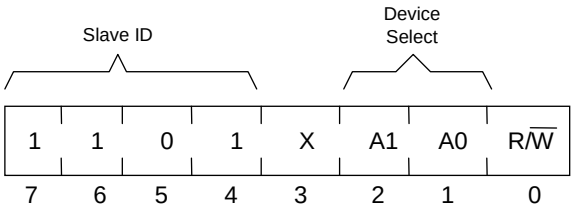


Figure 9. Slave Address – Companion

Addressing Overview – Memory

After the FM32xx acknowledges the Slave Address, the master can place the memory address on the bus for a write operation. The address requires two bytes. This is true for all members of the family. Therefore the 4Kb and 16Kb configurations will be addressed differently from stand alone serial memories but the entire family will be upwardly compatible with no software changes.

The first is the MSB (upper byte). For a given density unused address bits are don't cares, but should be set to 0 to maintain upward compatibility. Following the MSB is the LSB (lower byte) which contains the remaining eight address bits. The address is latched internally. Each access causes the latched address to be incremented automatically. The current address is the value that is held in the latch, either a newly written value or the address following the last access. The current address will be held as long as VDD > VTP or until a new value is written. Accesses to the Companion do not affect the current memory address. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the Acknowledge, the FM32xx increments the internal address. This allows the next sequential byte to be accessed with no additional addressing externally. After the last address is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Addressing Overview – Companion

The Processor Companion operates in a similar manner to the memory, except that it uses only one byte of address. Addresses 09h to 18h correspond to special function registers. Attempting to load addresses outside this range is an illegal condition; the FM32xx will return a NACK and abort the 2-wire transaction. Note the address block begins at 09h to maintain software compatibility with the FM31xx family where the real-time clock starts at 00h.

Data Transfer

After the address information has been transmitted, data transfer between the bus master and the FM32xx begins. For a read, the FM32xx will place 8 data bits on the bus then wait for an ACK from the master. If the ACK occurs, the FM32xx will transfer the next byte. If the ACK is not sent, the FM32xx will end the read operation. For a write operation, the FM32xx will accept 8 data bits from the master then send an Acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Write Operation

All memory writes begin with a Slave Address, then a memory address. The bus master indicates a write operation by setting the slave address LSB to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an Acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap to 0000h. Internally, the actual memory write occurs after the 8th data bit is transferred. It will be complete before the Acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using a Start or Stop condition prior to the 8th data bit. The figures below illustrate a single- and multiple-writes to memory.

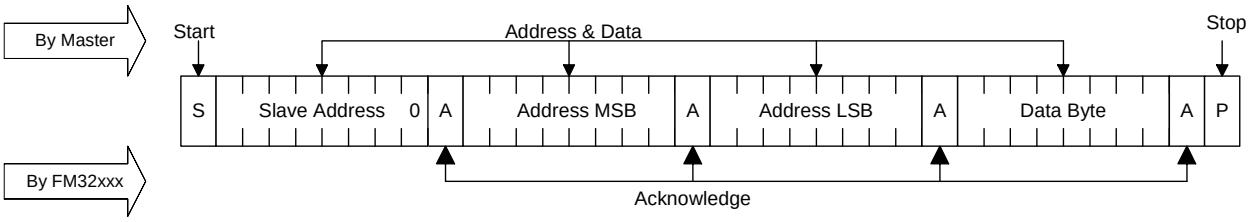


Figure 10. Single Byte Memory Write

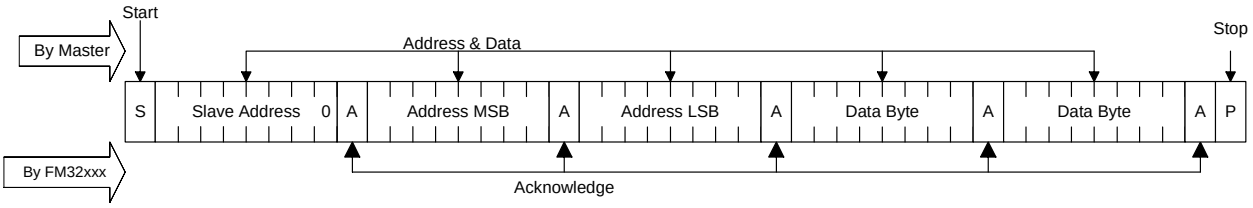


Figure 11. Multiple Byte Memory Write

Memory Read Operation

There are two types of memory read operations. They are current address read and selective address read. In a current address read, the FM32xx uses the internal address latch to supply the address. In a selective read, the user performs a procedure to first set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM32xx uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete device address, the FM32xx will begin shifting data out from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Each time the bus master acknowledges a byte, this indicates that the FM32xx should read out the next sequential byte.

There are four ways to terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM32xx attempts to read out additional data onto the bus. The four valid methods follow.

1. The bus master issues a NACK in the 9th clock cycle and a Stop in the 10th clock cycle. This is illustrated in the diagrams below and is preferred.
2. The bus master issues a NACK in the 9th clock cycle and a Start in the 10th.
3. The bus master issues a Stop in the 9th clock cycle.
4. The bus master issues a Start in the 9th clock cycle.

If the internal address reaches the top of memory, it will wrap around to 0000h on the next read cycle. The figures below show the proper operation for current address reads.

Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM32xx acknowledges the address, the bus master issues a Start condition. This simultaneously aborts the write operation and allows the read command to

be issued with the slave address LSB set to a 1. The operation is now a read from the current address. Read operations are illustrated below.

Companion Write Operation

All Companion writes operate in a similar manner to memory writes. The distinction is that a different device ID is used and only one byte of address is needed instead of two. Figure 15 illustrates a single byte write to this device.

Companion Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM32xx will begin shifting data out from the current register address on the next clock. Auto-increment operates for the special function registers as with the memory address. A current address read for the registers look exactly like the memory except that the device ID is different.

The FM32xx contains two separate address registers, one for the memory address and the other for the register address. This allows the contents of one address register to be modified without affecting the current address of the other register. For example, this would allow an interrupted read to the memory while still providing fast access to a companion register. A subsequent memory read will then continue from the memory address where it previously left off, without requiring the load of a new memory address. However, a write sequence always requires an address to be supplied.

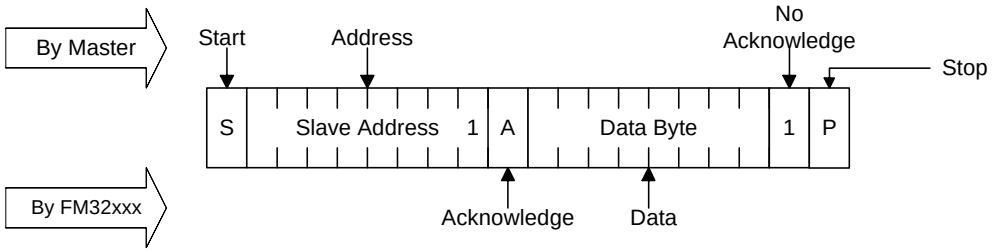


Figure 12. Current Address Memory Read

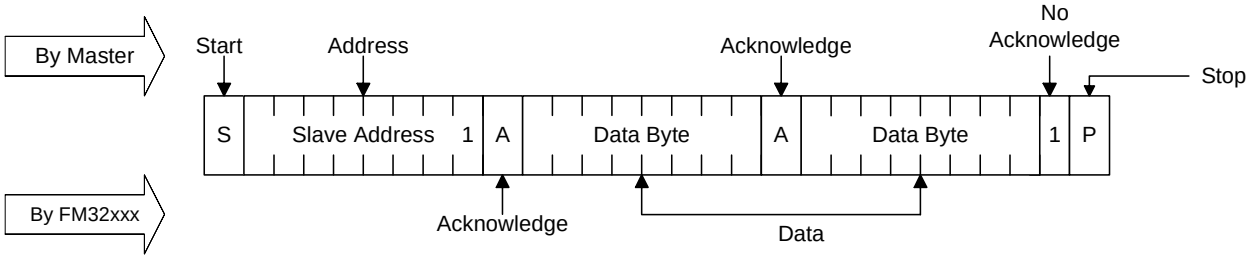


Figure 13. Sequential Memory Read

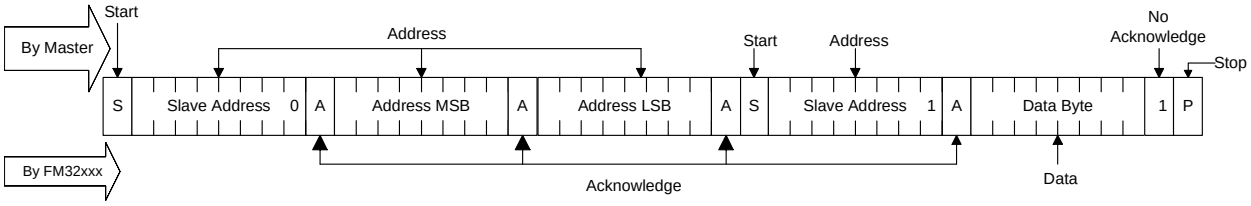


Figure 14. Selective (Random) Memory Read

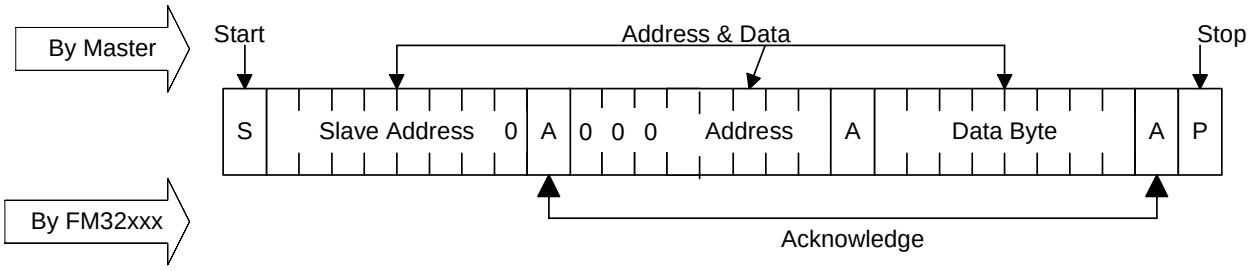


Figure 15. Byte Register Write

* Although not required, it is recommended that A5-A7 in the Register Address byte are zeros in order to preserve compatibility with future devices.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V, except SCL, SDA
V_{BAK}	Backup Supply Voltage	-1.0V to +4.5V
T_{STG}	Storage temperature	-55°C to + 125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	2.7		5.5	V	7
I_{DD}	V_{DD} Supply Current					1
	@ SCL = 100 kHz			500	µA	
	@ SCL = 400 kHz			900	µA	
	@ SCL = 1 MHz			1500	µA	
I_{SB}	Standby Current			150	µA	2
V_{BAK}	Backup Supply Voltage	2.0	3.0	3.75	V	9
I_{BAK}	Backup Supply Current			1	µA	4
I_{BAKTC}	Trickle Charge Current	5		15	µA	10
V_{TP0}	V_{DD} Trip Point Voltage, VTP(1:0) = 00b	2.50	-	2.75	V	5
V_{TP1}	V_{DD} Trip Point Voltage, VTP(1:0) = 01b	2.75	-	3.05	V	5
V_{TP2}	V_{DD} Trip Point Voltage, VTP(1:0) = 10b	3.70	-	4.05	V	5
V_{TP3}	V_{DD} Trip Point Voltage, VTP(1:0) = 11b	4.20	-	4.55	V	5
V_{RST}	V_{DD} for valid /RST @ I_{OL} = 80 µA at V_{OL}					6
	$V_{BAK} > V_{BAK}$ min	0			V	
	$V_{BAK} < V_{BAK}$ min	1.6			V	
I_{LI}	Input Leakage Current			1	µA	3
I_{LO}	Output Leakage Current			1	µA	3
V_{IL}	Input Low Voltage					
	All inputs except as listed	-0.3		0.3 V_{DD}	V	8
	CNT1-2 battery backed (V_{DD} < 2.5V)	-0.3		0.5	V	
	CNT1-2 (V_{DD} > 2.5V)	-0.3		0.8	V	
V_{IH}	Input High Voltage					
	All inputs except those listed below	0.7 V_{DD}		V_{DD} + 0.5	V	
	PFI (power fail input)	-		V_{BAK}	V	
	CNT1-2 battery backed (V_{DD} < 2.5V)	V_{BAK} – 0.5		V_{BAK} + 0.5	V	
	CNT1-2 V_{DD} > 2.5V	0.7 V_{DD}		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (I_{OL} = 3 mA)	-		0.4	V	
V_{OH}	Output High Voltage (I_{OH} = -2 mA)	2.4		-	V	
R_{RST}	Pull-up resistance for /RST inactive	50		400	KΩ	
R_{IN}	Input Resistance					
	A1-A0 for $V_{IN} = V_{IL}$ max	20			KΩ	
	A1-A0 for $V_{IN} = V_{IH}$ min	1			MΩ	
V_{PFI}	Power Fail Input Reference Voltage	1.125	1.15	1.175	V	
V_{HYS}	Power Fail Input (PFI) Hysteresis (Rising)		220	350	mV	

Notes

1. SCL toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V.
2. All inputs at V_{SS} or $V_{DD,}$ static. Stop command issued.

3. V_{IN} or $V_{OUT} = V_{SS}$ to V_{DD}. Does not apply to pins with internal pull down resistors or to PFI.
4. V_{BAK} = 3.0V, V_{DD} < 2.4V, oscillator running, CNT1-2 at V_{BAK}.
5. /RST is asserted active when $V_{DD} < V_{TP}$.
6. The minimum V_{DD} to guarantee the level of /RST remains a valid V_{OL} level.
7. Full complete operation. Supervisory circuits, etc operate to lower voltages as specified.
8. Includes /RST input detection of external reset condition to trigger driving of /RST signal by FM32xx.
9. The VBAK trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
10. V_{BAK} will source current when trickle charge is enabled (VBC bit=1), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V, C_L = 100 pF unless otherwise specified)

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Notes
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz	
t_{LOW}	Clock Low Period	4.7		1.3		0.6		µs	
t_{HIGH}	Clock High Period	4.0		0.6		0.4		µs	
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9		0.55	µs	
t_{BUF}	Bus Free Before New Transmission	4.7		1.3		0.5		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		0.25		µs	
$t_{SU:STA}$	Start Condition Setup for Repeated Start	4.7		0.6		0.25		µs	
$t_{HD:DAT}$	Data In Hold	0		0		0		ns	
$t_{SU:DAT}$	Data In Setup	250		100		100		ns	
t_R	Input Rise Time		1000		300		300	ns	1
t_F	Input Fall Time		300		300		100	ns	1
$t_{SU:STO}$	Stop Condition Setup	4.0		0.6		0.25		µs	
t_{DH}	Data Output Hold (from SCL @ VIL)	0		0		0		ns	
t_{SP}	Noise Suppression Time Constant on SCL, SDA		50		50		50	ns	

All SCL specifications as well as start and stop conditions apply to both read and write operations.

Supervisor Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V)

Symbol	Parameter	Min	Max	Units	Notes
t_{RPU}	Reset active after $V_{DD}>V_{TP}$	100	200	ms	
t_{RNR}	$V_{DD} < V_{TP}$ noise immunity	10	25	µs	1
t_{VF}	Fall time of VDD from V_{TP} to 0V	100	-	µs	1,2
t_{VR}	Rise time of VDD from 0V to VTP	100	-	µs	1,2
t_{WDP}	Pulse Width of /RST for Watchdog Reset	100	200	ms	
t_{WDOG}	Timeout of Watchdog	t_{DOG}	$2*t_{DOG}$	ms	3
f_{CIN}	Frequency of Event Counters	0	10	MHz	

Data Retention (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 5.5V)

Parameter	Min	Units	Notes
Data Retention	10	Years	

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.0V)

Symbol	Parameter	Max	Units	Notes
C_{IO}	Input/output capacitance	8	pF	1

Notes

1 This parameter is characterized but not tested.
2 Slew rate for proper transition between the battery-backed and normal operation.
3 t_{DOG} is the programmed time in register 0Ah, $V_{DD} > V_{TP}$ and t_{RPU} satisfied.

AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Equivalent AC Load Circuit

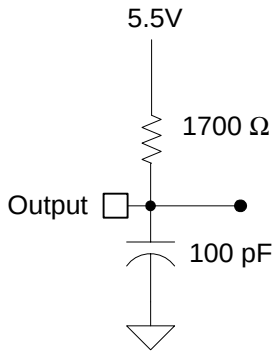
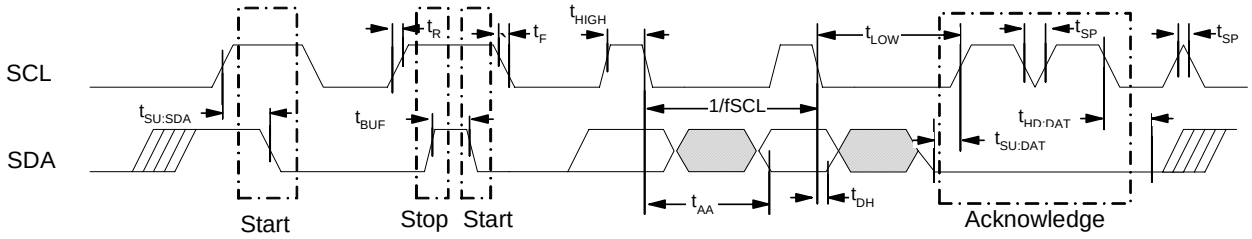


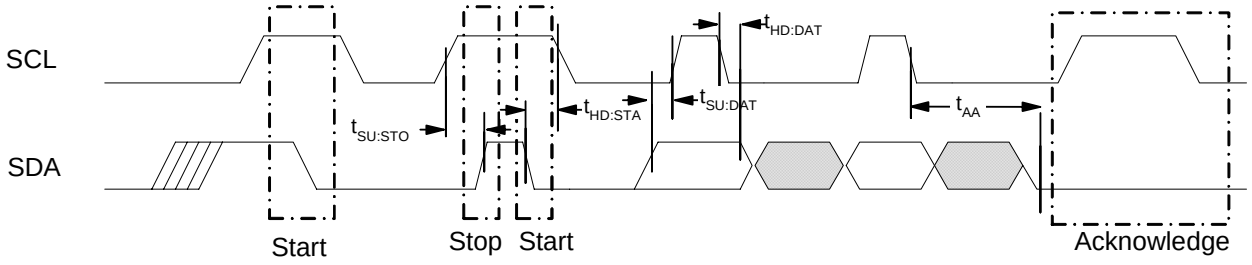
Diagram Notes

All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant data sheet sections. These diagrams illustrate the timing parameters only.

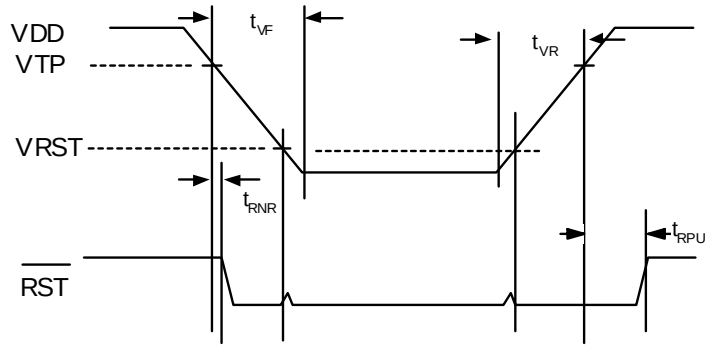
Read Bus Timing



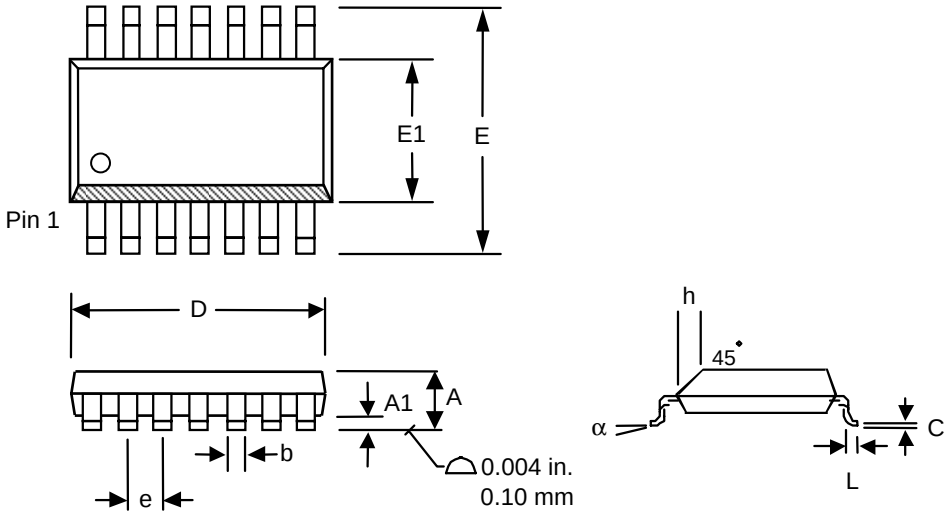
Write Bus Timing



/RST Timing



14-pin SOIC (JEDEC Standard MS-012 variation AB)



Controlling dimensions in millimeters.
Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm	1.35	-	1.75
	in.	0.053		0.069
A1	mm	0.10	-	0.25
	in.	0.004		0.010
b	mm	0.33	-	0.51
	in.	0.013		0.020
C	mm	0.19	-	0.25
	in.	0.007		0.010
D	mm	8.53	8.65	8.74
	in.	0.336	0.341	0.344
E	mm	5.80	6.00	6.20
	in.	0.228	0.236	0.244
E1	mm	3.73	-	3.99
	in.	0.147		0.157
e	mm		1.27 BSC	
	in.		0.050 BSC	
h	mm	0.25	-	0.50
	in.	0.010		0.020
L	mm	0.51	-	0.76
	in.	0.020		0.030
α		0°	-	8°

Revision History

Revision	Date	Summary
0.2	5/22/03	Initial release.
0.21	12/4/03	Change X1/X2 pins to NC.
1.0	3/30/04	Changed product status to Preliminary. Added V_{TP} and V_{PFI} parameters in DC Operating table. Changed V_{HYS} limits. Added “green” package.