CMM5114A

Radiation Hardened, High Reliability, CMOS/SOS 1024 Word by 4-Bit LSI Static RAM

November 1995

Features

- **Radiation Hardened to 10K RAD (Si)**
- **SEP Effective LET No Upsets: >100 MEV-cm^2/mg**
- **Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/ Bit-Day (Typ)**
- **Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s**
- **Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse**
- **Latch-Up Free Under Any Conditions**
- **Fully Static Operation**
- **Single Power Supply 4.5V to 6.5V**
- **All Inputs and Outputs TTL Compatible**
- **Three-State Outputs**
- **Industry Standard 18 Pin Configuration**
- **Low Standby and Operating Power**
- **Common Data Inputs and Outputs**
- **Gated Address Inputs by $\overline{CE}$**

Description

The CMM5114A is a high reliability 1024 word by 4-bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable. TTL compatibility on all I/O terminals permits easy system integration.

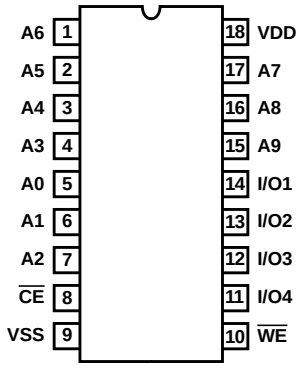
CMOS/SOS technology permits operation in radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistance to single event upset caused by cosmic rays or heavy ions.

Ordering Information

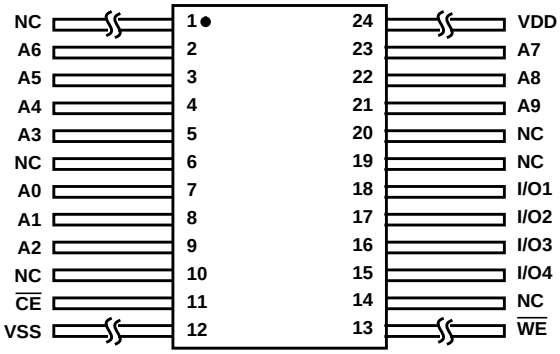
PART NUMBER	TEMP RANGE	PACKAGE
CMM5114AK3	-55^{o}C to +125^{o}C	Class B, 24 Lead Ceramic Flatpack (Not Rad Verified)
CMM5114AD3	-55^{o}C to +125^{o}C	Class B, 18 Lead SBDIP (Not Rad Verified)
CMM5114AK1DZ	-55^{o}C to +125^{o}C	Class S, 24 Lead Ceramic Flatpack (Rad Verified)
CMM5114AD1DZ	-55^{o}C to +125^{o}C	Class S, 18 Lead SBDIP (Rad Verified)

Pinouts

18 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835, CDIP2-T18
TOP VIEW



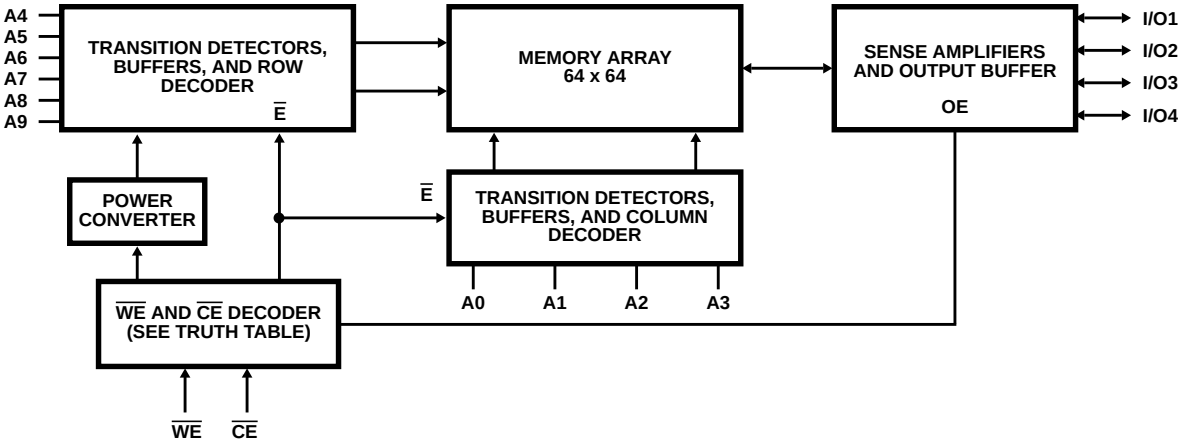
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835, CDFP4-F2
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Spec Number **518734**
File Number **2081.2**

Functional Diagram



TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT
L	H	Read	Dependent on Data
L	L	Write	Input
H	X	Not Selected	High Impedance

Absolute Maximum Ratings

Supply Voltage (VDD),
All voltage values referenced to VSS Terminal . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5 to VDD +0.5V
Input Current, Any One Input . . . . . ±10mA
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C
Typical Derating Factor. . . . . 3.0mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	78°C/W	18°C/W
Ceramic Flatpack Package	80°C/W	20°C/W

Maximum Package Power Dissipation at +125°C
SBDIP Package 0.64W
Ceramic Flatpack Package 0.63W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . . 12.8mW/°C
Ceramic Flatpack Package . . . . . 12.5mW/°C
Gate Count . . . . . 5400 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +6.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VDD/2 to VDD
Data Retention Supply Voltage 2.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Quiescent Device Current	IDD	VIN = 0V or VDD, $\overline{VCS}$ = VDD, VDD = 5.25V	-	0.1	-	1.0	mA
Operating Device Current (Note 2)	IDD1	Output Open Circuited Cycle Time = 1µs, VDD = 5.25V	-	5.0	-	6.0	mA
Output (Sink) Current	IOL	VOUT = 0.4V, VDD = 4.75V	2.6	-	1.7	-	mA
Output (Source) Current	IOH	VOUT = VDD - 0.4V, VDD = 4.75V	1.8	-	1.1	-	mA
Input Low Voltage (Note 3)	VIL	VDD = 4.75V	-	0.8	-	0.8	V
Input High Voltage (Note 3)	VIH	VDD = 4.75V	VDD/2	-	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD, VDD = 5.25V	-	±2	-	±10	µA
Three-State Output Leakage Current	IOZ	VDD = 5.25V Applied Voltage = 0V or VDD	-	±5	-	±50	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR	VDD = VDR	-	50	-	500	µA

NOTES:

1. VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified.
2. Operating current measured using 1MHz cycle and CL = 50pF.
3. Measured using 1MHz cycle.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

PARAMETER	SYMBOL	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
READ CYCLE TIMES						
Read Cycle	tAVAV	200	-	250	-	ns
Access	tAVQV	-	200	-	250	ns
Chip Enable to Output Valid	tELQV	-	220	-	280	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	250	-	300	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1) **(Continued)**

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Write Pulse Width (Note 2)	tWLWH	200	-	200	-	ns
Address Hold Time From Write Enable	tWHAV	40	-	50	-	ns
Address to Write Set Up Time	tAVWL	0	-	0	-	ns
Address Set Up to End of Write	tAVWH	200	-	250	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	200	-	250	-	ns
$\overline{CE}$ Pulse Width (Note 2)	tELEH	200	-	250	-	ns
Data to Write Set Up Time	tDVWH	90	-	105	-	ns
Data Hold From Write	tWHDX	5	-	5	-	ns

NOTES:

1. VDD = 5V ±5%, CL = 50pF.
2. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap and $\overline{CE}$ must be held low for 10ns after $\overline{WE}$ goes high.
3. Table 2 AC parameters are verified with VDD = 4.75V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Output Voltage Low Level	VOL	-	0.1	-	0.2	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.2	-	V
Input Capacitance	CIN	-	5	-	5	pF
Output Capacitance	COUT	-	7	-	7	pF
Chip Enable to Output Active	tELQA	20	-	20	-	ns
Output Three-State from Disable	tEHQZ	-	100	-	140	ns
Output Hold from Address Change	tAVQZ	30	110	55	150	ns

NOTE:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterize upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 10K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, $\overline{VCS}$ = VDD	-	1.0	mA
Operating Device Current (Note 1)	IDD1	Output Open Circuited Cycle Time = 1µs	-	6.0	mA
Output Current (Sink)	IOL	VOUT = 0.4V	1.7	-	mA
Output Current (Source)	IOH	VOUT = VDD - 0.4V	-1.1	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±10	µA
Three-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD	-	±50	µA

TABLE 4. POST 10K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Minimum Data Retention Voltage	VDR		-	2.5	V
Data Retention Quiescent Current	IDDDR		-	500	µA
Read Cycle	tAVAV		250	-	ns
Access	tAVQV		-	250	ns
$\overline{CE}$ to Output Valid	tELQV		-	280	ns
Write Cycle	tAVAV		300	-	ns
Write Pulse Width (Note 3)	tWLWH		200	-	ns
Address Hold Time from Write Enable	tWHAV		50	-	ns
Address to Write Set Up Time	tAVWL		0	-	ns
Address Set Up to End of Write	tAVWH		250	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH		250	-	ns
$\overline{CE}$ Pulse Width (Note 3)	tELEH		250	-	ns
Data to Write Set Up Time	tDVWH		105	-	ns
Data Hold From Write	tWHDX		5	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Measured using 1MHz cycle.
3. Operating current measured using 1MHz cycle and CL = 50pF.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IOL	-10% of 0 hour value
Output High Drive Current (Source)	IOH	-10% of 0 hour value
Three-State Output Leakage Current	IOZ	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	-IRZ SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9
Group E, Subgroup 2		Samples/5005	1, 7, 9	N/A

Intersil Space Level Product Flow -1DZ

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer), 2 Samples/Wafer, 0 Rejects

Sample - Die Shear Monitor, Method 2019 or 2027

Sample - Wire Bond Monitor, Method 2011

100% Nondestructive Bond Pull, Method 2023

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% Serialization

100% Initial Test

Optional High Temperature Stress Test, 48 Hours at +125^{o}C (This is a Intersil Option)

Optional Interim Electrical Test (T0) (Only if the High Temperature Stress Test was performed) 10% PDA (Note 1)

100% Static Burn-In 1, Condition A or B, 24 Hours Minimum, +125^{o}C Minimum (or Equivalent Time/Temperature), Method 1015

100% Interim Electrical Test (T1) and Deltas (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 Hours Minimum, +125^{o}C Minimum, (or equivalent Time/Temperature), Method 1015

100% Interim Electrical Test (T2) and Delta (T0-T2) (Notes 2, 3)

100% Dynamic Burn-In, Condition D, 240 Hours at 125^{o}C (or Equivalent Time/Temperature), Method 1015

100% Interim Electrical Test (T3). 5% PDA All Failures, Deltas (T0-T3) (Note 3)

100% Final Test, Method 5004

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 4)

100% External Inspection, Method 2009

Sample - Group A, Method 5005 (Note 5)

100% Data Package Generation (Note 6)

NOTES:

1. If the optional 48-hour Stress Test is not utilized, then the Initial Test is used for T0 reference when calculating deltas.
2. Failures from Interim Electrical Tests T1 and T2 are combined for determining PDA.
3. Failures from subgroups 1, 7, and deltas are used for calculating PDA. The maximum allowable PDA is 5% with no more than 3% from subgroup 7.
4. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004. Per Method 5004.
5. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
6. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, RAD Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Intersil Space Level Product Flow -3

100% Internal Visual Inspection, Method 2010, Condition B or Alternate Condition B

100% Temperature Cycle, Method 1010, Condition C

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% Fine/Gross Leak, Method 1014

100% Initial Electrical Test, +25^{o}C

Optional High Temperature Stress Test, 48 Hours at +125^{o}C (This is a Intersil Option)

Optional Interim Electrical Test (Only if the High Temperature Stress Test was performed at Intersil option) 10% PDA

100% Static Burn-In, Condition A or B, 24 Hours minimum, +125^{o}C minimum (or Equivalent Time/Temperature), per Method 1015

100% Interim Electrical Test, 5% PDA, 3% PDA functional (Note 1)

100% Final Electrical Tests

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

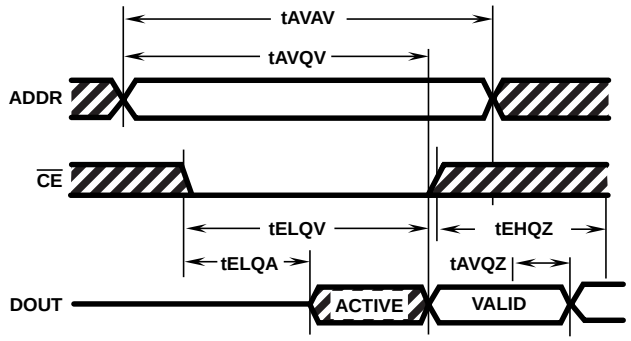
Data Package Generation (Note 3)

NOTES:

1. Failures from subgroups 1 and 7 are used for calculating PDA. The maximum allowable PDA is 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

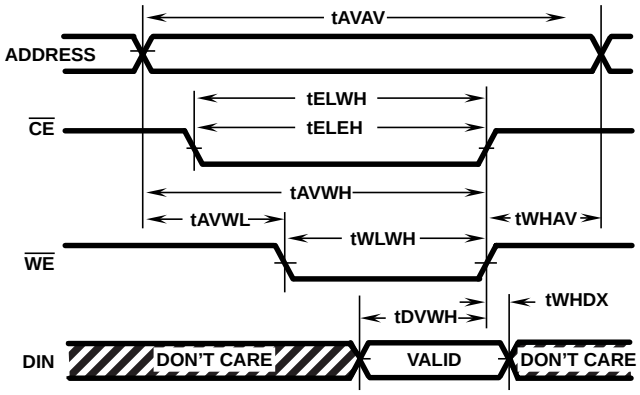
Timing Waveforms

READ CYCLE



NOTE: $\overline{WE}$ is high during the READ cycle timing measurement reference level is VDD/2.

WRITE CYCLE



NOTE:

1. Timing measurement is referenced to VDD/2.

Typical Performance Curves

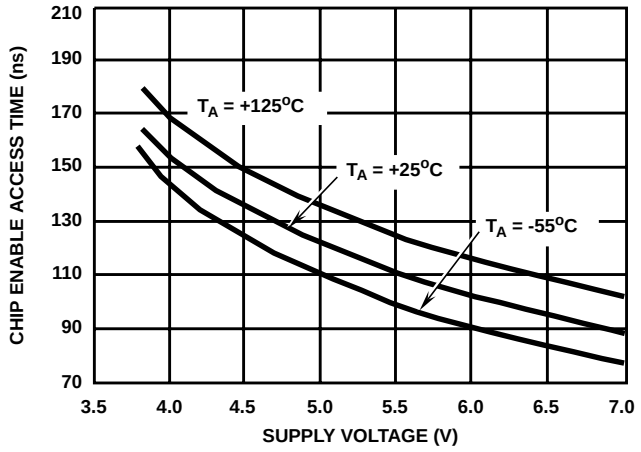


FIGURE 1. ADDRESS ACCESS TIME CHARACTERISTICS

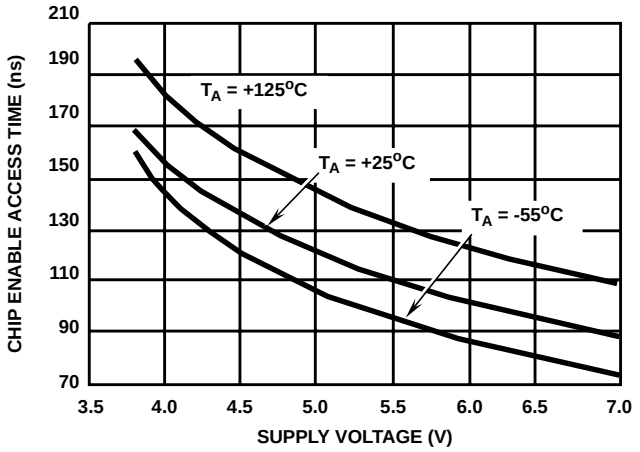


FIGURE 2. CHIP ENABLE ACCESS TIME CHARACTERISTICS

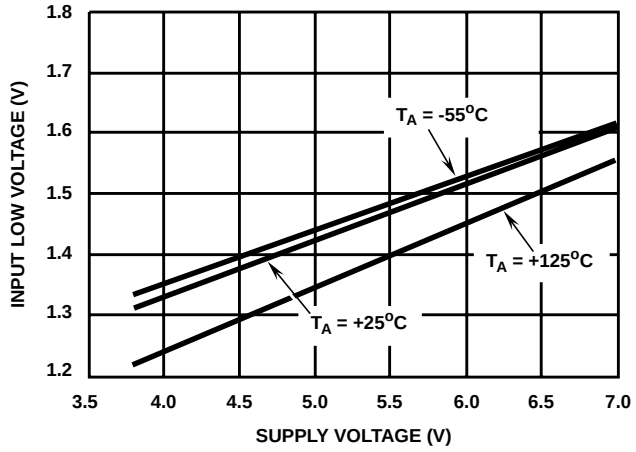


FIGURE 3. INPUT LOW VOLTAGE CHARACTERISTICS

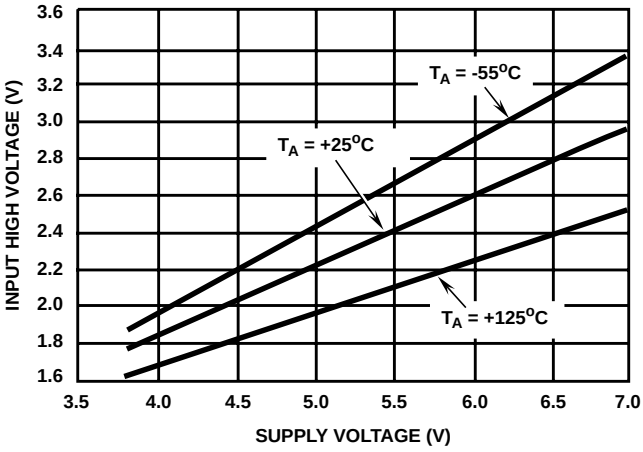


FIGURE 4. INPUT HIGH VOLTAGE CHARACTERISTICS

Typical Performance Curves (Continued)

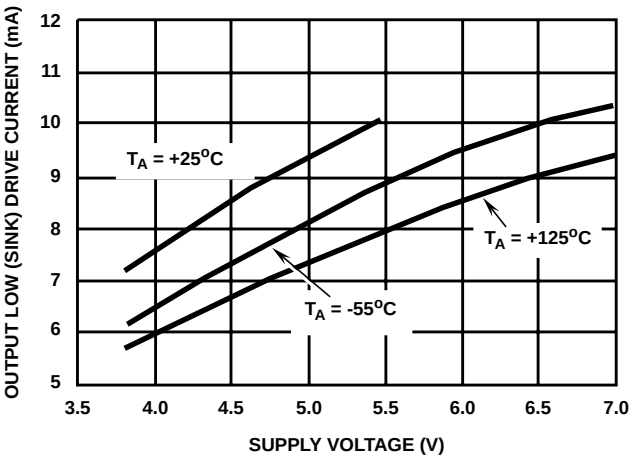


FIGURE 5. OUTPUT LOW (SINK) DRIVE CURRENT CHARACTERISTICS

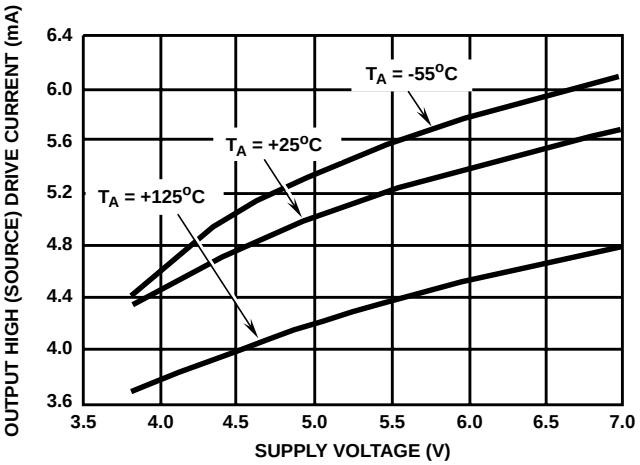


FIGURE 6. OUTPUT HIGH (SOURCE) DRIVE CURRENT CHARACTERISTICS

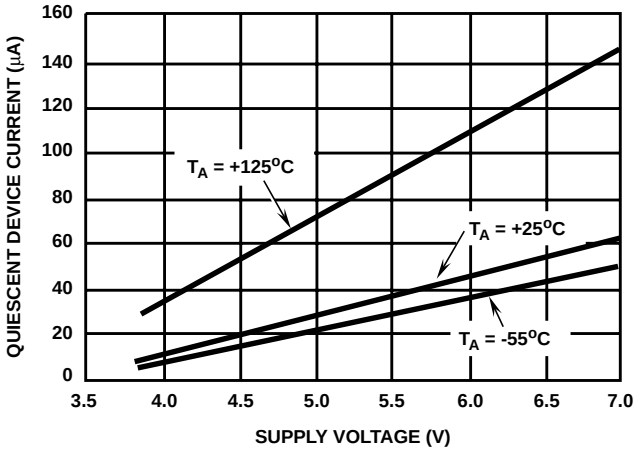
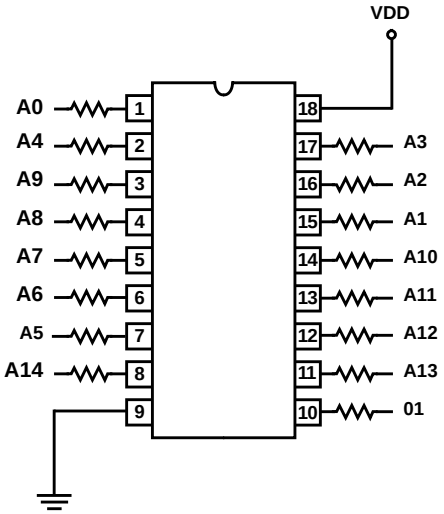


FIGURE 7. QUIESCENT DEVICE CURRENT CHARACTERISTICS

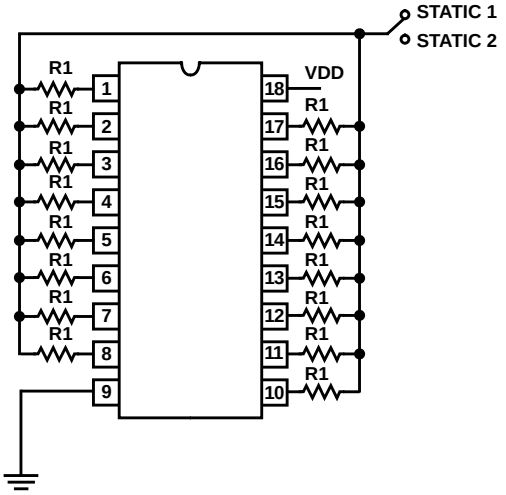
Burn-In Circuits



DYNAMIC CONFIGURATION

NOTES:

R1 = 1kΩ to 6kΩ, Unless Otherwise Specified
VDD = 5.5V (Min)
Frequencies: A0 = 100KHz ±5%
A1 = A0/2 . . . . A13 = A12/2
01 = 200KHz ±5%, 0.6µs Low, 4.4µs High
Ceramic DIP biasing shown.

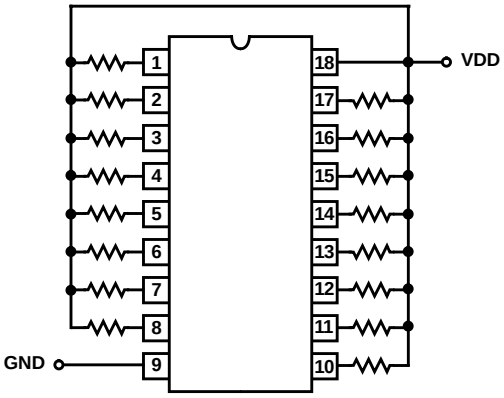


STATIC CONFIGURATION

NOTES:

R1 = 1kΩ to 6kΩ
VDD = 5.5V (Min)
Stress Test; Switch is at VSS
Static 1: Switch is at VDD
Static 2: Switch is at VSS
Ceramic DIP biasing shown.

Irradiation Circuit



NOTES:

VDD = +5V, ±5%
GND = Ground
All Resistors are 47kΩ ±5%

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029