ICS8543

LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

GENERAL DESCRIPTION

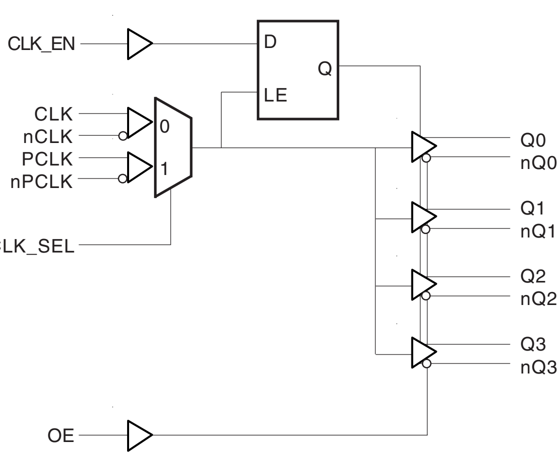
The ICS8543 is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8543 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8543 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8543 ideal for those applications demanding well defined performance and repeatability.

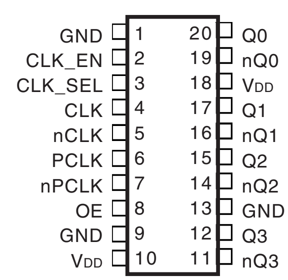
FEATURES

- 4 differential LVDS outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 800MHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLK input
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 2.6ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8543

20-Lead TSSOP
4.4mm x 6.5mm x 0.92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 9, 13	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0, nQ0 through Q3, nQ3. When logic HIGH, the outputs are active. When logic LOW, the outputs are in high impedance state. LVCMOS/ LVTTL interface levels.
10, 18	V_{DD}	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldow*n refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs	
OE	**CLK_EN**	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**nQ0:nQ3**
0	X	X		Hi Z	Hi Z
1	0	0	CLK, nCLK	Disabled; Low	Disabled; High
1	0	1	PCLK, nPCLK	Disabled; Low	Disabled; High
1	1	0	CLK, nCLK	Enabled	Enabled
1	1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in *Figure 1.*
In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.

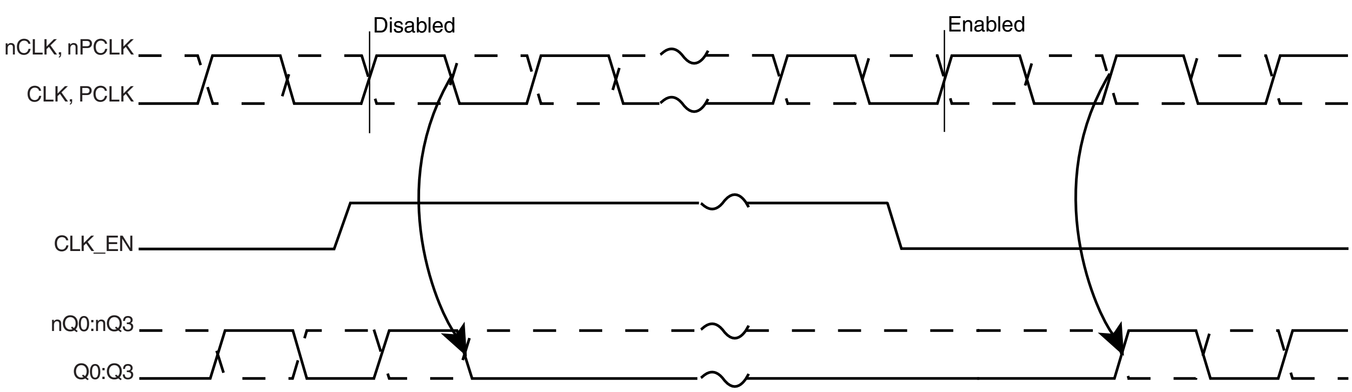


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK, PCLK	**nCLK, nPCLK**	**Q0:Q3**	**nQ0:nQ3**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_EN, CLK_SEL, OE		2		3.765	V
V_{IL}	Input Low Voltage	CLK_EN, CLK_SEL, OE				0.8	V
I_{IH}	Input High Current	CLK_EN, OE				5	µA
		CLK_SEL				150	µA
I_{IL}	Input Low Current	CLK_EN, OE		-150			µA
		CLK_SEL		-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 4E. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

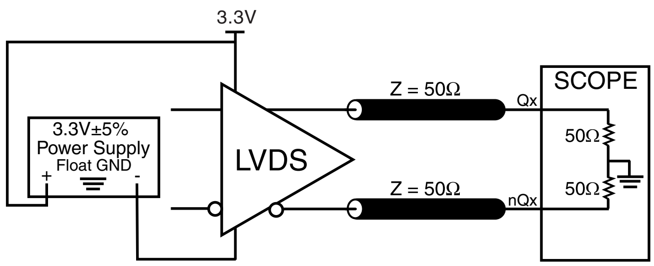
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200	280	360	mV
ΔV_{OD}	VOD Magnitude Change			0	40	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	VOS Magnitude Change			5	25	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	µA
I_{OFF}	Power Off Leakage		-20	±1	+20	µA
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output Short Circuit Current			-3.5	-5	mA
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		V

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

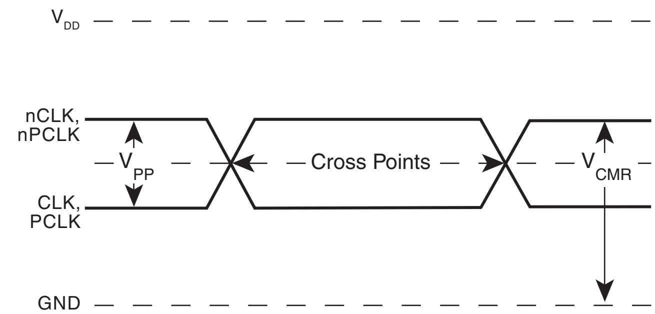
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				800	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 800MHz	1.7		2.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	150		350	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	150		350	ps
odc	Output Duty Cycle		45	50	55	%

All parameters measured at 500MHz.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

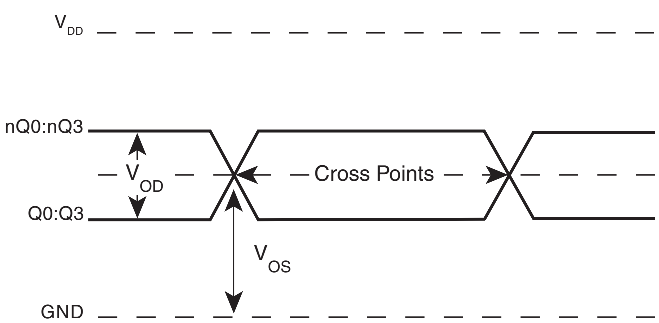
PARAMETER MEASUREMENT INFORMATION



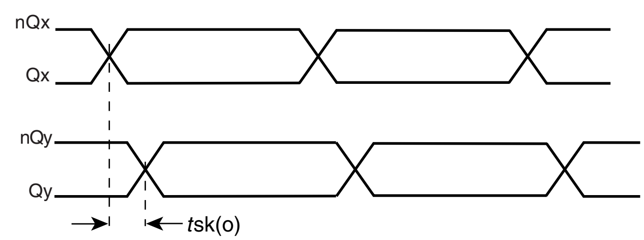
3.3V OUTPUT LOAD AC TEST CIRCUIT



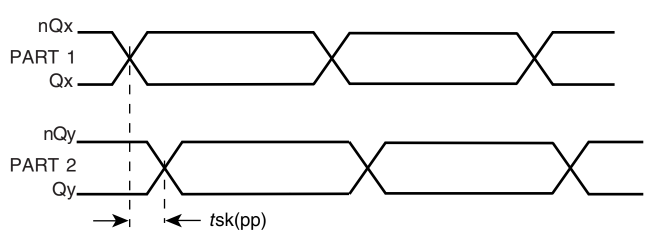
DIFFERENTIAL INPUT LEVEL



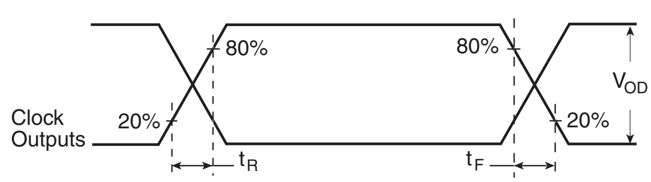
DIFFERENTIAL OUTPUT LEVEL



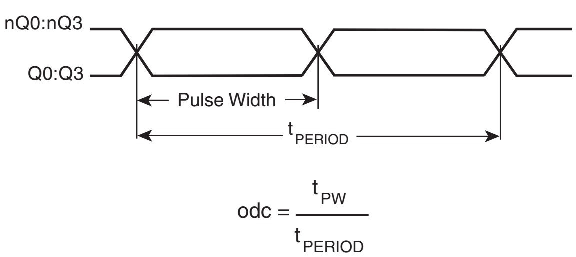
OUTPUT SKEW



PART-TO-PART SKEW

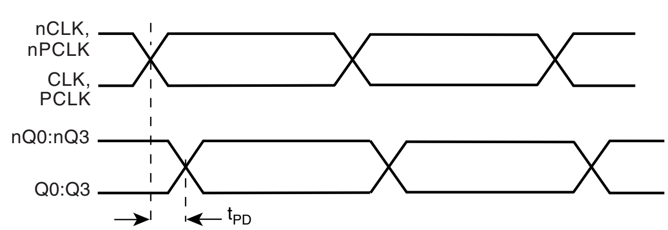


OUTPUT RISE/FALL TIME

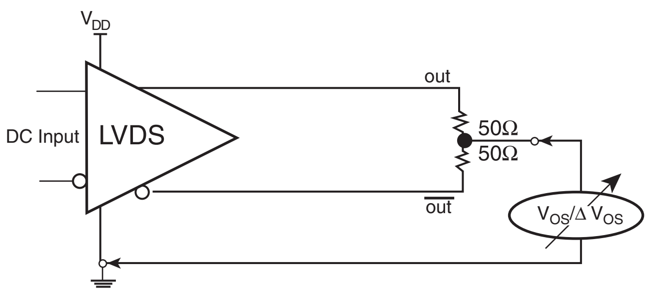


$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

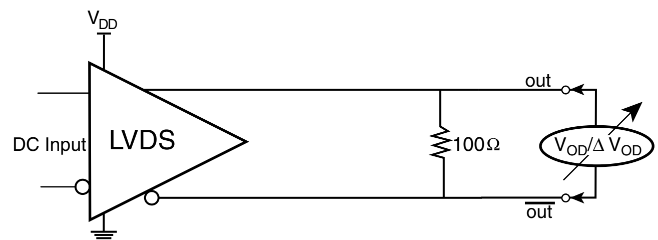
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



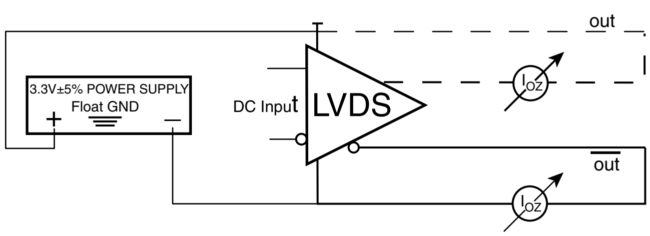
PROPAGATION DELAY



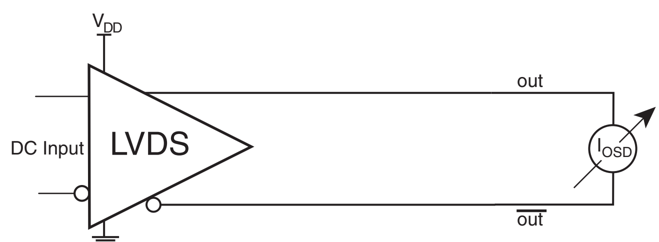
OFFSET VOLTAGE SETUP



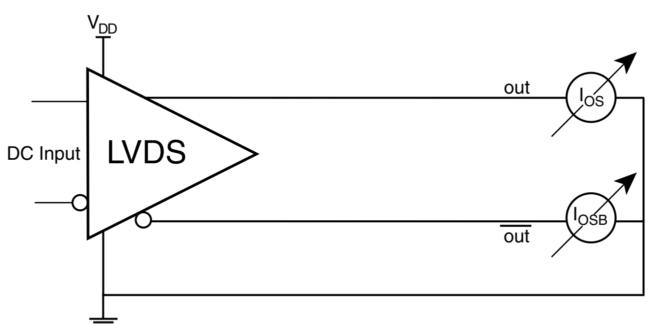
DIFFERENTIAL OUTPUT VOLTAGE SETUP



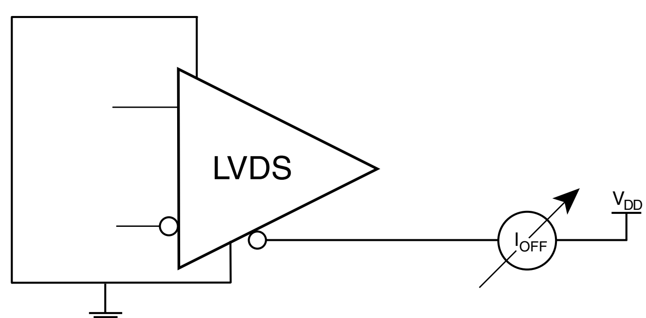
HIGH IMPEDANCE LEAKAGE CURRENT SETUP



DIFFERENTIAL OUTPUT SHORT CIRCUIT SETUP



OUTPUT SHORT CIRCUIT CURRENT SETUP



POWER OFF LEAKAGE SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

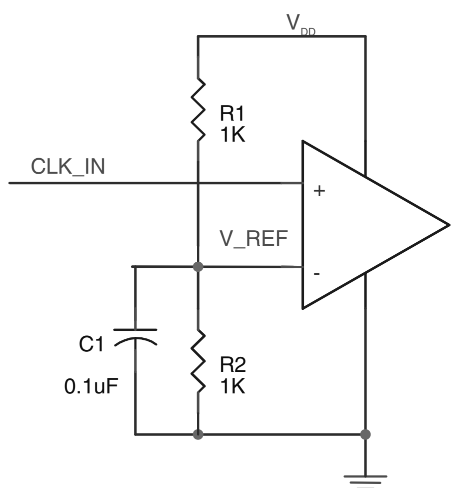


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

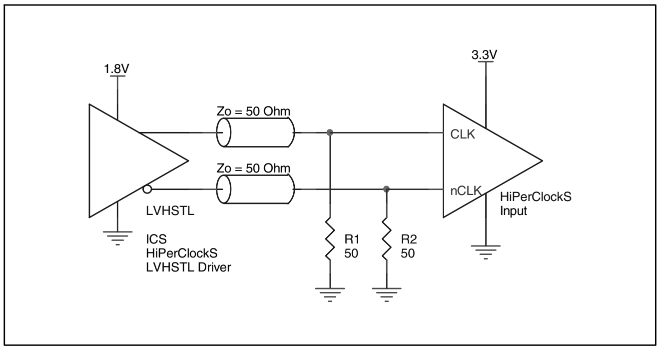


FIGURE 3A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

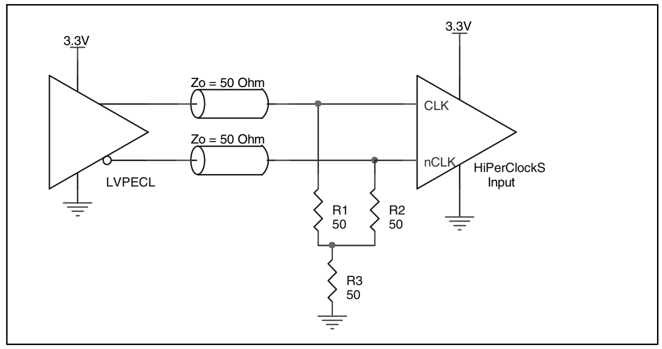


FIGURE 3B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

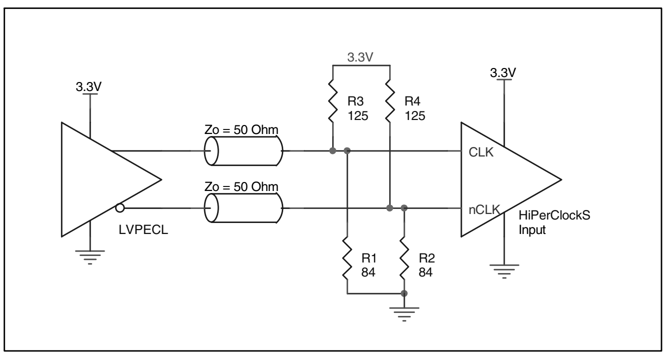


FIGURE 3C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

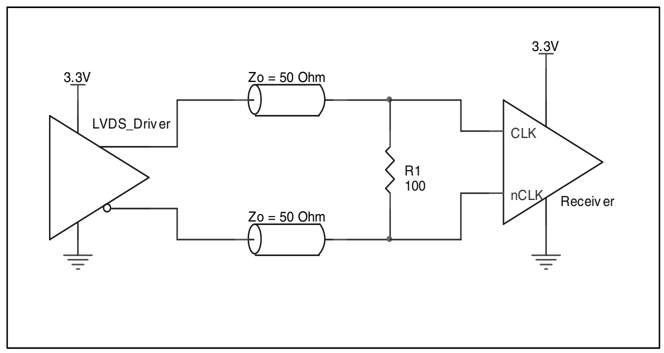


FIGURE 3D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

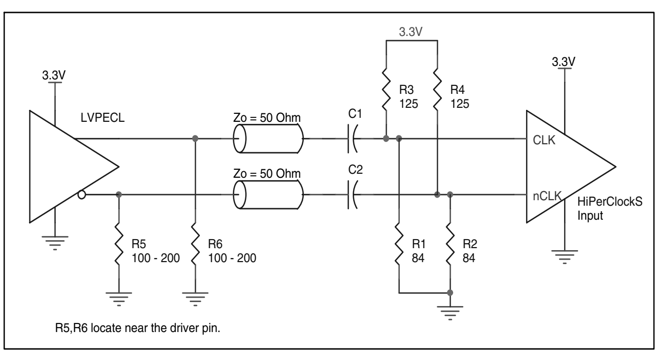


FIGURE 3E. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

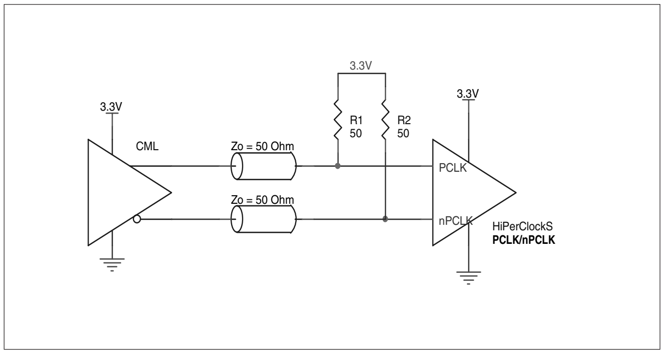


FIGURE 4A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

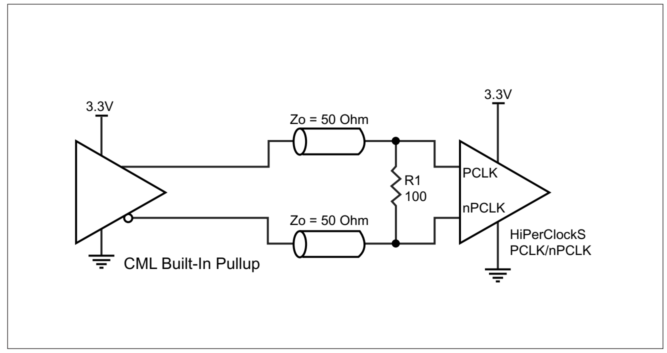


FIGURE 4B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

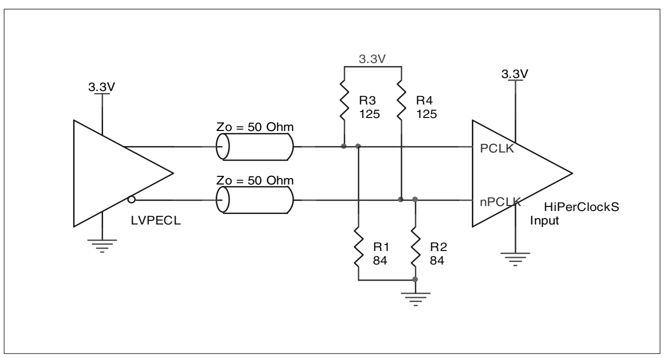


FIGURE 4C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

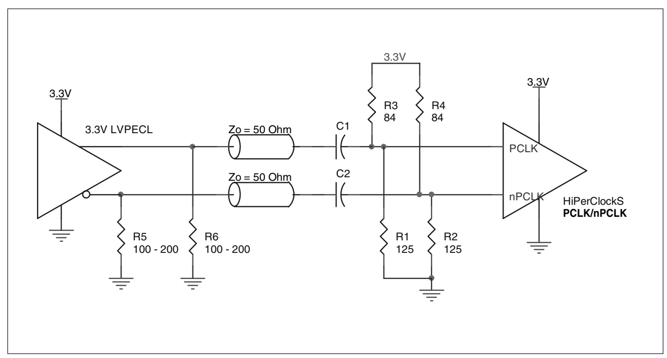


FIGURE 4D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

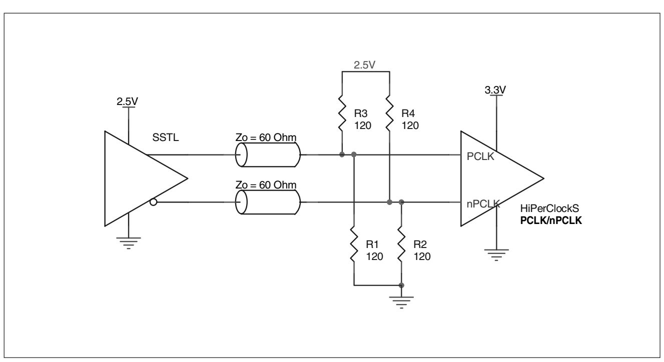


FIGURE 4E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

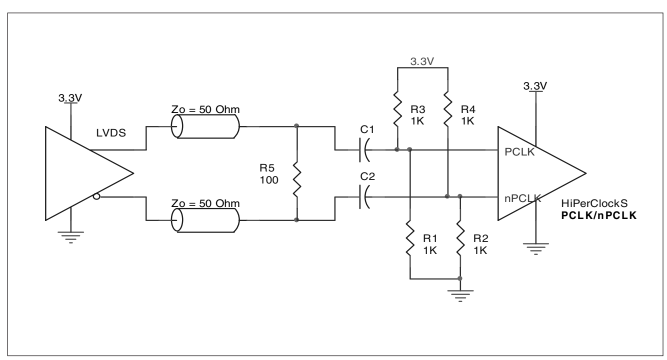


FIGURE 4F. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 4. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

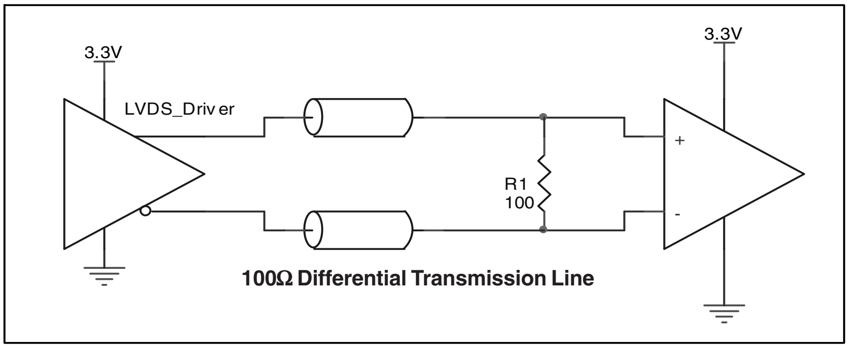


FIGURE 5. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8543 is: 636

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

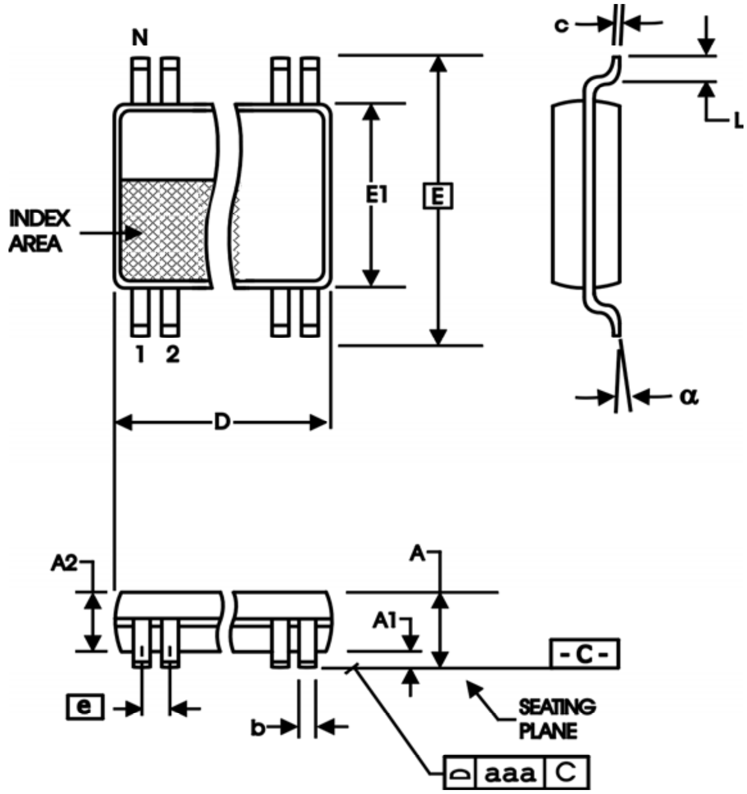


TABLE 7. PACKAGE DIMENSIONS

Symbol	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8543BG	ICS8543BG	20 lead TSSOP	72 per tube	0°C to 70°C
ICS8543BGT	ICS8543BG	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C
ICS8543BGLF	ICS8543BGLF	20 lead "Lead Free" TSSOP	72 per tube	0°C to 70°C
ICS8543BGLFT	ICS8543BGLF	20 lead "Lead Free" TSSOP on Tape and Reel	2500	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T4E	5	In the V_{OL} row, 1.06 has been moved to the Typical column from the maximum column.	9/18/01
A		3	Updated Figure 1, CLK_EN Timing Diagram.	10/17/01
A		3	Updated Figure 1, CLK_EN Timing Diagram.	11/2/01
A		1 6-10	Features section, Bullet 6 to read 3.3V LVDS levels instead of LVPECL. Udated Parameter Measurment Information figures.	5/6/02
B	T5	5	AC Characteristics table - revised Output Frequency from 650MHz to 800MHz.	6/5/02
C	 T4E	1 5	Features - deleted bullet "Designed to meet or exceed the requirements of ANSI TIA/EIA-644". LVDS Table - changed V_{OD} typical value from 350mV to 280mV.	9/19/02
D	T2	2 4 9 10 11	Pin Characteristics - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - changed Output rating. Added Differential Clock Input Interface section. Added LVPECL Clock Input Interface section. Added LVDS Driver Termination section. Updated format throughout data sheet.	12/31/03
D	T1	2	Pin Description table - added function description to the OE pin.	4/7/04
D	 T8	10 13	Updated LVPECL CLock Input Interface section. Added Lead Free part number to Ordering Information table.	6/16/04