Integrated
Circuit
Systems, Inc.

ICS87016I

LOW SKEW, 1-TO-16 LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87016I is a low skew, 1:16 LVCMOS/LVTTL Clock Generator and is a member of the HiPerClockS family of High Performance Clock Solutions. The device has 4 banks of 4 outputs and each bank can be independently selected for ÷1 or ÷2 frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

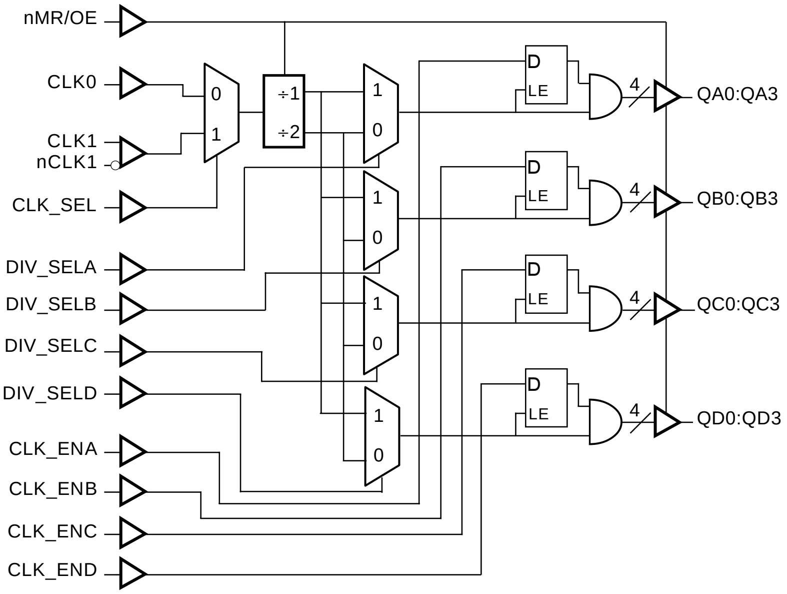
The divide select inputs, DIV_SELA:DIV_SELD, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The bank enable inputs, CLK_ENA:CLK_END, support enabling and disabling each bank of outputs individually. The CLK_ENA:CLK_END circuitry has a synchronizer to prevent runt pulses when enabling or disabling the clock outputs. The master reset input, nMR/OE, resets the ÷1/÷2 flip flops and also controls the active and high impedance states of all outputs. This pin has an internal pull-up resistor and is normally used only for test purposes or in systems which use low power modes.

The ICS87016I is characterized to operate with the core at 3.3V and the banks at 3.3V, 2.5V, or 1.8V. Guaranteed bank, output, and part-to-part skew characteristics make the 87016I ideal for those clock applications demanding well-defined performance and repeatability.

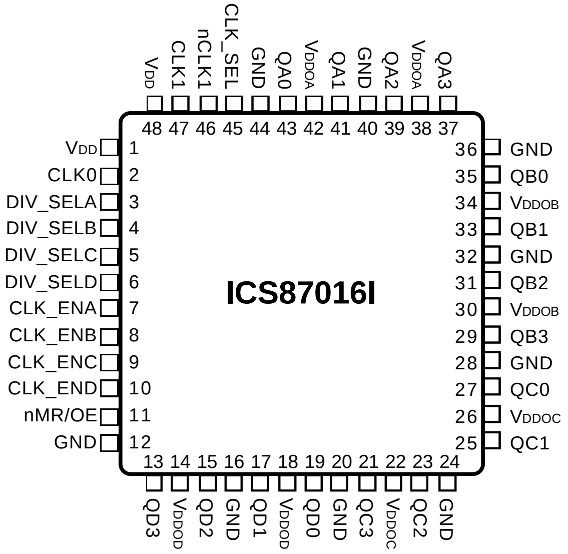
FEATURES

- 16 LVCMOS/LVTTL outputs (4 banks of 4 outputs)
- Selectable differential CLK1, nCLK1 or LVCMOS clock input
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operation
- Asynchronous clock enable/disable
- Output skew: 170ps (maximum)
- Bank skew: 50ps (maximum)
- Part-to-part skew: 800ps (maximum)
- 3.3V core, 3.3V, 2.5V, or 1.8V output operating supply
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Pin LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 48	V_{DD}	Power		Core supply pins.
2	CLK0	Input	Pulldown	LVCMOS / LVTTL clock input.
3	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs LVCMOS / LVTTL interface levels..
5	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels.
7	CLK_ENA	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
8	CLK_ENB	Input	Pullup	Output enable for Bank B outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
9	CLK_ENC	Input	Pullup	Output enable for Bank C outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
10	CLK_END	Input	Pullup	Output enable for Bank D outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
11	nMR/OE	Input	Pullup	Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels.
12, 16, 20, 24, 28, 32, 36, 40, 44	GND	Power		Supply ground.
13, 15, 17, 19	QD3, QD2, QD1, QD0	Output		Bank D outputs. LVCMOS / LVTTL interface levels.
14, 18	V_{DDOD}	Power		Output Bank D supply pins.
21, 23, 25, 27	QC3, QC2, QC1, QC0	Output		Bank C outputs. LVCMOS / LVTTL interface levels.
22, 26	V_{DDOC}	Power		Output Bank C supply pins.
29, 31, 33, 35	QB3, QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels.
30, 34	V_{DDOB}	Power		Output Bank B supply pins.
37, 39, 41, 43	QA3, QA2, QA1, QA0	Output		Bank A outputs. LVCMOS / LVTTL interface levels.
38, 42	V_{DDOA}	Power		Output Bank A supply pins.
45	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
46	nCLK1	Input	Pullup	Inverting differential clock input.
47	CLK1	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDOx} = 3.465V; NOTE 1			18	pF
		V_{DD} = 3.465, V_{DDOx} = 2.625V; NOTE 1			20	pF
		V_{DD} = 3.465, V_{DDOx} = 1.89V; NOTE 1			30	pF
R_{OUT}	Output Impedance		5	7	12	Ω

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, and V_{DDOD}.

TABLE 3. FUNCTION TABLE

Inputs			Outputs	
nMR/OE	CLK_ENx	DIV_SELx	Bank X	Qx Frequency
0	X	X	Hi Z	N/A
1	1	0	Active	fIN/2
1	1	1	Active	fIN
1	0	X	Low	N/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				100	mA
I_{DDOx}	Output Supply Current; NOTE 2				15	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, and V_{DDOD}. NOTE 2: I_{DDOx} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, and I_{DDOD}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA:DIV_SELD, CLK_ENA:CLK_END, nMR/OE, CLK_SEL		2		V_{DD} + 0.3	V
		CLK0		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, CLK_ENA:CLK_END, nMR/OE, CLK_SEL		-0.3		0.8	V
		CLK0		-0.3		1.3	V
I_{IH}	Input High Current	CLK_ENA:CLK_END, DIV_SELA:DIV_SELD, nMR/OE	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK0, CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_ENA:CLK_END, DIV_SELA:DIV_SELD, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK0, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%; NOTE 2	2.6			V
			V_{DDOx} = 2.5V ± 5%; NOTE 2	1.8			V
			V_{DDOx} = 1.8V ± 5%; NOTE 2 I_{OH} = -2mA	V_{DD} - 0.45			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%; NOTE 2			0.5	V
			V_{DDOx} = 2.5V ± 5%; NOTE 2			0.5	V
			V_{DDOx} = 1.8V ± 5%; NOTE 2 I_{OL} = 2mA			0.45	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOx}/2. See Parameter Measurement Information, Output Load Test Circuit.
NOTE 2: V_{DDOx} denotes V_{DDOA}, $V_{DDOB.}$ V_{DDOC} and V_{DDOD}.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK1	$V_{IN} = V_{DD}$ = 3.465V			5	µA
		CLK1	$V_{IN} = V_{DD}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
		CLK1	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK1, nCLK1 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDOx}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.8	3.4	3.9	ns
		CLK1, nCLK1; NOTE 1B		2.75	3.4	4.1	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		f < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.9	3.5	4.0	ns
		CLK1, nCLK1; NOTE 1B		3.0	3.5	4.0	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		f < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

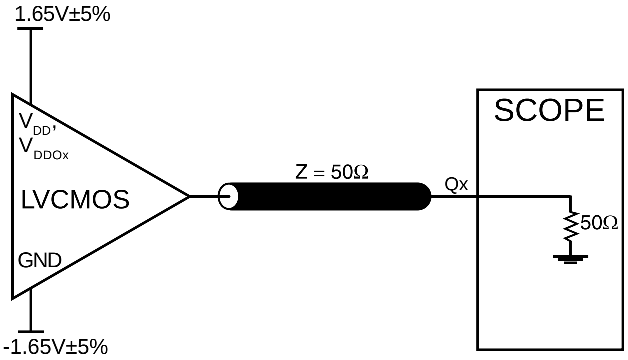
All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 1.8V±5%, TA = -40°C TO 85°C

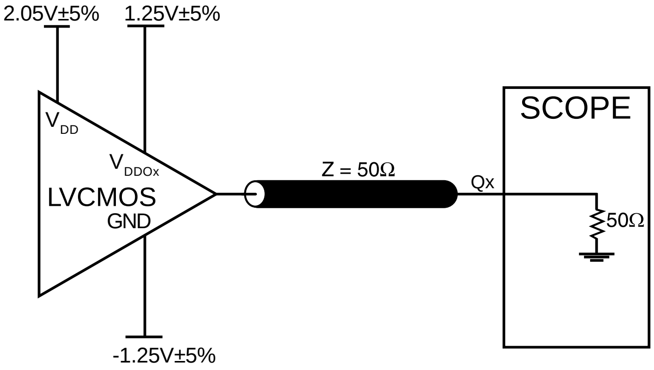
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		3.0	3.9	4.7	ns
		CLK1, nCLK1; NOTE 1B		3.0	3.9	4.7	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		f < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

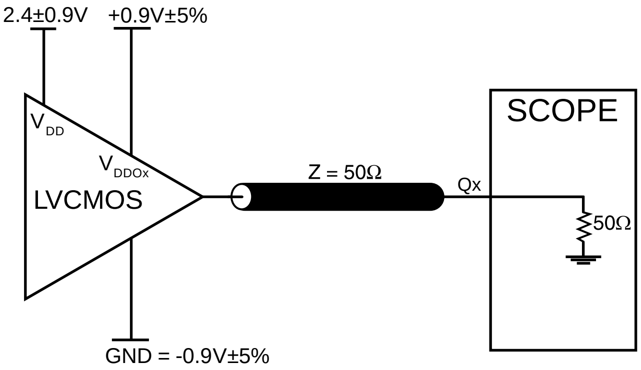
PARAMETER MEASUREMENT INFORMATION



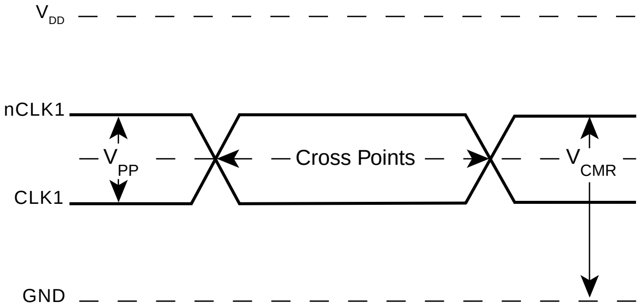
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



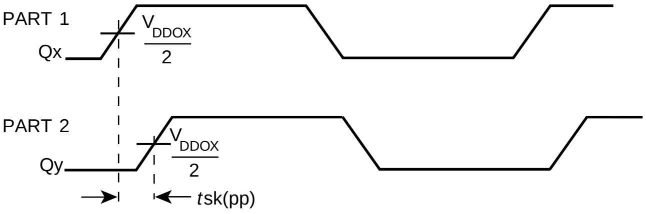
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



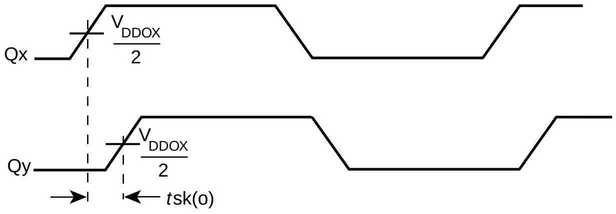
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



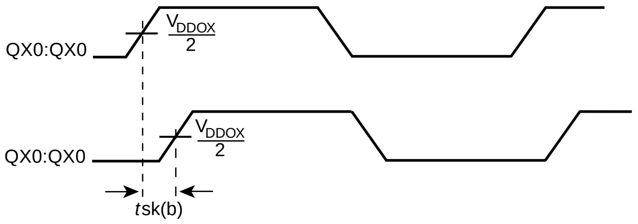
DIFFERENTIAL INPUT LEVEL



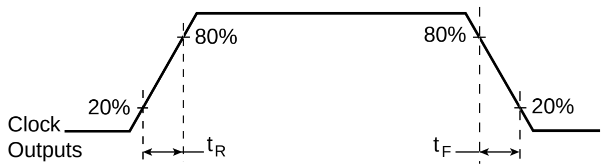
PART-TO-PART SKEW



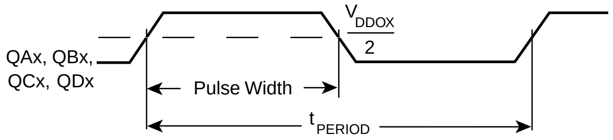
OUTPUT SKEW



Bank Skew (where X denotes outputs in the same bank)

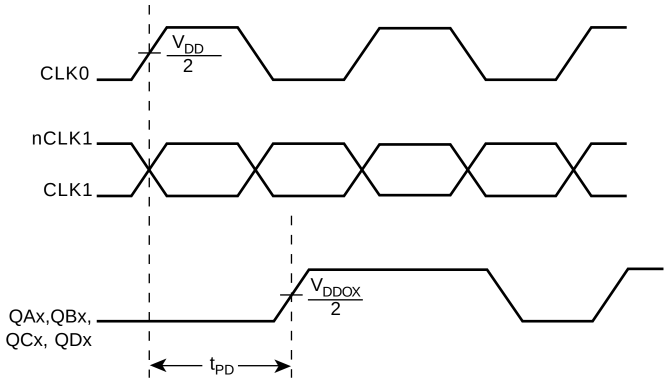


Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period



Propagation Delay

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

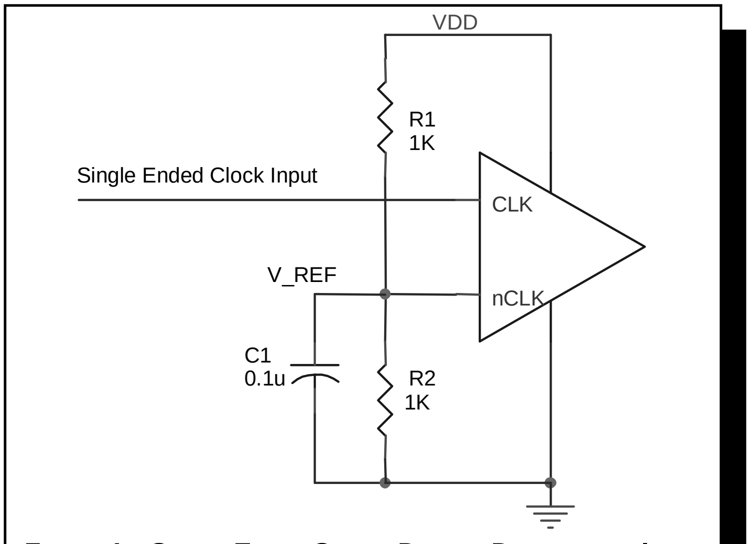


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

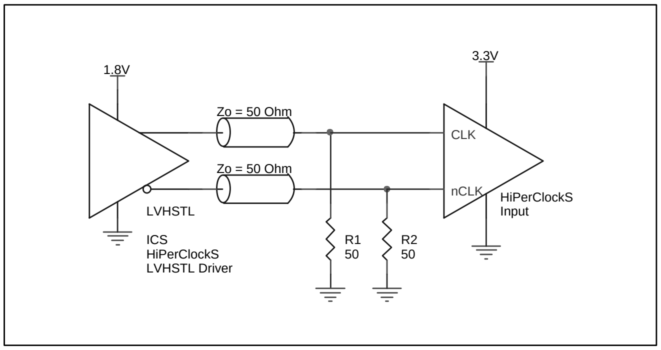


Figure 2A. HiPerClockS CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

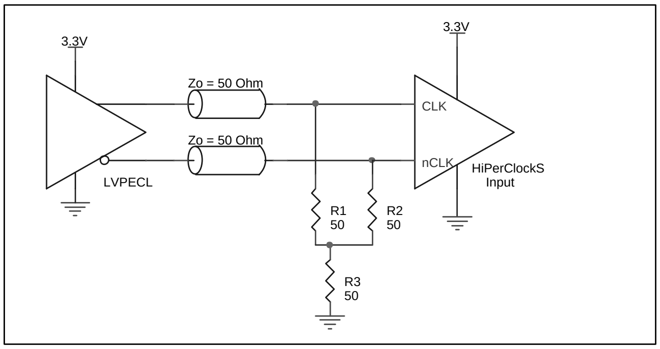


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

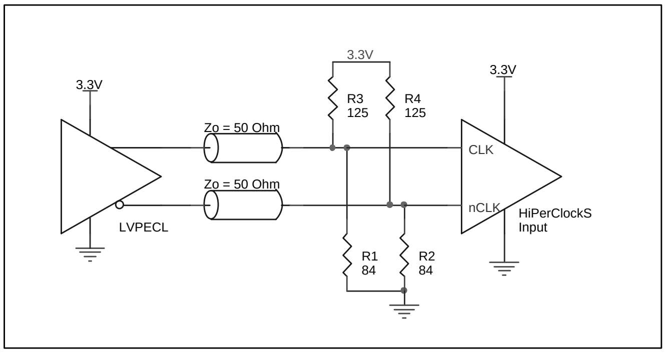


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

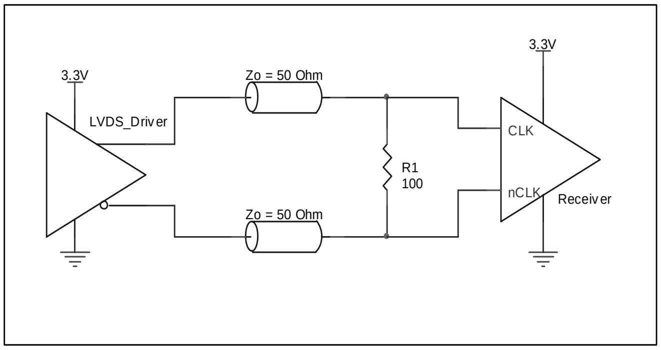
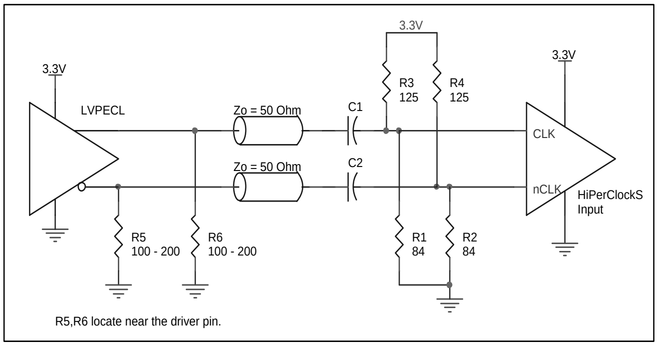


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver



R5,R6 locate near the driver pin.

Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87016I is: 2034

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

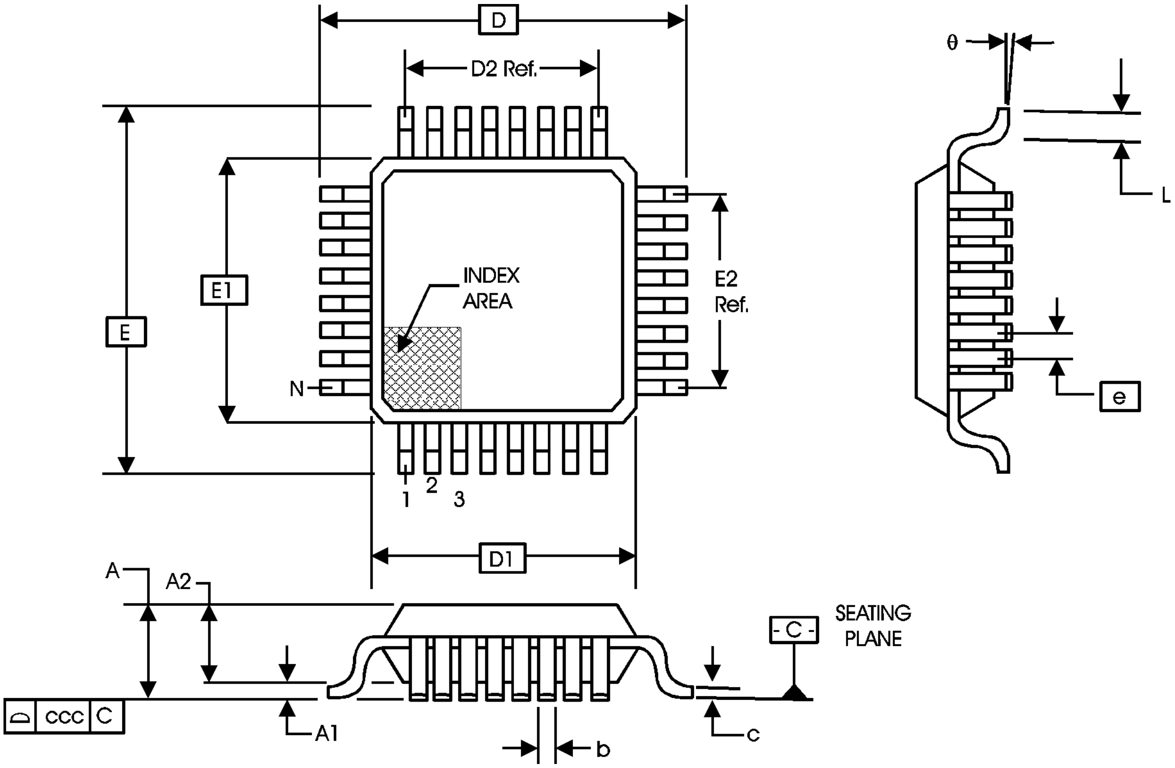


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87016AYI	ICS87016AYI	48 Lead LQFP	250 per tray	-40°C to 85°C
ICS87016AYIT	ICS87016AYI	48 Lead LQFP on Tape and Reel	1000	-40°C to 85°C