

ILC7083

150mA SOT-23 Ultra Low Noise CMOS RF-LDO™ Regulator

Features

- Ultra low 1mV dropout per 1mA load
- 3% output voltage accuracy
- Only 40 μ V_{RMS} noise
- Uses low ESR ceramic output capacitor to minimize noise and output ripple
- Only 100 μ A ground current at 100mA load
- Ripple rejection up to 85dB at 1kHz, 60dB at 1MHz
- Excellent line and load transient response
- Over current / over temperature protection
- Guaranteed to 150mA output current
- Industry standard five lead SOT-23 package
- Fixed 3.0V and adjustable output voltage options
- Metal mask option available for custom voltages between 2.5V and 5.1V

Description

The ILC7083 is a 150mA low dropout (LDO) voltage regulator designed to provide a high performance solution to low power systems. The device offers a typical combination of low dropout and low quiescent current expected of CMOS parts, while uniquely providing the low noise and high ripple rejection characteristics usually only associated with bipolar LDO regulators.

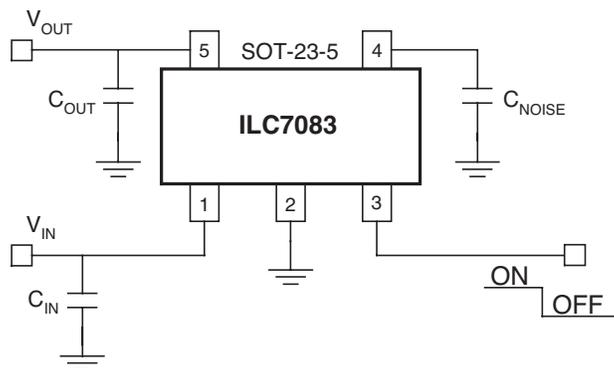
The device has been optimized to meet the needs of modern wireless communications design; Low noise, low dropout, small size, high peak current, high noise immunity.

The ILC7083 is designed to make use of low cost ceramic capacitors while outperforming other devices that require tantalum capacitors.

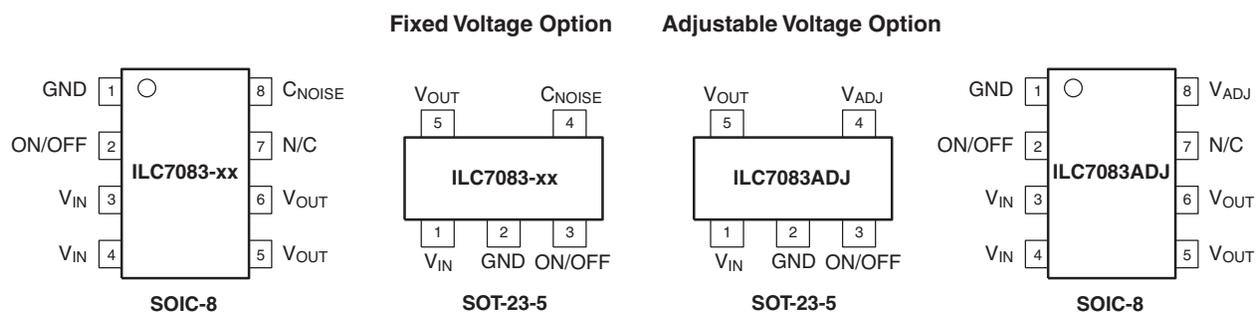
Applications

- Cellular phones
- Wireless communicators
- PDAs / palmtops / organizers
- Battery powered portable electronics

Typical Applications



Pin Assignments



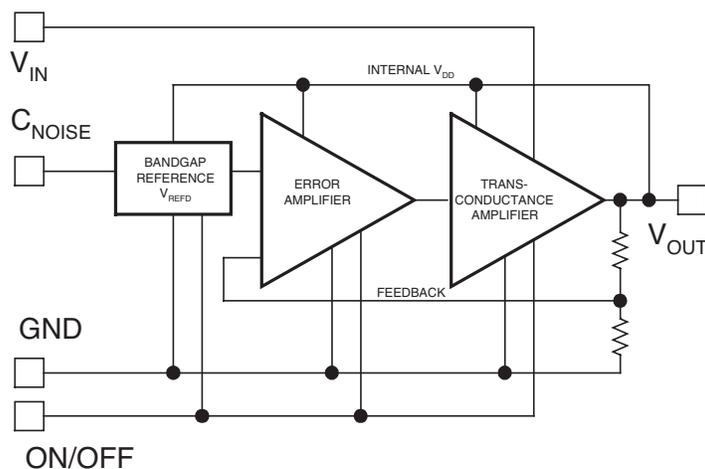
Pin Description ILC7083-xx (Fixed voltage version)

| Pin Number | | Pin Name | Pin Description |
|------------|----------|--------------------|---|
| SOIC-8 | SOT-23-5 | | |
| 3 and 4 | 1 | V _{IN} | Connect directly to supply |
| 1 | 2 | GND | Ground pin. Local ground for C _{NOISE} and C _{OUT} . |
| 2 | 3 | ON/OFF | By applying less than 0.6V to this pin the device will be turned off. |
| 8 | 4 | C _{NOISE} | Optional noise bypass capacitor may be connected between this pin and GND. Do not connect C _{NOISE} directly to the main power ground plane. |
| 5 and 6 | 5 | V _{OUT} | Output Voltage. Connect C _{OUT} between this pin and GND. |
| 7 | – | N/C | Not Connected |

Pin Description ILC7083-ADJ (Adjustable voltage version)

| Pin Number | | Pin Name | Pin Description |
|------------|----------|------------------|--|
| SOIC-8 | SOT-23-5 | | |
| 3 and 4 | 1 | V _{IN} | Connect directly to supply |
| 1 | 2 | GND | Ground pin. Local ground for C _{NOISE} and C _{OUT} . |
| 2 | 3 | ON/OFF | By applying less than 0.6V to this pin the device will be turned off. |
| 8 | 4 | V _{ADJ} | Voltage feedback pin to set the adjustable output voltage. Do not connect a capacitor to this pin. |
| 5 and 6 | 5 | V _{OUT} | Output Voltage. Connect C _{OUT} between this pin and GND. |
| 7 | – | N/C | Not Connected |

Internal Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Units |
|--------------------------------------|---------------|--------------------------|-------|
| Input Voltage | V_{IN} | -0.3 to +13.5 | V |
| On/Off Input Voltage | $V_{ON/OFF}$ | -0.3 to V_{IN} | |
| Output Current | I_{OUT} | Short circuit protected | mA |
| Output Voltage | V_{OUT} | -0.3 to $V_{IN} + 0.3$ | V |
| Package Power Dissipation (SOT-23-5) | P_D | 250 (Internally Limited) | mW |
| Maximum Junction Temp Range | $T_{J(max)}$ | -40 ~ +150 | °C |
| Storage Temperature | T_{STG} | -40 ~ +125 | °C |
| Package Thermal Resistance | θ_{JA} | 333 | °C/W |

Recommended Operating Conditions

| Parameter | Min. | Typ. | Max. | Units |
|-------------------------------|--------------------|---------------|------|-------|
| Input Voltage | $V_{OUT} + V_{DO}$ | $V_{OUT} + 1$ | 13 | V |
| Operating Ambient Temperature | -40 | | +85 | °C |

Electrical Characteristics ILC7083AIM5

Unless otherwise specified, all limits are at $T_A=25^{\circ}\text{C}$; $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1\text{V}$, $I_{\text{OUT}} = 1\text{mA}$, $C_{\text{OUT}} = 1\mu\text{F}$, $V_{\text{ON/OFF}} = 2\text{V}$.
 Boldface type denotes specifications which apply over the specified operating temperature range.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--------------------------------|---|---|-----------------------|-----------------------|-----------------------|----------------------------|
| Input Voltage Range | V_{IN} | | 2 | | 13 | V |
| Output Voltage | V_{OUT} | $1\text{mA} \leq I_{\text{OUT}} \leq 150\text{mA}$ | -3 | $V_{\text{OUT(NOM)}}$ | +3 | % $V_{\text{OUT(NOM)}}$ |
| | | $1\text{mA} \leq I_{\text{OUT}} \leq 150\text{mA}$ | -4 | $V_{\text{OUT(NOM)}}$ | +4 | |
| Feedback Voltage (ADJ version) | V_{ADJ} | | 1.217 1.204 | 1.255 | 1.292 1.305 | V |
| Line Regulation | $\frac{\Delta V_{\text{OUT}}}{(V_{\text{OUT}} \cdot \Delta V_{\text{IN}})}$ | $V_{\text{OUT(NOM)}} + 1\text{V} \leq V_{\text{IN}} \leq 12\text{V}$ | | 0.007 | 0.014 0.032 | %/V |
| Dropout Voltage (Note 3) | $V_{\text{IN}} - V_{\text{OUT}}$ | $I_{\text{OUT}} = 0\text{mA}$ (Note 4) | | 0.1 | 1 2 | mV |
| | | $I_{\text{OUT}} = 10\text{mA}$ | | 10 | 25 35 | |
| | | $I_{\text{OUT}} = 50\text{mA}$ | | 50 | 75 100 | |
| | | $I_{\text{OUT}} = 100\text{mA}$ | | 100 | 150 200 | |
| | | $I_{\text{OUT}} = 150\text{mA}$ | | 150 | 225 300 | |
| Ground Pin Current | I_{GND} | $I_{\text{OUT}} = 0\text{mA}$ | | 95 | 200 220 | μA |
| | | $I_{\text{OUT}} = 10\text{mA}$ | | 100 | 220 240 | |
| | | $I_{\text{OUT}} = 50\text{mA}$ | | 100 | 220 240 | |
| | | $I_{\text{OUT}} = 100\text{mA}$ | | 100 | 240 260 | |
| | | $I_{\text{OUT}} = 150\text{mA}$ | | 115 | 260 280 | |
| Shutdown (OFF) Current | $I_{\text{ON/OFF}}$ | $V_{\text{ON/OFF}} = 0\text{V}$ | | 0.1 | 2 | μA |
| ON/OFF Input Voltage | $V_{\text{ON/OFF}}$ | High = Regulator On Low = Regulator Off | 1.5 | | 0.6 | |
| ON/OFF Pin Input Current | $I_{\text{IN(ON/OFF)}}$ | $V_{\text{ON/OFF}} = 0.6\text{V}$, regulator OFF $V_{\text{ON/OFF}} = 2\text{V}$, regulator ON | | 0.3 1 | | μA |
| Peak Output Current (Note 4) | $I_{\text{OUT(peak)}}$ | $V_{\text{OUT}} \geq 0.95V_{\text{OUT(NOM)}}$, $t_{\text{pw}} = 2\text{ms}$ | 400 | 500 | | mA |
| Output Noise Voltage (RMS) | eN | BW = 300Hz to 50kHz, $C_{\text{IN}} = 1\mu\text{F}$ $C_{\text{NOISE}} = 0.01\mu\text{F}$, $C_{\text{OUT}} = 2.2\mu\text{F}$, $I_{\text{OUT}} = 10\text{mA}$ | | 40 | | μV_{RMS} |
| Ripple Rejection | $\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$ | $C_{\text{OUT}} = 4.7\mu\text{F}$, $I_{\text{OUT}} = 100\text{mA}$ | Freq. = 1kHz | | 85 | dB |
| | | | Freq. = 10kHz | | 70 | |
| | | | Freq. = 1MHz | | 60 | |
| Dynamic Line Regulation | $\Delta V_{\text{OUT(line)}}$ | $V_{\text{IN}}: V_{\text{OUT(NOM)}} + 1\text{V}$ to $V_{\text{OUT(NOM)}} + 2\text{V}$, $t_{\text{r/tf}} = 2\mu\text{s}$; $I_{\text{OUT}} = 150\text{mA}$ | | 14 | | mV |
| Dynamic Load Regulation | $\Delta V_{\text{OUT(load)}}$ | $I_{\text{OUT}}: 1\text{mA}$ to 150mA ; $t_{\text{r}} < 5\mu\text{s}$ | | 40 | | mV |
| Short Circuit Current | I_{SC} | $V_{\text{OUT}} = 0\text{V}$ | | 600 | | mA |

Notes:

- Absolute maximum ratings indicate limits which when exceeded may result in damage to the component. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- Specified Min/Max limits are production tested or guaranteed through correlation based on statistical control methods. Measurements are taken at constant junction temperature as close to ambient as possible using low duty pulse testing.
- Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the nominal value measured with an IV differential.
- Guaranteed by design.

Operation

The ILC7083 LDO design is based on an advanced circuit configuration for which patent protection has been applied. Typically it is very difficult to drive a capacitive output with an amplifier. The output capacitance produces a pole in the feedback path, which upsets the carefully tailored dominant pole of the internal amplifier. Traditionally the pole of the output capacitor has been “eliminated” by reducing the output impedance of the regulator such that the pole of the output capacitor is moved well beyond the gain bandwidth product of the regulator. In practice, this is difficult to do and still maintain high frequency operation. Typically the output impedance of the regulator is not simply resistive, such that the reactive output impedance interacts with the reactive impedance of the load resistance and capacitance. In addition, it is necessary to place the dominant pole of the circuit at a sufficiently low frequency such that the gain of the regulator has fallen below unity before any of the complex interactions between the output and the load occur. The ILC7083 does not try to eliminate the output pole, but incorporates it into the stability scheme. The load and output capacitor forms a pole, which rolls off the gain of the regulator below unity. In order to do this the output impedance of the regulator must be high, looking like a current source. The output stage of the regulator becomes a transconductance amplifier, which converts a voltage to a current with a substantial output impedance. The circuit which drives the transconductance amplifier is the error amplifier, which compares the regulator output to the band gap reference and produces an error voltage as the input to the transconductance amplifier. The error amplifier has a dominant pole at low frequency and a “zero” which cancels out the effects of the pole. The zero allows the regulator to have gain out to the frequency where the output pole continues to reduce the gain to unity. The configuration of the poles and zero are shown in Figure 1. Instead of powering the critical circuits from the unregulated input voltage, the CMOS RF LDO powers the internal circuits such as the bandgap, the error amplifier and most of the transconductance amplifier from the boot strapped regulated output voltage of the regulator. This technique offers extremely high ripple rejection and excellent line transient response.

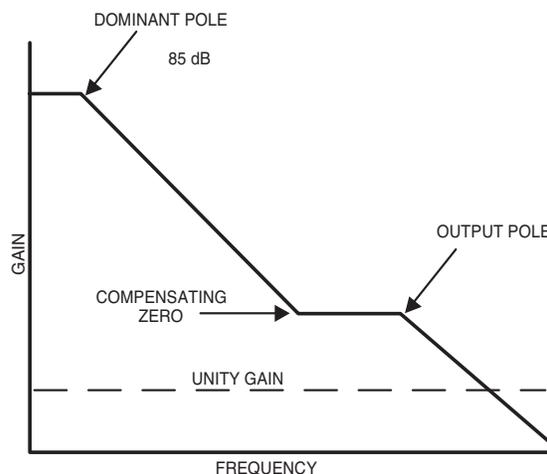


Figure 1. ILC7083 RF LDO Frequency Response

A block diagram of the regulator circuit used in the ILC7083 is shown in Figure 2, which shows the input-to-output isolation and the cascaded sequence of amplifiers that implement the pole-zero scheme outlined above.

The ILC7083 is designed in a CMOS process with some minor additions, which allow the circuit to be used at input voltages up to 13V. The resulting circuit exceeds the frequency response of traditional bipolar circuits. The ILC7083 is very tolerant of output load conditions with the inclusion of both short circuit and thermal overload protection. The device has a very low dropout voltage, typically a linear response of 1mV per milliamp of load current, and none of the quasi-saturation characteristics of a bipolar output devices. All the good features of the frequency response and regulation are valid right to the point where the regulator goes out of regulation in a 4 millivolt transition region. Because there is no base drive, the regulator is capable of providing high current surges while remaining in regulation. This is shown in the high peak current of 500mA which allows for the ILC7083 to be used in systems that require short burst mode operation.

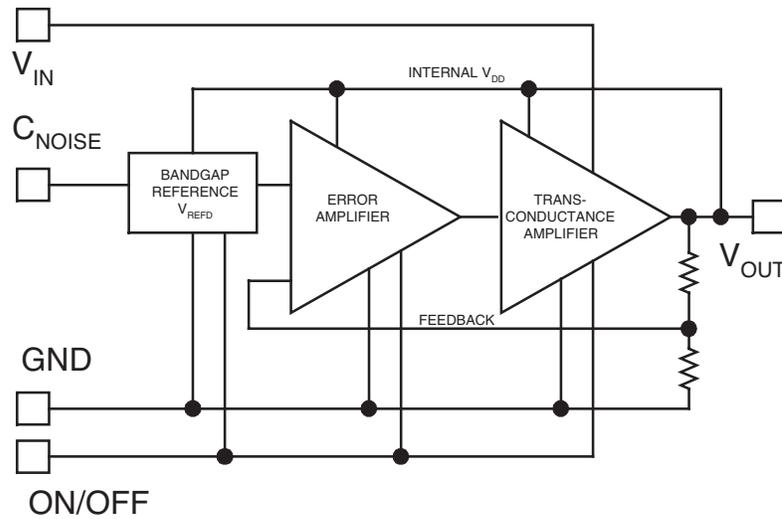


Figure 2. ILC7083 RF LDO Regulator Block Diagram

Shutdown (ON/OFF) Operation

The ILC7083 output can be turned off by applying 0.6V or less to the device’s ON/OFF pin (pin 3). In shutdown mode, the ILC7083 draws less than 1mA quiescent current. The output of the ILC7083 is enabled by applying 1.5V to 13V at the ON/OFF pin. In applications where the ILC7083 output will always remain enabled, the ON/OFF pin may be connected to V_{IN} (pin 1). The ILC7083’s shutdown circuitry includes hysteresis, as such the device will operate properly even if a slow moving signal is applied to the ON/OFF pin.

Short Circuit Protection

The ILC7083 output can withstand momentary short circuit to ground. Moreover, the regulator can deliver very high output peak current due to its 1A instantaneous short circuit current capability.

Thermal Protection

The ILC7083 also includes a thermal protection circuit which shuts down the regulator when die temperature exceeds 150°C due to overheating. In thermal shutdown, once the die temperature cools to below 140°C, the regulator is enabled. If the die temperature is excessive due to high package power dissipation, the regulator’s thermal circuit will continue to pulse the regulator on and off. This is called thermal cycling.

Excessively high die temperature may occur due to high differential voltage across the regulator or high load current or high ambient temperature or a combination of all three. Thermal protection protects the regulator from such fault conditions and is a necessary requirement in today’s designs. In normal operation, the die temperature should be limited to under 150°C.

Adjustable Output Voltage

Figure 5 shows how an adjustable output voltage can be easily achieved using ILC7083-ADJ. The output voltage, V_{OUT} is given by the following equation:

$$V_{OUT} = 1.255V \times (R1/R2 + 1)$$

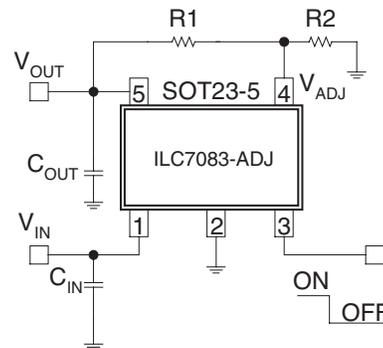


Figure 3. Application Circuit for Adjustable Output Voltage

For best results, a resistor value of 470kΩ or less may be used for R2. The output voltage can be programmed from 2.5V to 12V.

Note that an external capacitor should not be connected to the adjustable feedback pin (pin 4). Connecting an external capacitor to pin 4 may cause regulator instability and lead to oscillations.

Maximum Output Current

The maximum output current available from the ILC7083 is limited by the maximum package power dissipation as well as the device's internal current limit. For a given ambient temperature, T_A , the maximum package power dissipation is given by:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)} = 150^\circ\text{C}$ is the maximum junction temperature and $\theta_{JA} = 333^\circ\text{C/W}$ is the package thermal resistance. For example at $T_A = 85^\circ\text{C}$ ambient temperature, the maximum package power dissipation is;

$$P_{D(MAX)} = 195\text{mW.}$$

The maximum output current can be calculated from the following equation:

$$I_{OUT(MAX)} < P_{D(MAX)} / (V_{IN} - V_{OUT})$$

For example at $V_{IN} = 6\text{V}$, $V_{OUT} = 5\text{V}$ and $T_A = 85^\circ\text{C}$, the maximum output current is $I_{OUT(MAX)} < 195\text{mA}$. At higher output current, the die temperature will rise and cause the thermal protection circuit to be enabled.

Application Hints

Figure 4 shows the typical application circuit for the ILC7083.

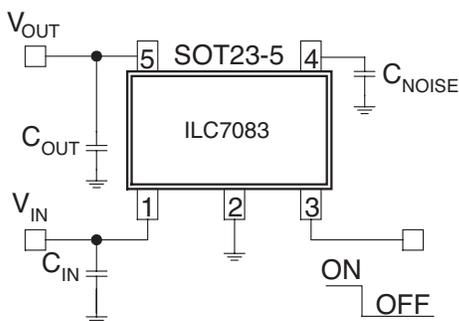


Figure 4. Basic Application Circuit for Fixed Output Voltage Versions

Input Capacitor

An input capacitor C_{IN} of value $1\mu\text{F}$ or larger should be connected from V_{IN} to the main ground plane. This will help to filter supply noise from entering the LDO. The input capacitor should be connected as close to the LDO regulator input pin as is practical. Using a high-value input capacitor will offer superior line transient response as well as better power supply ripple rejection. A ceramic or tantalum capacitor may be used at the input of the LDO regulator.

Note that there is a parasitic diode from the LDO regulator output to the input. If the input voltage swings below the regulator's output voltage by a couple of hundred millivolts then

the regulator may be damaged. This condition must be avoided. In many applications a large value input capacitor, C_{IN} , will hold V_{IN} higher than V_{OUT} and decay slower than V_{OUT} when the LDO is powered off.

Output Capacitor Selection

Fairchild strongly recommends the use of low ESR (equivalent series resistance) ceramic capacitors for C_{OUT} and C_{NOISE} . The ILC7083 is stable with low ESR capacitor (as low as zero Ω). The value of the output capacitor should be $1\mu\text{F}$ or higher. Either ceramic chip or a tantalum capacitor may be used at the output.

Use of ceramic chip capacitors offer significant advantages over tantalum capacitors. A ceramic capacitor is typically cheaper than a tantalum capacitor, it usually has a smaller footprint, lower height, and lighter weight than a tantalum capacitor. Furthermore, unlike tantalum capacitors which are polarized and can be damaged if connected incorrectly, ceramic capacitors are non-polarized. Low value ceramic chip capacitors with X5R or X7R dielectric are available in the 100pF to $4.7\mu\text{F}$ range. Beware of using ceramic capacitors with Y5V dielectric since their ESR increases significantly at cold temperatures. Figure 12 shows a list of recommended ceramic capacitors for use at the output of ILC7083.

Note: If a tantalum output capacitor is used then for stable operation. We recommend a low ESR tantalum capacitor with maximum rated ESR at or below 0.4Ω . Low ESR tantalum capacitors, such as the TPS series from AVX Corporation (www.avxcorp.com) or the T495 series from Kemet (www.kemet.com) may be used.

In applications where a high output surge current can be expected, use a high value but low ESR output capacitor for superior load transient response. The ILC7083 is stable with no load.

Noise Bypass Capacitor

In low noise applications, the self noise of the ILC7083 can be decreased further by connecting a capacitor from the noise bypass pin (pin 4) to ground (pin 2). The noise bypass pin is a high impedance node as such care should be taken in printed circuit board layout to avoid noise pick-up from external sources. Moreover, the noise bypass capacitor should have low leakage.

Noise bypass capacitors with a value as low as 470pF may be used. However, for optimum performance, use a $0.01\mu\text{F}$ or larger, ceramic chip capacitor. Note that the turn on and turn off response of the ILC7083 is inversely proportional to the value of the noise bypass capacitor. For fast turn on and turn off, use a small value noise bypass capacitor. In applications where exceptionally low output noise is not required, consider omitting the noise bypass capacitor altogether.

The Effects of ESR (Equivalent Series Resistance)

The ESR of a capacitor is a measure of the resistance due to the leads and the internal connections of the component. Typically measured in mΩ (milli-ohms) it can increase to ohms in some cases.

Wherever there is a combination of resistance and current, voltages will be present. The control functions of LDOs use two voltages in order to maintain the output precisely; V_{OUT} and V_{REF} .

With reference to the block diagram in Figure 4, V_{OUT} is fed back to the error amplifier and is used as the supply voltage for the internal components of the ILC7083. So any change in V_{OUT} will cause the error amplifier to try to compensate to maintain V_{OUT} at the set level and noise on V_{OUT} will be reflected into the supply of each internal component of the ILC7083. So any change in V_{OUT} will cause the error amplifier to try to compensate to maintain V_{OUT} at the set level and noise on V_{OUT} will be reflected into the supply of each internal circuit. The reference voltage, V_{REF} is influenced by the C_{NOISE} pin. Noise into this pin will add to the reference voltage and be fed through the circuit. These factors will not cause a problem if some simple steps are taken. Figure 5 shows where these added ESR resistances are present in the typical LDO circuit.

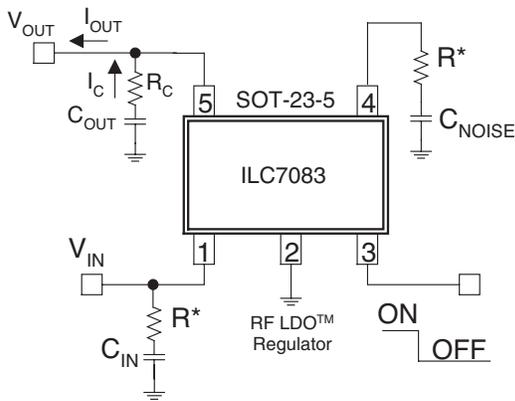


Figure 5. ESR Present in C_{OUT} and C_{NOISE}

With this in mind low ESR components will offer better performance where the LDO may be subjected to large load transients current. ESR is less of a problem with C_{IN} as the voltage fluctuations at the input will be filtered by the LDO.

However, being aware of these current flows, there is also another potential source of induced voltage noise from the resistance inherent in the PCB trace. Figure 6 shows where the additive resistance of the PCB can manifest itself. Again

these resistances may be very small, but a summation of several currents can develop detectable voltage ripple and will be amplified by the LDO. Particularly the accumulation of current flows in the ground plane can develop significant voltages unless care is taken. With a degree of care, the ILC7083 will yield outstanding performance.

Printed Circuit Board Layout Guidelines

As was mentioned in the previous section, to take full advantage of any high performance LDO regulator requires paying careful attention to grounding and printed circuit board (PCB) layout.

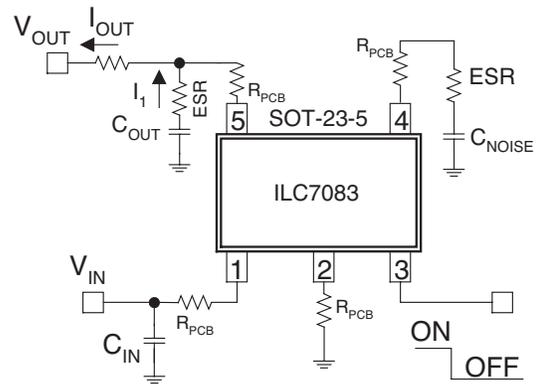


Figure 6. Inherent PCB resistance

Figure 7 shows the effects of poor grounding and PCB layout magnified by the ESR and PCB resistances and the accumulation of current flows.

Note that particularly during high output load current, the LDO regulator's ground pin and the ground return for C_{OUT} and C_{NOISE} are not at the same potential as the system ground. This is due to high frequency impedance caused by PCB's trace inductance and DC resistance. The current loop between C_{OUT} , C_{NOISE} and the LDO regulator's ground pin will degrade performance of the LDO.

Figure 8 shows an optimum schematic. In this schematic, high output surge current has little effect on the ground current and noise bypass current return of the LDO regulator. Note that the key difference here is that C_{OUT} and C_{NOISE} are directly connected to the LDO regulator's ground pin. The LDO is then separately connected to the main ground plane and returned to a single point system ground.

The layout of the LDO and its external components are also based on some simple rules to minimize EMI and output voltage ripple.

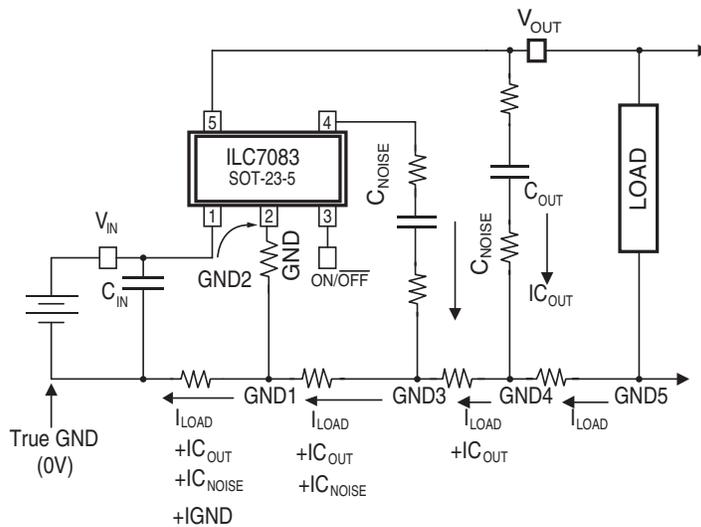


Figure 7. Effects of Poor Circuit Layout

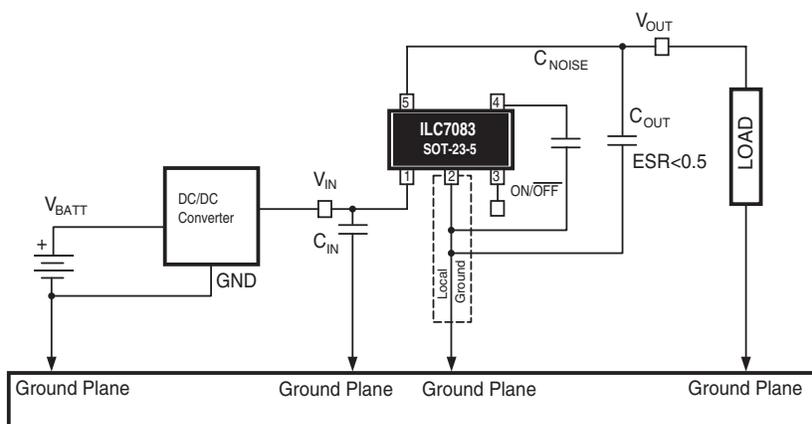


Figure 8. Recommended Application Circuit Schematic

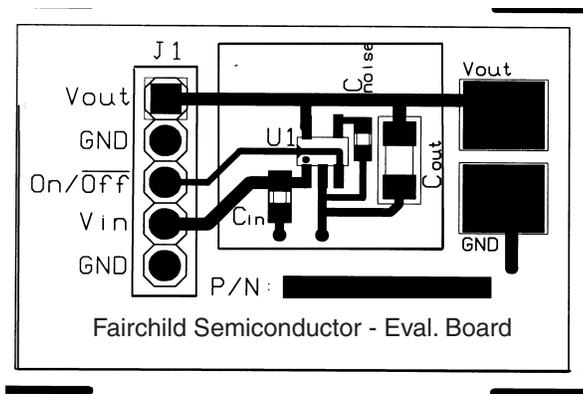


Figure 9. Recommended Application Circuit Layout (not drawn to scale)

Note, ground plane is bottom layer of PCB and connects to top layer ground connections through vias.

Evaluation Board Parts List (for Figure 9)

| Label | Part Number | Manufacturer | Description |
|--------|------------------|-------------------------|---|
| U1 | ILC7083AIM5-30 | Fairchild Semiconductor | 150mA RF LDO™ regulator |
| J1 | 69190-405 | Berg | Connector, four position header |
| Cin | GRM40 Y5V 105Z16 | muRata | Ceramic capacitor, 1 μ F, 16V, SMT (size 0805) |
| Cnoise | ECU-V1H103KBV | Panasonic | Ceramic capacitor, 0.01 μ F, 16V, SMT (size 0603) |
| Cout | GRM42-6X5R475K10 | muRata | Ceramic capacitor, 4.7 μ F, 16V, SMT (size 1206) |

Grounding Recommendations

1. Connect C_{IN} between V_{IN} of the ILC7083 and the “GROUND PLANE”.
2. Keep the ground side of C_{OUT} and C_{NOISE} connected to the “LOCAL GROUND” and not directly to the “GROUND PLANE”.
3. On multilayer boards use component side copper for grounding around the ILC7083 and connect back to a “GROUND PLANE” using vias.
4. If using a DC-DC converter in your design, use a star grounding system with separate traces for the power ground and the control signals. The star should radiate from where the power supply enters the PCB.

Layout Considerations

1. Place all RF LDO related components; ILC7083, input capacitor C_{IN} , noise bypass capacitor C_{NOISE} and output capacitor C_{OUT} as close together as possible.
2. Keep the output capacitor C_{OUT} as close to the ILC7083 as possible with very short traces to the V_{OUT} and GND pins.
3. The traces for the related components; ILC7083, input capacitor C_{IN} , noise bypass capacitor C_{NOISE} and output capacitor C_{OUT} can be run with minimum trace widths close to the LDO.
4. Maintain a separate “LOCAL GROUND” remote from the “GROUND PLANE” to ensure a quiet ground near the LDO.

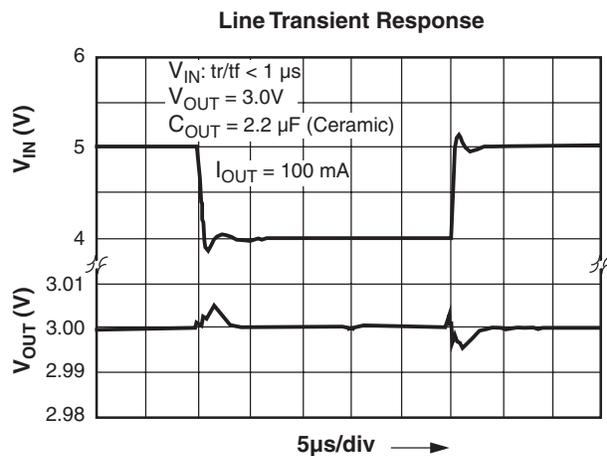
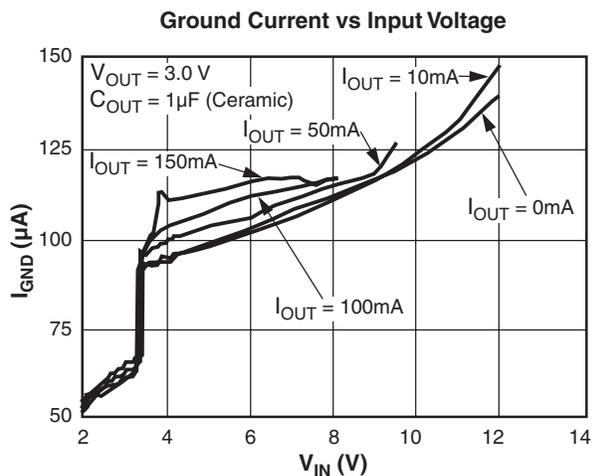
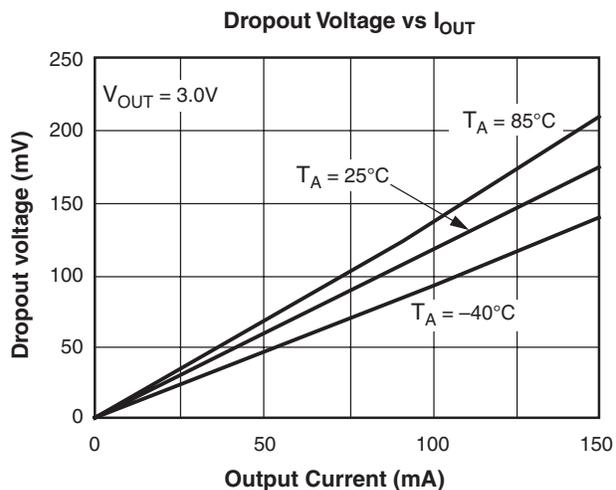
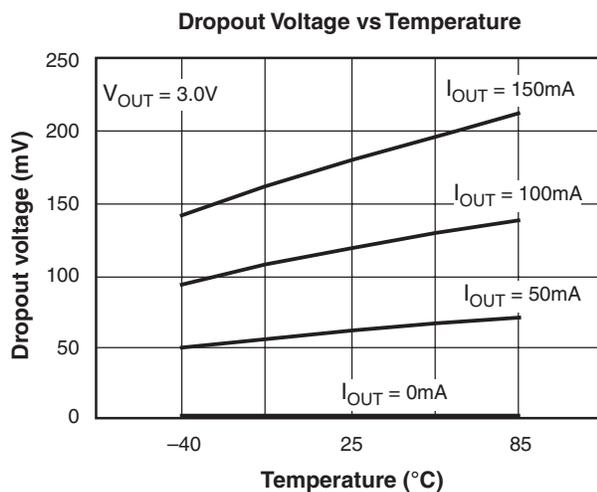
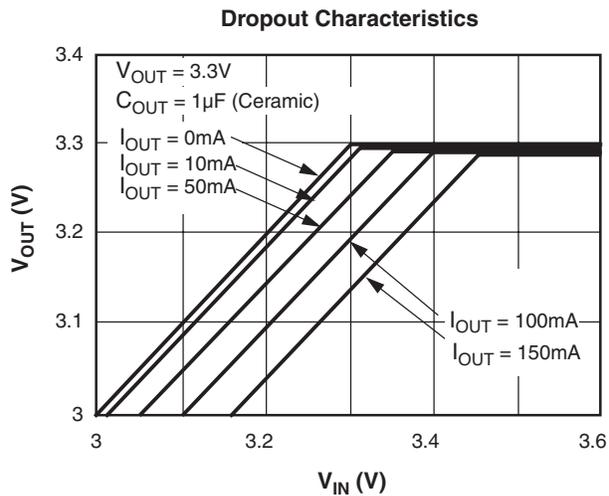
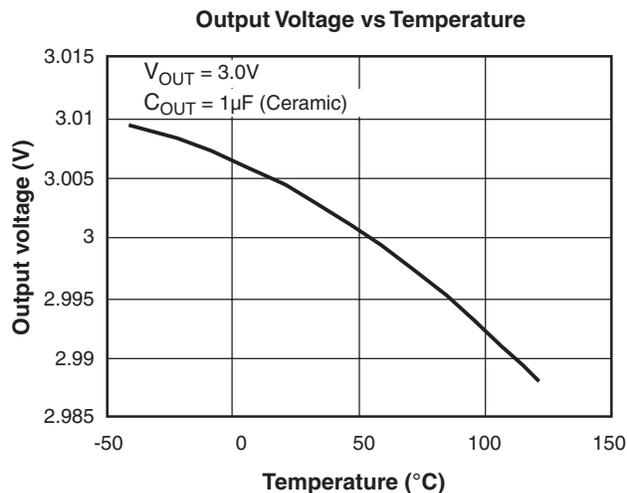
Figure 9 shows how this circuit can be translated into a PCB layout.

Recommended Ceramic Output Capacitors

| C_{OUT} | Capacitor Size | I_{OUT} | Dielectric | Part Number | Capacitor Vendor |
|-------------|----------------|------------|------------|-------------------|------------------|
| 1 μ F | 0805 | 0 to 150mA | X5R | C2012X5R1A105KT | TDK |
| | 0805 | | X7R | GRM40X7R105K010 | muRata |
| | 0805 | | X7R | LMK212BJ105KG | Taiyo-Yuden |
| | 1206 | | X7R | GRM42-6X7R105K016 | muRata |
| | 1206 | | X7R | EMK316BJ105KL | Taiyo-Yuden |
| | 1206 | | X5R | TMK316BJ105KL | Taiyo-Yuden |
| 2.2 μ F | 0805 | 0 to 150mA | X5R | GRM40X5R225K 6.3 | muRata |
| | 0805 | | X5R | C2012X5R0J225KT | TDK |
| | 1206 | | X5R | EMK316BJ225ML | Taiyo-Yuden |
| 4.7 μ F | 1206 | 0 to 150mA | X5R | GRM42-6X5R475K010 | muRata |
| | 1206 | | X7R | LMK316BJ475ML | Taiyo-Yuden |

Typical Performance Characteristics ILC7083

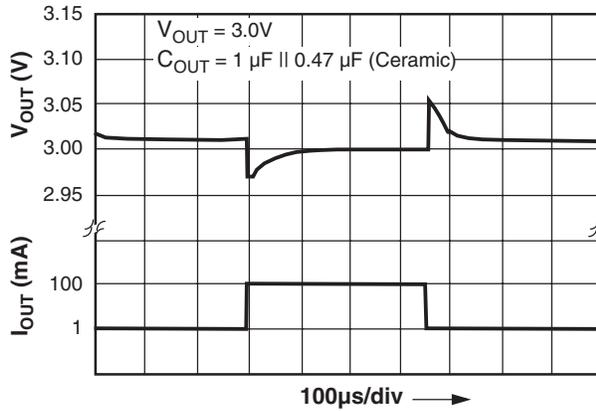
Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{V}$, ON/OFF pin tied to V_{IN}



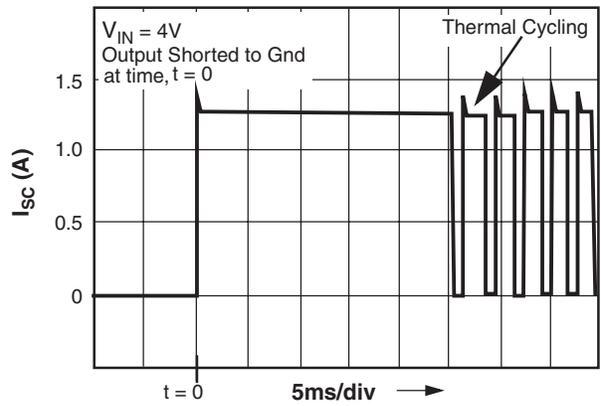
Typical Performance Characteristics ILC7083

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{V}$, ON/OFF pin tied to V_{IN}

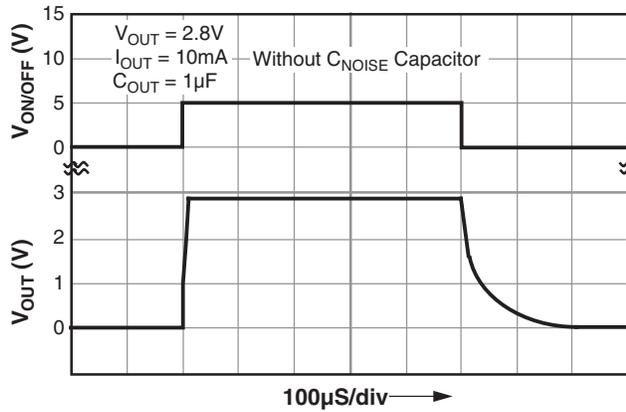
Load Transient Response



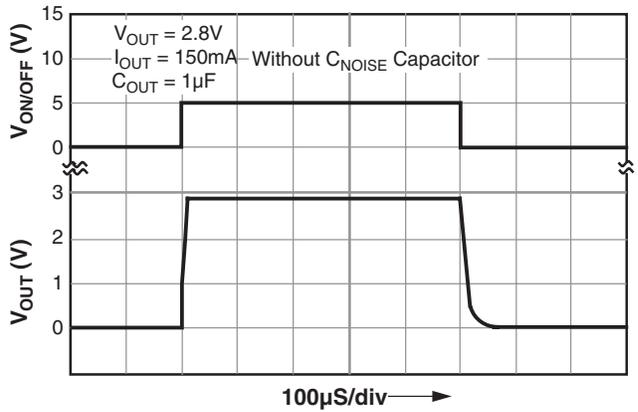
Short Circuit Current



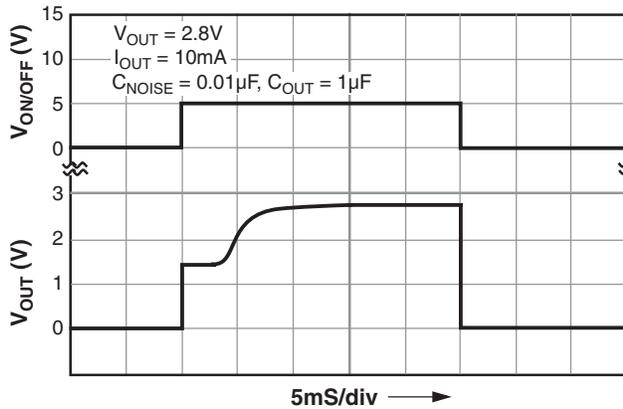
On/Off Transient Response



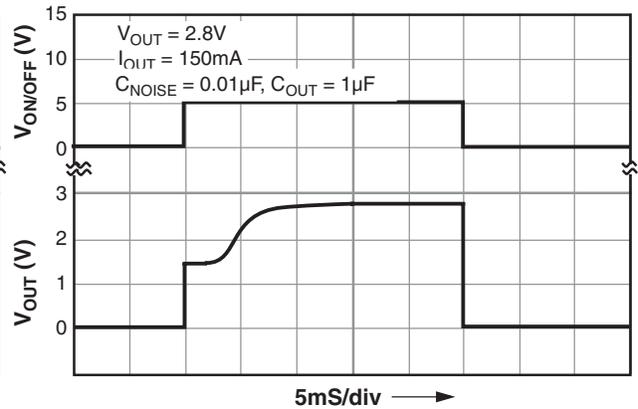
On/Off Transient Response



On/Off Transient Response

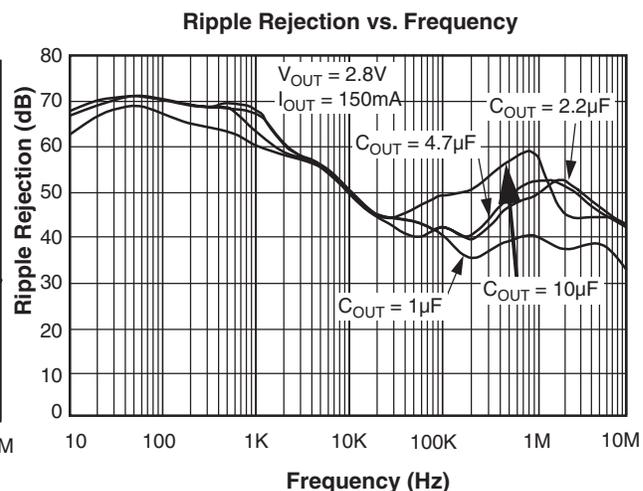
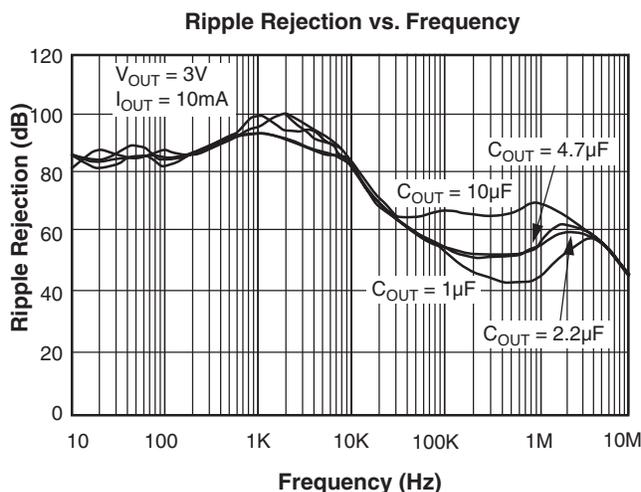
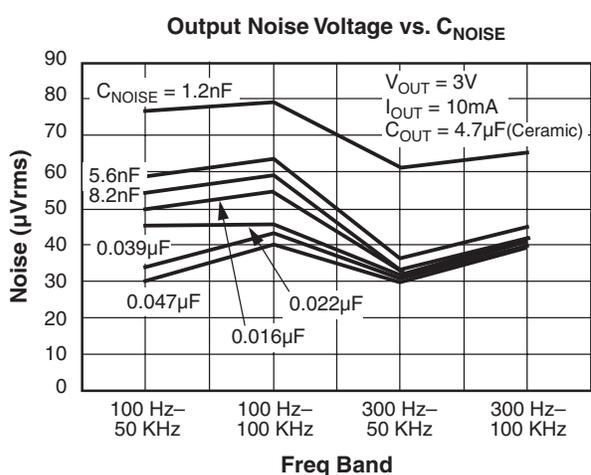
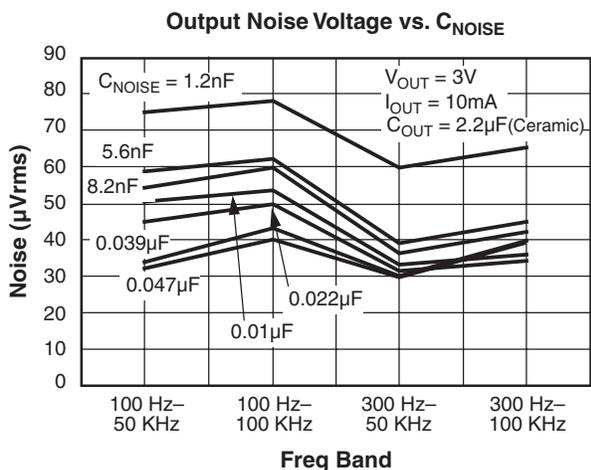
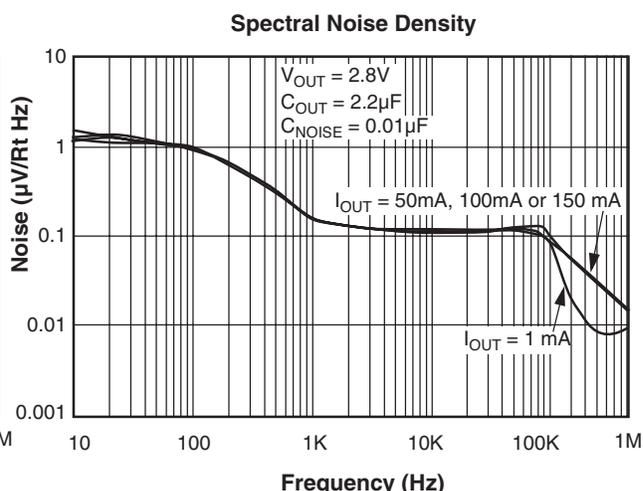
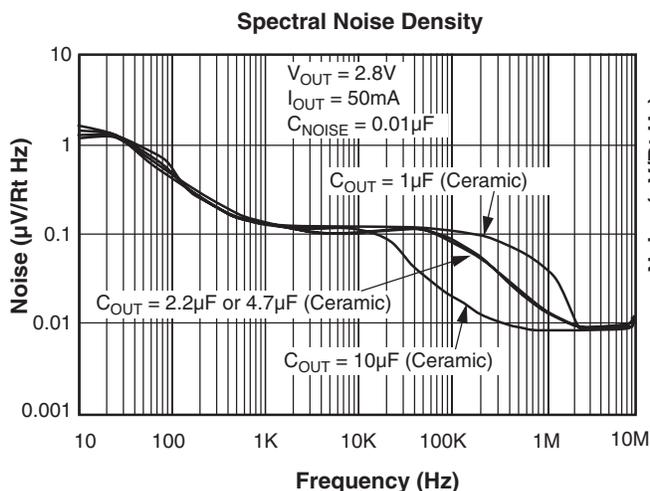


On/Off Transient Response



Typical Performance Characteristics ILC7083

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 1\text{V}$, ON/OFF pin tied to V_{IN}



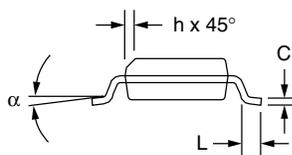
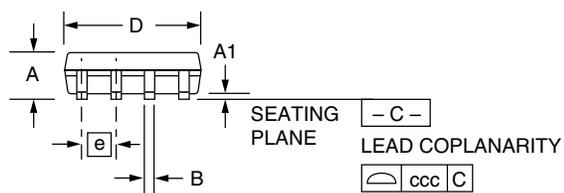
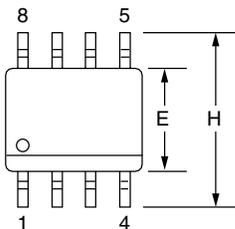
Mechanical Dimensions

8-Lead Plastic Surface Mount (SOIC)

| Symbol | Inches | | Millimeters | | Notes |
|----------|----------|------|-------------|------|-------|
| | Min. | Max. | Min. | Max. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .0075 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| α | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

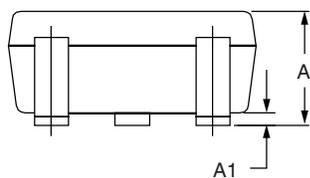
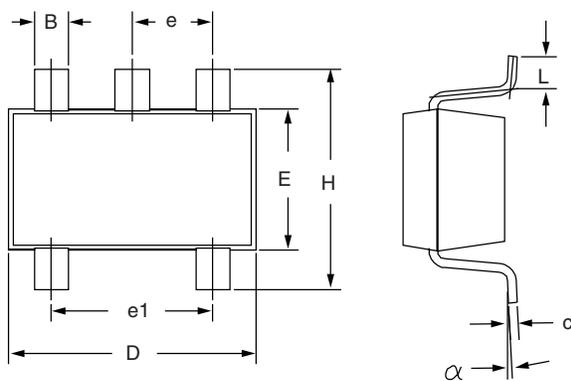


5-Lead Plastic Surface Mount (SOT-23-5)

| Symbol | Inches | | Millimeters | | Notes |
|----------|----------|------|-------------|------|-------|
| | Min. | Max. | Min. | Max. | |
| A | .035 | .057 | .90 | 1.45 | |
| A1 | .000 | .006 | .00 | .15 | |
| B | .008 | .020 | .20 | .50 | |
| c | .003 | .010 | .08 | .25 | |
| D | .106 | .122 | 2.70 | 3.10 | |
| E | .059 | .071 | 1.50 | 1.80 | |
| e | .037 BSC | | .95 BSC | | |
| e1 | .075 BSC | | 1.90 BSC | | |
| H | .087 | .126 | 2.20 | 3.20 | |
| L | .004 | .024 | .10 | .60 | |
| α | 0° | 10° | 0° | 10° | |

Notes:

1. Package outline exclusive of mold flash & metal burr.
2. Package outline exclusive of solder plating.
3. EIAJ Ref Number SC-74A.



Ordering Information ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

| Part Number | Output Voltage (V) | Package |
|-----------------|--------------------|----------|
| ILC7083AIM530X | 3.0 | SOT-23-5 |
| ILC7083AIM5ADJX | Adjustable | SOT-23-5 |
| ILC7083AIK530 | 3.0 | SOIC-8 |
| ILC7083AIK5ADJ | Adjustable | SOIC-8 |

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.