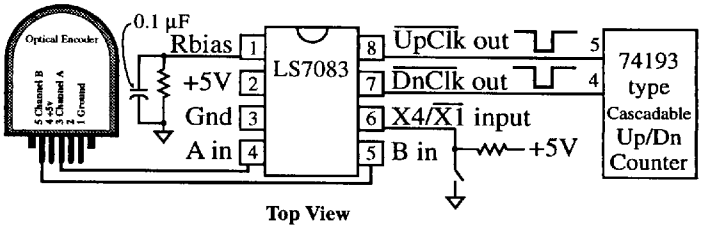
LS7083 Encoder to Counter Interface Chips
LS7084

Technical Data, rev. 1.08, June 1994

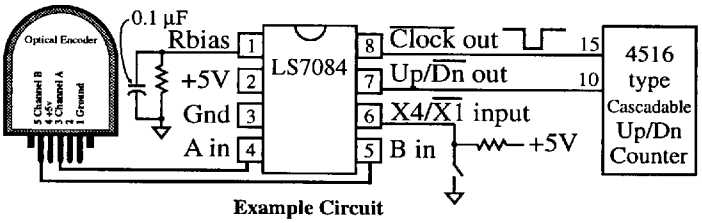
Quadrature Clock Converters

Features:

- X4 or X1 resolution multiplication
- TTL and CMOS compatible
- Low power (micro-amps)
- 8-pin DIP package
- No external clocks required
- Drive standard Up/Dn counters
- Monolithic CMOS



Top View



Example Circuit

Description:

These devices allow incremental shaft encoders to drive standard up/down counters. Connect the encoder quadrature outputs to the A & B inputs. The LS7083 outputs can connect directly to the up and down clock inputs of counters such as 74193 or 40193. The LS7084 outputs can connect directly to the Clock and Up/Dn inputs of counters such as 4516 or 74169.

Pin Descriptions

Pin 1 (Rbias input):
Connect a 0.1 µF bypass capacitor and resistor to ground for the internal current mirror which feeds the two internal dual one-shots. The resistor value sets the width of the low-true clock outputs. A typical value is 300kΩ which sets the output pulse width to 1µSec and max A,B frequency to 250kHz. Minimum resistor value is 50kΩ. See the Rbias table (next page) for other values. The chip current consumption is inversely proportional to this resistance. Typical current is 40µAmp @ 100KΩ and 6µAmp @ 2MegΩ.

Pins 4 & 5 (A & B inputs):
Connect to the A & B quadrature outputs of the encoder. Both inputs have debounce filters. Minimum pulse width is set at 160nSec. There is no maximum limit. Input current is less than 1 µAmp. The A&B inputs can be swapped to reverse the direction of the external counters.

Pin 6 (X4/X1 input):
A high level applied to this input selects X4 mode, a low level selects the X1 mode. Input current is less than 1µAmp. Do not let this input float. In X4 mode, a clock pulse is generated for every transition of the A or B input. Note that there are 4 transition per cycle of quadrature code. Thus, a 500 cycle/rev encoder will produce 2000 counts/rev in X4 mode. In X1 mode, only one clock is generated per quadrature cycle.

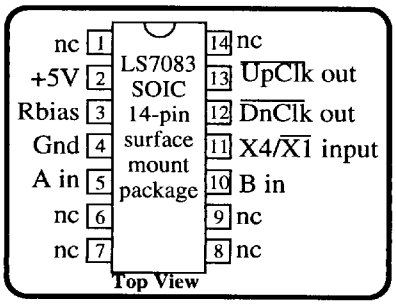
LS7083 pin 7 (Down Clock output):
Normally high, low-true. The low level pulse width is set by pin 1. Down counts are enabled only when B leads A (clockwise rotation). In X4 mode, one pulse is generated for each A/B state change. In X1 mode, one pulse is generated per quadrature cycle.

LS7084 pin 7 (Up/Down Clock output):
This output steers the external counter up or down. High = Up (A leads B), Low = Down (B leads A).

LS7083 pin 8 (Up Clock output):
Normally high, Low-true. The low level pulse width is set by pin 1. Up counts are enabled only when A leads B (counter-clockwise rotation). In X4 mode, one pulse is generated for each A/B state change. In X1 mode, one pulse is generated per quadrature cycle.

LS7084 pin 8 (Clock output):
Normally high, Low-true. The low level pulse width is set by pin 1. In X4 mode, one pulse is generated for each A/B state change regardless of count direction. In X1 mode, one pulse is generated per quadrature cycle. The external counter should count on the rising (high-going) edge of this output.

Surface Mount Package:
The LS7083 is also available in a 14-pin SOIC surface mopunt package shown below. The die is too large to fit in an 8-pin surface mount package..



Top View

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9004685 0000001 021

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Operating Temperature	0	70	°C
Storage Temperature	-65	150	°C
Voltage at any input	-.5	VCC+.5	Volts
Supply Voltage (Vcc)		13	Volts

Rbias Resistor Value vs Timing

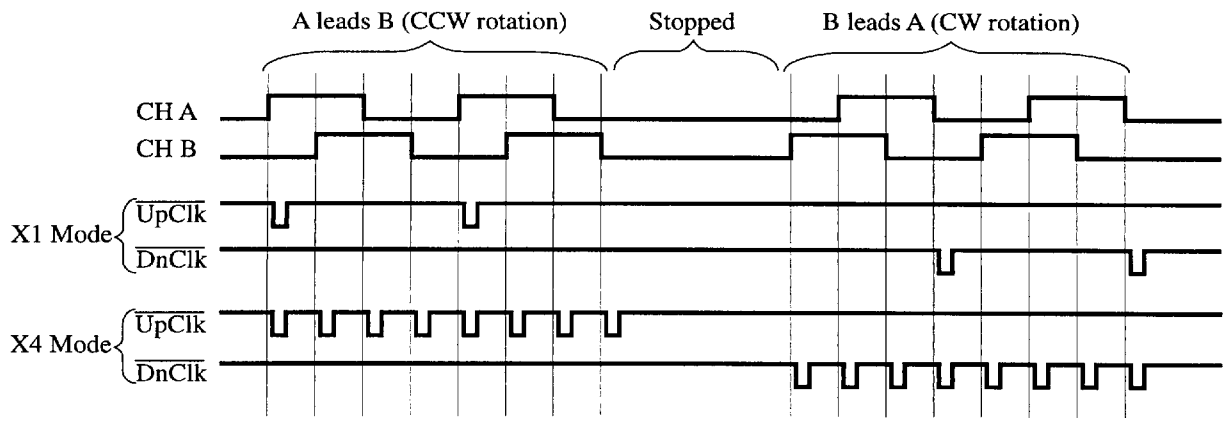
Resistor Ω	Pulse Width	Max A,B Freq
100k	400nSec	625kHz
300k	1µSec	250kHz
500k	1.4µSec	180kHz
2Meg	5µSec	50kHz
10Meg	25µSec	10kHz

DC Electrical Characteristics for 5v Operation

Parameter	Min.	Max.	Units	Notes
Supply Voltage	4.75	5.25	Volts	
Supply Current	-	8	µAmps	A,B = 0Hz Rbias=300K
X4/X1 Logic Low		1.4	Volts	
X4/X1 Logic High	3.7		Volts	
A,B Logic Low		0.6	Volts	
A,B Logic High	3.3		Volts	
Logic Low Output Current	1.75		mA	Vout = 0.4V
Logic High Output Current	1.0		mA	Vout = 4.5V

Use standard CMOS levels when operating with higher supply voltages up to 12v.

LS7083 Timing Diagram



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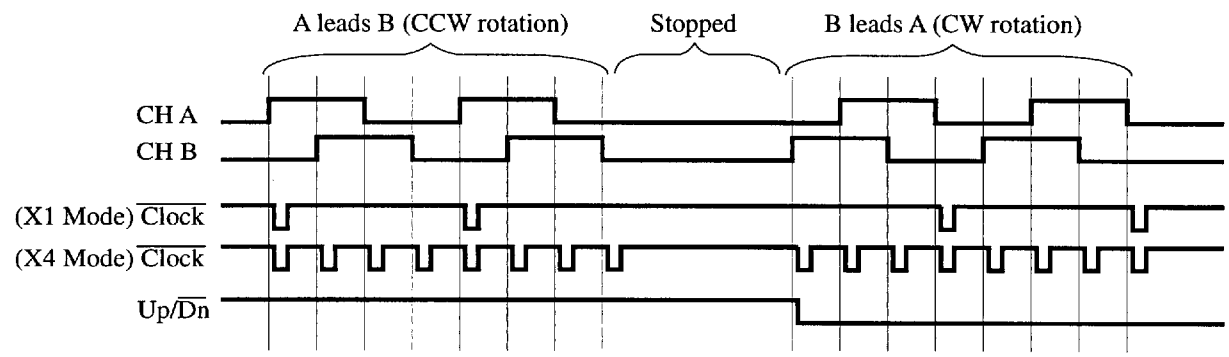

Timing Diagram Notes:
The maximum time delay from the A or B input to the leading edge of any output is 235nSec.

The pulse width of all clock outputs is set by the value of the Rbias resistor as shown in the table above.

Typical rise or fall time of each logic output 10 to 20 nSec.

Price: LS7083 or LS7084
$1.02/10K
$1.20/5K
$1.40/1K
$1.65/500
$1.95/100
$2.45/25-99
$3.05/1-24

Add $0.35 for 14-pin SOIC surface mount package

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