19-2238; Rev 0; 10/01

EVALUATION KIT AVAILABLE

MAXIM

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

General Description

The MAX5904–MAX5909 +1V to +13.2V dual hot-swap controllers provide complete protection for dual-supply systems. They allow the safe insertion and removal of circuit cards into live backplanes.

The discharged filter capacitors of the circuit card provide low impedance to the live backplane. High inrush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. The MAX5904 family of hot-swap controllers prevents such problems by gradually ramping up the output voltage and regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, as well as immunity against system noise and load transients. In the event of a fault condition, the load is disconnected. The MAX5905/MAX5907/MAX5909 must be unlatched after a fault, and the MAX5904/MAX5906/MAX5908 automatically restart after a fault.

The MAX5904 family offers a variety of options to reduce component count and design time. All devices integrate an on-board charge pump to drive the gates of low-cost, external N-channel MOSFETs. The devices offer integrated features like startup current regulation and current glitch protection to eliminate external timing resistors and capacitors. The MAX5906–MAX5909 provide an open-drain status output, an adjustable startup timer, an adjustable current limit, an uncommitted comparator, and output undervoltage/overvoltage monitoring.

The MAX5904/MAX5905 are available in 8-pin SO packages. The MAX5906–MAX5909 are available in space-saving 16-pin QSOP packages. All devices are specified over the extended temperature range, -40°C to +85°C.

Applications

Basestation Line Cards

Network Switches or Routers

Solid-State Circuit Breaker

Power-Supply Sequencing

Hot Plug-In Daughter Cards

RAID

Portable Computer Device Bays

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Selector Guide and Typical Operating Circuits appear at end of data sheet.

Features

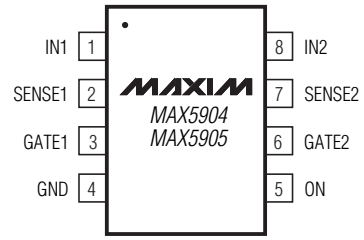
- ♦ **Safe Hot Swap for +1V to +13.2V Power Supplies**
- ♦ **Low 25mV Default Current-Limit Threshold**
- ♦ **Internal Charge Pumps Generate N-Channel MOSFET Gate Drives**
- ♦ **Inrush Current Regulated at Startup**
- ♦ **Circuit Breaker Function**
- ♦ **Adjustable Circuit Breaker/Current-Limit Threshold**
- ♦ **VariableSpeed/BiLevel Circuit-Breaker Response**
- ♦ **Auto-Retry or Latched Fault Management**
- ♦ **On/Off Sequence Programming**
- ♦ **Status Output Indicates Fault/Safe Condition**
- ♦ **Output Undervoltage and Overvoltage Monitoring and/or Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5904ESA	-40°C to +85°C	8 SO
MAX5905ESA	-40°C to +85°C	8 SO
MAX5906EEE	-40°C to +85°C	16 QSOP
MAX5907EEE	-40°C to +85°C	16 QSOP
MAX5908EEE	-40°C to +85°C	16 QSOP
MAX5909EEE	-40°C to +85°C	16 QSOP

Pin Configurations

TOP VIEW



NARROW SO

Pin Configurations continued at end of data sheet.

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

ABSOLUTE MAXIMUM RATINGS

IN_ to GND .....+14V
GATE_ to GND .....+0.3V to ($V_{IN\_}$ + 6.2V)
ON, PGOOD, COMP+, COMPOUT, TIM to GND .....-0.3V to the higher of (V_{IN1} + 0.3V) and (V_{IN2} + 0.3V)
SENSE_, MON_, LIM_ to GND .....-0.3V to ($V_{IN\_}$ + 0.3V)
Current into Any Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Narrow SO (derate 5.9mW/°C above +70°C) 471mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = +1V to +13.2V provided at least one supply is higher than +2.7V, V_{ON} = +2.7V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN1} = +5V, V_{IN2} = +3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
IN_ Input Voltage Range	$V_{IN\_}$	Other V_{IN} = +2.7V		1.0		13.2	V
Supply Current	I_{IN}	I_{IN1} + I_{IN2}			1.2	2.3	mA
CURRENT CONTROL							
Slow-Comparator Threshold (V_{IN} - V_{SENSE}) (Note 2)	$V_{SC,TH}$	MAX5904/MAX5905	T_A = +25°C	22.5	25	27.5	mV
			T_A = -40°C to +85°C	20.5		27.5	
		MAX5906–MAX5909	LIM = GND	22.5	25	27.5	
			R_{LIM} = 300kΩ	80	100	125	
Slow-Comparator Response Time (Note 3)	t_{SCD}	1mV overdrive			3		ms
		50mV overdrive			110		µs
Fast-Comparator Threshold	$V_{SU,TH}$	$V_{IN\_}$ - $V_{SENSE\_}$; during startup			2 x $V_{SC, TH}$		mV
	$V_{FC,TH}$	$V_{IN\_}$ - $V_{SENSE\_}$; normal operation			4 x $V_{SC, TH}$		
Fast-Comparator Response Time	t_{FCD}	10mV overdrive, from overload condition			260		ns
SENSE Input Bias Current	$I_{B\ SEN}$	$V_{SEN\_}$ = $V_{IN\_}$			0.03	6	µA
MOSFET DRIVER							
Startup Period (Note 4)	t_{START}	R_{TIM} = 100kΩ		8	10.8	13.6	ms
		R_{TIM} = 4kΩ (minimum value)		0.35	0.45	0.55	
		TIM floating for MAX5906–MAX5909 fixed for MAX5904/MAX5905		5	9	14	
Average Gate Current	I_{GATE}	Charging, V_{GATE} = +5V, V_{IN} = +10V (Note 5)		80	100	130	µA
		Weak discharge, during startup when current limit is active or when 0.4V < V_{ON} < 0.8V			100		µA
		Strong discharge, triggered by a fault or when V_{ON} < 0.4V			3		mA
Gate Drive Voltage	V_{DRIVE}	$V_{GATE\_}$ - $V_{IN\_}$, $I_{GATE\_}$ < 1µA		4.8	5.4	5.8	V
ON COMPARATOR							
Fast Pulldown ON Threshold	$V_{ONFP,TH}$	Low to high		0.375	0.4	0.425	V
		Hysteresis			25		mV

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = +1V to +13.2V provided at least one supply is higher than +2.7V, V_{ON} = +2.7V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN1} = +5V, V_{IN2} = +3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Channel 1 ON Threshold	$V_{ON1,TH}$	Low to high		0.80	0.825	0.85	V
		Hysteresis			25		mV
Channel 2 ON Threshold	$V_{ON2,TH}$	Low to high		1.95	2.025	2.07	V
		Hysteresis			25		mV
ON Propagation Delay	t_{ON}	10mV overdrive			50		µs
ON Input Bias Current	I_{BON}	V_{IN1} = V_{IN2} = +13.2V	V_{ON} < 4.5V		0.03		µA
			V_{ON} > 4.5V		100		
			V_{ON} = 4V		0.03	1	
ON Pulse Width Low	$t_{UNLATCH}$	To unlatch after a latched fault		100			µs
DIGITAL OUTPUT (PGOOD)							
Output Leakage Current		V_{PGOOD} = 13.2V				1	µA
Output Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
PGOOD Delay	t_{PGDLY}	After t_{START}, MON_ = $V_{IN\_}$			0.75		ms
OUTPUT VOLTAGE MONITORS (MON1, MON2)							
MON_ Trip Threshold	$V_{MON\_}$	Overvoltage		657	687	707	mV
		Undervoltage		513	543	563	
MON_ Glitch Filter					20		µs
MON_ Input Bias Current		$V_{MON\_}$ = 600mV			0.03		µA
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	V_{UVLO}	Startup is initiated when this threshold is reached by V_{IN1} or V_{IN2}, V_{ON} > 0.8V, $V_{IN\_}$ increasing		2.1	2.4	2.67	V
		Hysteresis			100		mV
UVLO Glitch Filter Reset Time		$V_{IN\_}$ = 0, to unlatch after a fault		100			µs
UVLO to Startup Delay	$t_{D,UVLO}$	$V_{IN\_}$ step from 0 to 2.8V		20	37.5	60	ms
SHUTDOWN RESTART							
Auto-Retry Delay	t_{RETRY}	Delay time to restart after a fault shutdown MAX5904/MAX5906/MAX5908			64 x t_{START}		ms
UNCOMMITTED COMPARATOR							
INC+ Trip Threshold Voltage	$V_{C,TH}$	Low to high		1.206	1.236	1.266	V
		Hysteresis			10		mV
Propagation Delay		10mV overdrive			50		µs
OUTC Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
INC+ Bias Current		V_{INC+} = 5V			0.02	1	µA
OUTC Leakage Current	I_{OUTC}	V_{OUTC} = 13.2V			0.02	1	µA

Note 1: Limits are 100% tested at T_A = +25°C and +85°C. Limits at -40° are guaranteed by characterization but are not production tested.

Note 2 The MAX5906–MAX5909 slow-comparator threshold is adjustable. $V_{SC,TH}$ = R_{LIM} x 0.25µA + 25mV (see *Typical Operating Characteristics*).

Note 3: The current-limit slow-comparator response time is weighted against the amount of overcurrent; the higher the overcurrent condition, the faster the response time. See *Typical Operating Characteristics*.

Note 4: The startup period (t_{START}) is the time during which the slow comparator is ignored and the device acts as a current limiter by regulating the sense current with the fast comparator. See the *Startup Period* section.

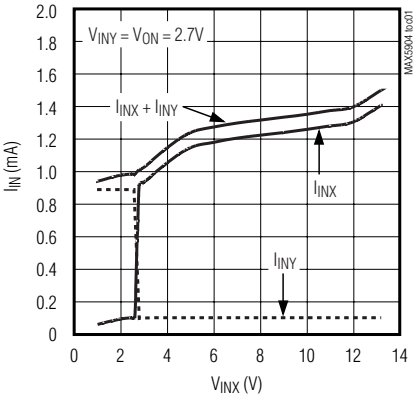
Note 5: The current available at GATE is a function of V_{GATE} (see *Typical Operating Characteristics*).

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

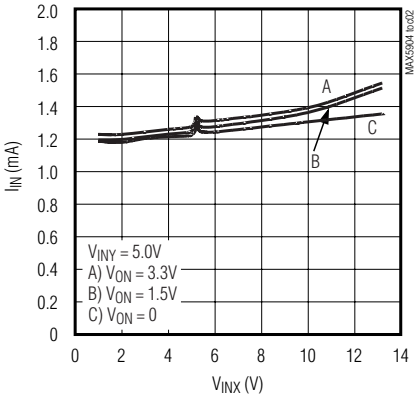
Typical Operating Characteristics

(Typical Operating Circuits, Q1 = Q2 = Fairchild FDB7090L, V_{IN1} = +5V, V_{IN2} = +3.3V, T_A = +25°C, unless otherwise noted. Channels 1 and 2 are identical in performance. Where characteristics are interchangeable, channels 1 and 2 are referred to as X and Y.)

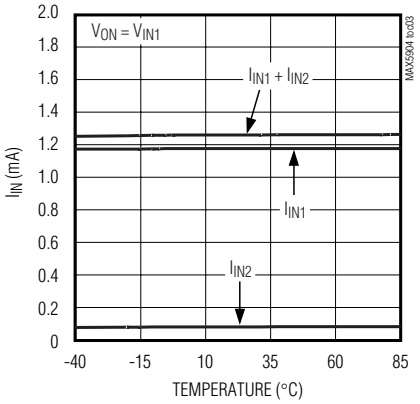
SUPPLY CURRENT vs. SUPPLY VOLTAGE



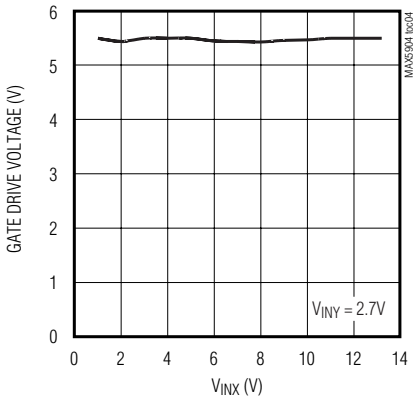
TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



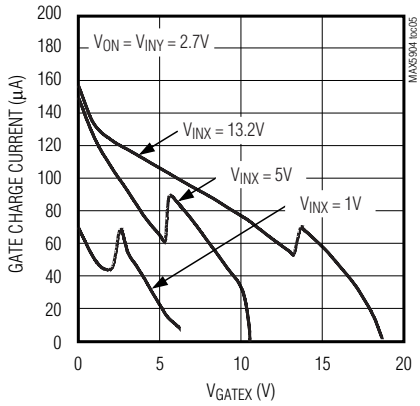
SUPPLY CURRENT vs. TEMPERATURE



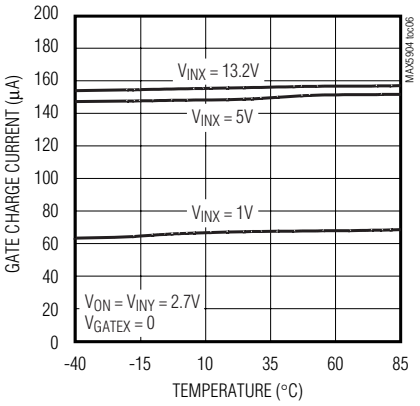
GATE DRIVE VOLTAGE vs. INPUT VOLTAGE



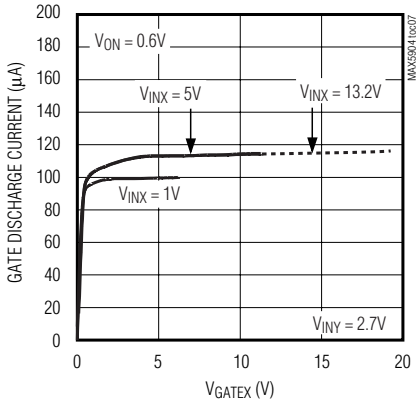
GATE CHARGE CURRENT vs. GATE VOLTAGE



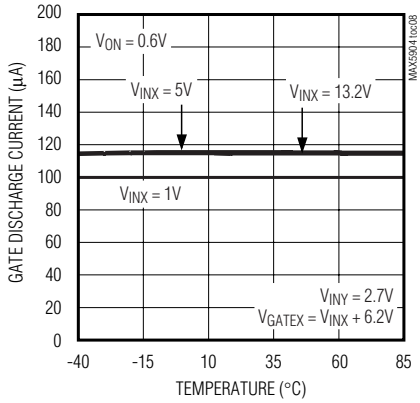
GATE CHARGE CURRENT vs. TEMPERATURE



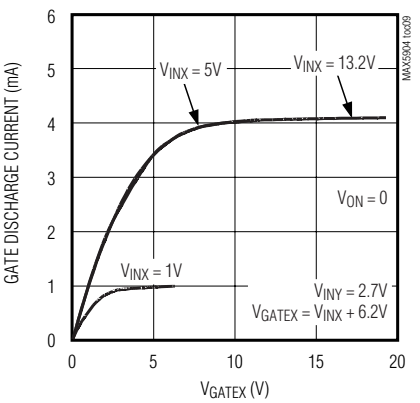
GATE WEAK DISCHARGE CURRENT vs. GATE VOLTAGE



GATE WEAK DISCHARGE CURRENT vs. TEMPERATURE



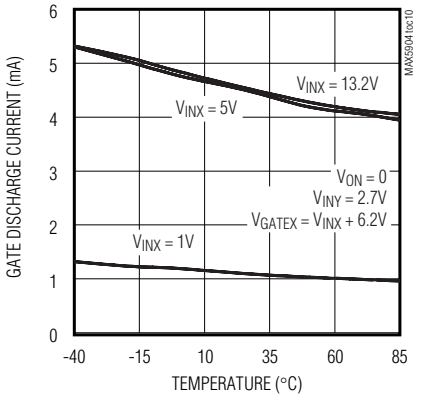
GATE STRONG DISCHARGE CURRENT vs. GATE VOLTAGE



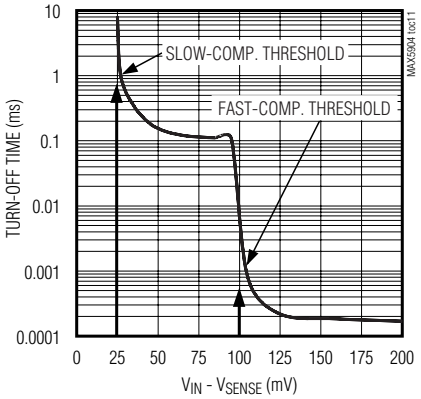
Typical Operating Characteristics (continued)

(Typical Operating Circuits, Q1 = Q2 = Fairchild FDB7090L, V_{IN1} = +5V, V_{IN2} = +3.3V, T_A = +25°C, unless otherwise noted. Channels 1 and 2 are identical in performance. Where characteristics are interchangeable, channels 1 and 2 are referred to as X and Y.)

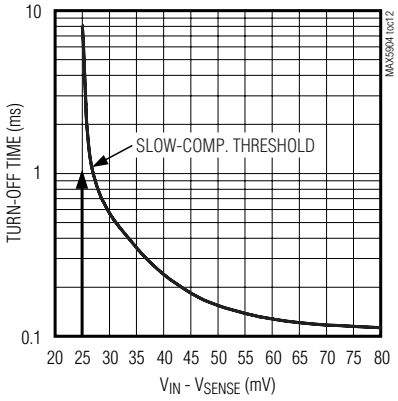
GATE STRONG DISCHARGE CURRENT vs. TEMPERATURE



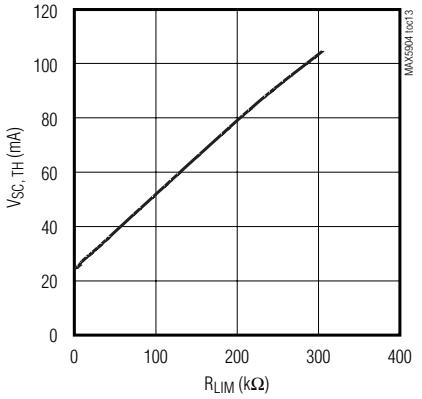
TURN-OFF TIME vs. SENSE VOLTAGE



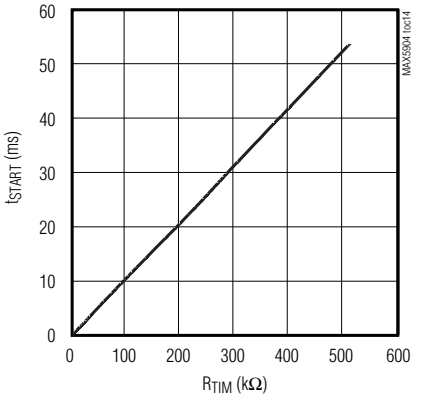
TURN-OFF TIME vs. SENSE VOLTAGE (EXPANDED SCALE)



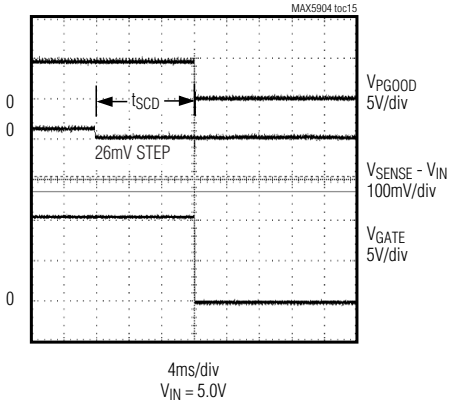
SLOW-COMPARATOR THRESHOLD vs. R_{LIM}



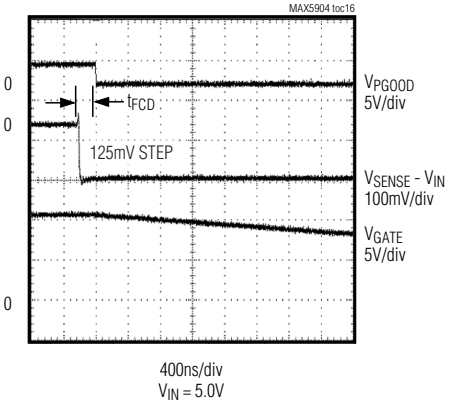
STARTUP PERIOD vs. R_{TIM}



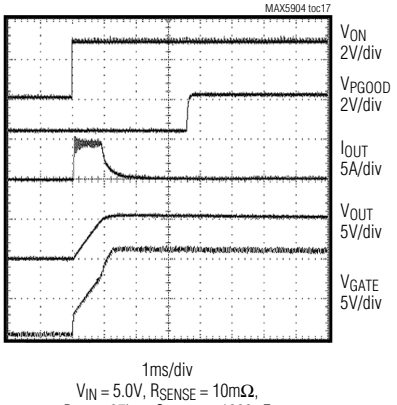
TURN-OFF TIME FAST-COMPARATOR FAULT



TURN-OFF TIME FAST-COMPARATOR FAULT



STARTUP WAVEFORMS FAST TURN-ON

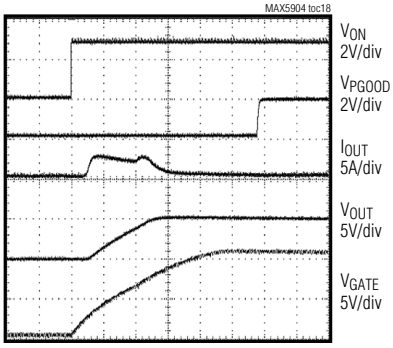


Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

Typical Operating Characteristics (continued)

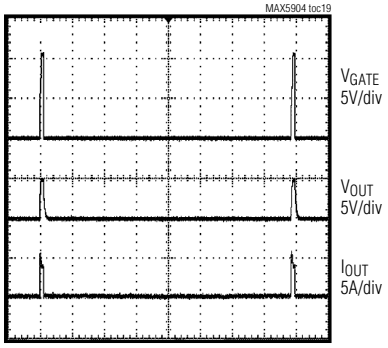
(Typical Operating Circuits, Q1 = Q2 = Fairchild FDB7090L, V_{IN1} = +5V, V_{IN2} = +3.3V, T_A = +25°C, unless otherwise noted. Channels 1 and 2 are identical in performance. Where characteristics are interchangeable, channels 1 and 2 are referred to as X and Y.)

STARTUP WAVEFORMS SLOW TURN-ON



1ms/div
V_{IN} = 5.0V, R_{SENSE} = 10mΩ, R_{TIM} = 47kΩ, C_{BOARD} = 1000µF, C_{GATE} = 22nF

AUTO-RETRY DELAY



40ms/div
V_{IN} = 5.0V, R_{SENSE} = 10mΩ, R_{TIM} = 47kΩ, C_{BOARD} = 1000µF, R_{BOARD} = 1.4Ω

Pin Description

PIN		NAME	FUNCTION
MAX5904/ MAX5905	MAX5906–MAX5909		
—	1	PGOOD	Open-Drain Status Output. High impedance when startup is complete and no faults are detected. Actively held low during startup and when a fault is detected.
—	2	TIM	Startup Timer Setting. Connect a resistor from TIM to GND to set the startup period. Leave TIM unconnected for the default startup period of 9ms.
1	3	IN1	Channel 1 Supply Input. Connect to a supply voltage from 1V to 13.2V.
2	4	SENSE1	Channel 1 Current-Sense Input. Connect R_{SENSE1} from IN1 to SENSE1.
3	5	GATE1	Channel 1 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
4	6	GND	Ground
—	7	LIM1	Channel 1 Current-Limit Setting. Connect a resistor from LIM1 to GND to set current-trip level. Connect to GND for the default 25mV threshold.
—	8	MON1	Channel 1 Output Voltage Monitor. Window comparator input. Connect through a resistive-divider from OUT1 to GND to set the channel 1 overvoltage and undervoltage thresholds. Connect to IN1 to disable.
—	9	MON2	Channel 2 Output Voltage Monitor. Window comparator input. Connect through a resistive-divider from OUT2 to ground to set the channel 2 overvoltage and undervoltage thresholds. Connect to IN2 to disable.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5904/ MAX5905	MAX5906– MAX5909		
—	10	LIM2	Channel 2 Current-Limit Setting. Connect a resistor from LIM2 to GND to set current-trip level. Connect to GND for the default 25mV threshold.
5	11	ON	On Comparator Input
6	12	GATE2	Channel 2 Gate-Drive Output. Connect to gate of external N-channel MOSFET.
7	13	SENSE2	Channel 2 Current-Sense Input. Connect R_{SENSE2} from IN2 to SENSE2.
8	14	IN2	Channel 2 Supply Input. Connect to a supply voltage from 1V to 13.2V.
—	15	INC+	Uncommitted Comparator Noninverting Input
—	16	OUTC	Uncommitted Comparator Open-Drain Output. Actively held low when V_{INC+} is less than 1.236V.

Detailed Description

The MAX5904–MAX5909 are circuit breaker ICs for hot-swap applications where a line card is inserted into a live backplane. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide low impedance that can momentarily cause the main power supply to collapse. The MAX5904–MAX5909 reside either on the backplane or on the removable card to provide inrush current limiting and short-circuit protection. This is achieved by using external N-channel MOSFETs, external current-sense resistors, and two on-chip comparators. Figure 1 shows the MAX5906–MAX5909 functional diagram.

The MAX5904/MAX5905 have a fixed startup period and current-limit threshold. The startup period and current-limit threshold of the MAX5906–MAX5909 can be adjusted with external resistors.

Startup Period

R_{TIM} sets the duration of the startup period for the MAX5906–MAX5909 from 0.4ms to 50ms (see the *Setting the Startup Period* section). The duration of the startup period is fixed at 9ms for the MAX5904/MAX5905. The startup period begins after the following three conditions are met:

1) V_{IN1} or V_{IN2} exceeds the UVLO threshold (2.4V) for the UVLO to startup delay (37.5ms).
2) V_{ON} exceeds the channel 1 ON threshold (0.825V).
3) The device is not latched or in its auto-retry delay. (See *Latched and Auto-Retry Fault* Management.)

The MAX5904–MAX5909 limit the load current if an overcurrent fault occurs during startup. The slow comparator is disabled during the startup period and the load current can be limited in two ways:

1) Slowly enhancing the MOSFETs by limiting the MOSFET gate charging current
2) Limiting the voltage across the external current-sense resistor.

During the startup period the gate drive current is typically 100µA and decreases with the increase of the gate voltage (see *Typical Operating Characteristics*). This allows the controller to slowly enhance the MOSFETs. If the fast comparator detects an overcurrent, the MAX5904–MAX5909 regulate the gate voltage to ensure that the voltage across the sense resistor does not exceed $V_{SU,TH}$. This effectively regulates the inrush current during startup. Figure 2 shows the startup waveforms. PGOOD goes high impedance 0.75ms after the startup period if no fault condition is present.

VariableSpeed/BiLevel Fault Protection

VariableSpeed/BiLevel fault protection incorporates two comparators with different thresholds and response times to monitor the load current (Figure 3). During the startup period, protection is provided by limiting the load current. Protection is provided in normal operation (after the startup period has expired) by discharging both MOSFET gates with a strong 3mA pulldown current in response to a fault condition. After a fault, PGOOD is pulled low, the MAX5905/MAX5907/

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

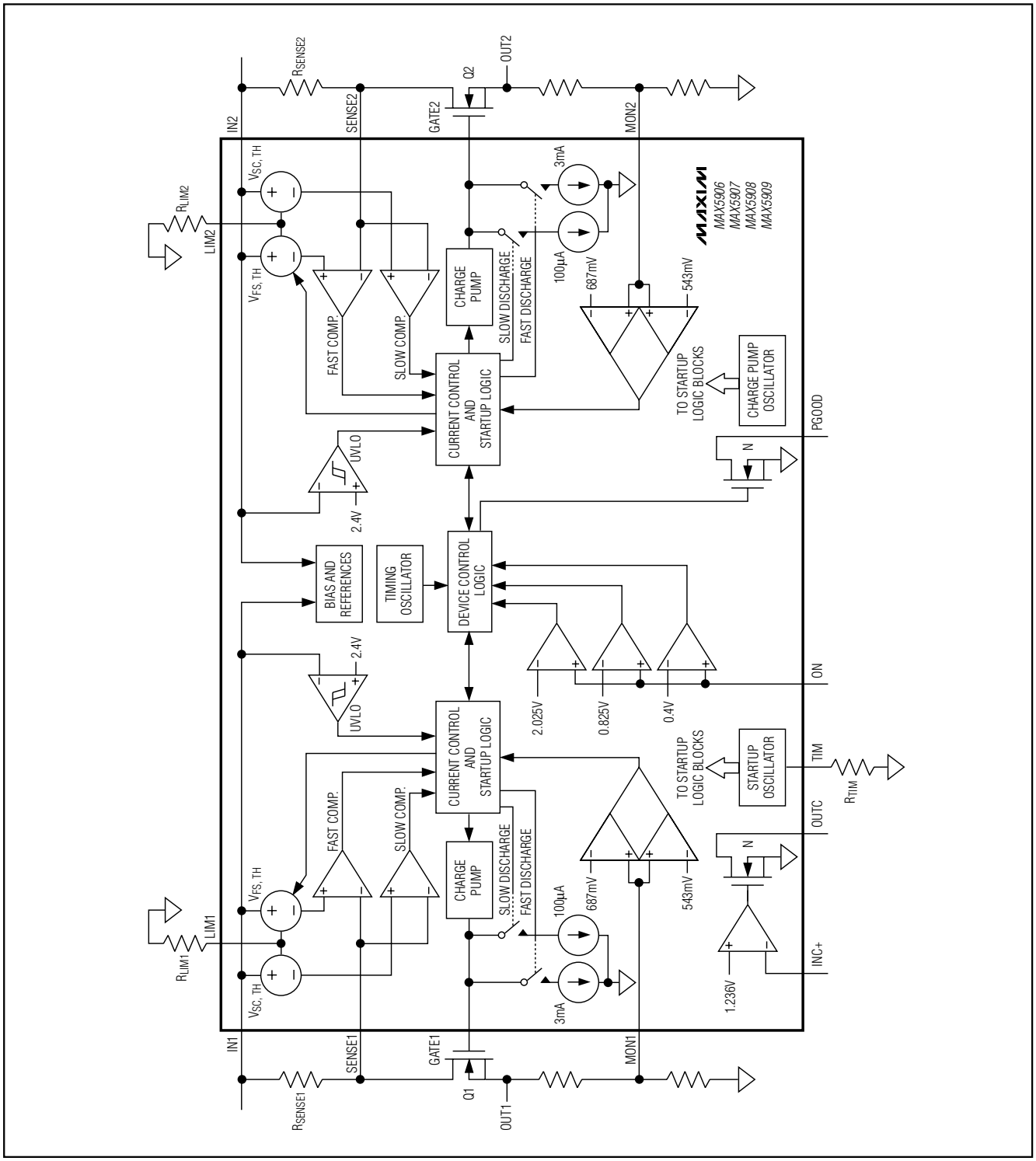


Figure 1. MAX5906–MAX5909 Functional Diagram

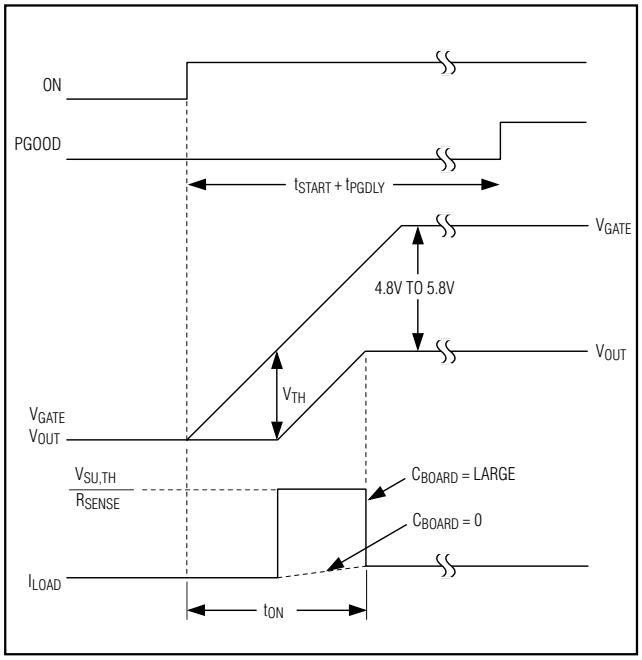


Figure 2. Startup Waveforms

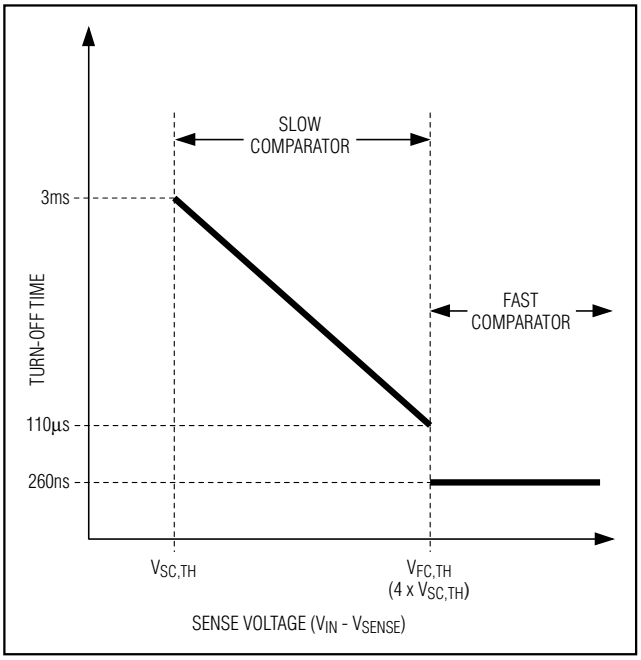


Figure 3. VariableSpeed/BiLevel Response

MAX5909 stay latched off and the MAX5904/MAX5906/MAX5908 automatically restart.

Slow Comparator Startup Period

The slow comparator is disabled during the startup period while the external MOSFETs are turning on. Disabling the slow comparator allows the device to ignore the higher-than-normal inrush current charging the board capacitors when a card is first plugged into a live backplane.

Slow Comparator Normal Operation

After the startup period is complete the slow comparator is enabled and the device enters normal operation. The comparator threshold voltage ($V_{SC,TH}$) is fixed at 25mV for the MAX5904/MAX5905 and is adjustable from 25mV to 100mV for the MAX5906–MAX5909. The slow comparator response time decreases to a minimum of 110µs with a large overdrive voltage (Figure 3). Response time is 3ms for a 1mV overdrive. The variable speed response time allows the MAX5904–MAX5909 to ignore low-amplitude momentary glitches, thus increasing system noise immunity. After an extended overcurrent condition, a fault is generated, PGOOD is pulled low, and the MOSFET gates are discharged with a strong 3mA pulldown current.

Fast Comparator Startup Period

During the startup period the fast comparator regulates the gate voltage to ensure that the voltage across the sense resistor does not exceed $V_{SU,TH}$. The startup fast-comparator threshold voltage ($V_{SU,TH}$) is scaled to two times the slow-comparator threshold ($V_{SC,TH}$).

Fast Comparator Normal Operation

In normal operation, if the load current reaches the fast-comparator threshold, a fault is generated, PGOOD is pulled low, and the MOSFET gates are discharged with a strong 3mA pulldown current. This happens in the event of a serious current overload or a dead short. The fast-comparator threshold voltage ($V_{FC,TH}$) is scaled to four times the slow-comparator threshold ($V_{SC,TH}$). This comparator has a fast response time of 260ns (Figure 3).

Undervoltage Lockout (UVLO)

The undervoltage lockout prevents the MAX5904–MAX5909 from turning on the external MOSFETs until one input voltage exceeds the UVLO threshold (2.4V) for $t_{D,UVLO}$. The MAX5904–MAX5909 use power from the higher input voltage rail for the charge pumps. This allows for more efficient charge-pump operation. The UVLO protects the external MOSFETs from an insufficient gate drive voltage. $t_{D,UVLO}$ ensures that the board is fully inserted into the backplane and that the input

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

voltages are stable. Any input voltage transient on **both** supplies below the UVLO threshold will reinitiate the $t_{D,UVLO}$ and the startup period.

Latched and Auto-Retry Fault Management

The MAX5905/MAX5907/MAX5909 latch the external MOSFETs off when a fault is detected. Toggling ON below 0.4V or one of the supply voltages below the UVLO threshold for at least 100µs clears the fault latch and reinitiates the startup period. Similarly, the MAX5904/MAX5906/MAX5908 turn the external MOSFETs off when a fault is detected then automatically restart after the auto-retry delay that is internally set to 64 times t_{START}. During the auto-retry delay, toggling ON below 0.4V does not clear the fault. The auto-retry can be overridden causing the startup period to begin immediately by toggling one of the supply voltages below the UVLO threshold.

Output Voltage Monitor

The MAX5905–MAX5909 monitor the output voltages with the MON1 and MON2 window comparator inputs. These voltage monitors are enabled after the startup period. Once enabled, the voltage monitor detects a fault if $V_{MON\_}$ is less than 543mV or greater than 687mV. If an output voltage fault is detected PGOOD pulls low. When the MAX5906/MAX5907 detect an output voltage fault on either MON1 or MON2, the fault is latched and both external MOSFET gates are discharged at 3mA. When the MAX5908/MAX5909 detect an output voltage fault the external MOSFET gates are not affected. The MAX5908/MAX5909 PGOOD goes high impedance when the output voltage fault is removed. The voltage monitors do not react to output glitches of less than 20µs. A capacitor from MON_ to GND increases the effective glitch filter time. Connect MON1 to IN1 and MON2 to IN2 to disable the output voltage monitors.

Status Output (PGOOD)

The status output is an open-drain output that pulls low in response to one of the following conditions:

- Forced off (ON < 0.8V)
- Overcurrent fault
- Output voltage fault

PGOOD goes high impedance 0.75ms after the device enters normal operation and no faults are present (Table 1).

Applications Information

Component Selection

N-Channel MOSFET

Select the external MOSFETs according to the application's current levels. Table 2 lists some recommended components. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ causes output ripple if there is a pulsating load. Determine the device power rating to accommodate a short-circuit condition on the board at startup and when the device is in automatic-retry mode (see *MOSFET Thermal Considerations*).

Using the MAX5905/MAX5907/MAX5909 in latched mode allows the use of MOSFETs with lower power ratings. A MOSFET typically withstands single-shot pulses with higher dissipation than the specified package rating. Table 3 lists some recommended manufacturers and components.

Sense Resistor

The slow-comparator threshold voltage is set at 25mV for the MAX5904/MAX5905 and is adjustable from 25mV to 100mV for the MAX5906–MAX5909. Select a sense resistor that causes a drop equal to the slow-comparator threshold voltage at a current level above

Table 1. Status Output Truth Table

DEVICE IN UVLO DELAY PERIOD	DEVICE IN STARTUP PERIOD	ON	OVERCURRENT FAULT	OVER/UNDER-VOLTAGE FAULT	PART IN RETRY-TIMEOUT PERIOD OR LATCHED OFF	PGOOD
Yes	X	X	X	X	X	Low
X	Yes	X	X	X	X	Low
X	X	Low	X	X	X	Low
X	X	X	Yes	X	X	Low
X	X	X	X	Yes	X	Low
X	X	X	X	X	Yes	Low
No	No	High	No	No	No	High-Z

X = don't care

Table 2. Recommended N-Channel MOSFETs

PART NUMBER	MANUFACTURER	DESCRIPTION
IRF7413	International Rectifier	11mΩ, 8 SO, 30V
IRF7401		22mΩ, 8 SO, 20V
IRL3502S		6mΩ, D2PAK, 20V
MMSF3300	Motorola	20mΩ, 8 SO, 30V
MMSF5N02H		30mΩ, 8 SO, 20V
MTB60N05H		14mΩ, D2PAK, 50V
FDS6670A	Fairchild	10mΩ, 8SO, 30V
NDS8426A		13.5mΩ, 8 SO, 20V
FDB8030L		4.5mΩ, D2PAK, 30V

the maximum normal operating current. Typically, set the overload current at 1.2 to 1.5 times the nominal load current. The fast-comparator threshold is four times the slow-comparator threshold in normal operating mode. Choose the sense resistor power rating to be greater than $(I_{OVERLOAD})^2 \times V_{SC,TH}$.

Slow-Comparator Threshold, R_{LIM}

The slow-comparator threshold voltage of the MAX5904/MAX5905 is fixed at 25mV and adjustable from 25mV to 100mV for the MAX5906–MAX5909.

The adjustable slow-comparator threshold of the MAX5906–MAX5909 allows designers to fine-tune the current-limit threshold for use with standard value sense resistors. Low slow-comparator thresholds allow for increased efficiency by reducing the power dissipated by the sense resistor. Furthermore, the low 25mV slow-comparator threshold is beneficial when operating with supply rails down to 1V because it allows a small percentage of the overall output voltage to be used for current sensing. The VariableSpeed/BiLevel fault protection feature offers inherent system immunity against load transients and noise. This allows the slow-comparator threshold to be set close to the maximum normal operating level without experiencing nuisance faults. Typically, set the overload current at 1.2 to 1.5 times the nominal load current. To adjust the slow-comparator threshold calculate R_{LIM} as follows:

$$R_{LIM} = \frac{V_{TH} - 25mV}{0.25\mu A}$$

where V_{TH} is the desired slow-comparator threshold voltage.

Setting the Startup Period, R_{TIM}

The startup period (t_{START}) of the MAX5904/MAX5905 is fixed at 9ms, and adjustable from 0.4ms to 50ms for the MAX5906–MAX5909. The adjustable startup period of the MAX5906–MAX5909 systems can be customized for MOSFET gate capacitance and board capacitance (C_{BOARD}). The startup period is adjusted with the resistance connected from TIM to GND (R_{TIM}). R_{TIM} must be between 4kΩ and 500kΩ. The MAX5906–MAX5909 startup period has a default value of 9ms when TIM is left floating. Calculate R_{TIM} with the following equation:

$$R_{TIM} = \frac{t_{START}}{128 \times 800pF}$$

where t_{START} is the desired startup period.

There are two ways of completing the startup sequence. **Case A** describes a startup sequence that slowly turns on the MOSFETs by limiting the gate charge. **Case B** uses the current-limiting feature and turns on the MOSFETs as fast as possible while still preventing a high inrush current. The output voltage ramp-up time (t_{ON}) is determined by the longer of the two timings, case A and case B. Set the MAX5906–MAX5909 startup timer t_{START} to be longer than t_{ON} to guarantee enough time for the output voltage to settle.

Case A: Slow Turn-ON (without current limit)

There are two ways to turn on the MOSFETs without reaching the fast-comparator current limit:

If the board capacitance (C_{BOARD}) is small, the inrush current is low.

Table 3. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistors	Dale-Vishay	402-564-3131	www.vishay.com
	IRC	704-264-8861	www.irctt.com
MOSFETs	International Rectifier	310-233-3331	www.irf.com
	Fairchild	888-522-5372	www.fairchildsemi.com
	Motorola	602-244-3576	www.mot-sps.com/ppd

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

If the gate capacitance is high, the MOSFETs turn on slowly.

In both cases, the turn-on time is determined only by the charge required to enhance the MOSFET. The small gate-charging current of 100µA effectively limits the output voltage dV/dt. Connecting an external capacitor between GATE and GND extends turn-on time. The time required to charge/discharge a MOSFET is as follows:

$$t = \frac{C_{GATE} \times \Delta V_{GATE} + Q_{GATE}}{I_{GATE}}$$

where:

C_{GATE} is the external gate to ground capacitance (Figure 4)

ΔV_{GATE} is the change in gate voltage

Q_{GATE} is the MOSFET total gate charge

I_{GATE} is the gate charging/discharging current

In this case, the inrush current depends on the MOSFET gate-to-drain capacitance (C_{rss}) plus any additional capacitance from gate to GND (C_{GATE}), and on any load current (I_{LOAD}) present during the startup period.

$$I_{INRUSH} = \frac{C_{BOARD}}{C_{rss} + C_{GATE}} \times I_{GATE} + I_{LOAD}$$

Example: Charging and Discharging times using the Fairchild FDB7030L MOSFET

If V_{IN1} = 5V then GATE1 charges up to 10.4V (V_{IN1} + V_{DRIVE}), therefore ΔV_{GATE} = 10.4V. The manufacturer's data sheet specifies that the FDB7030L has approximately 60nC of gate charge and C_{rss} = 600pF. The MAX5904–MAX5909 have a 100µA gate-charging current and a 100µA weak discharging current or 3mA strong discharging current.

C_{BOARD} = 6µF and the load does not draw any current during the startup period.

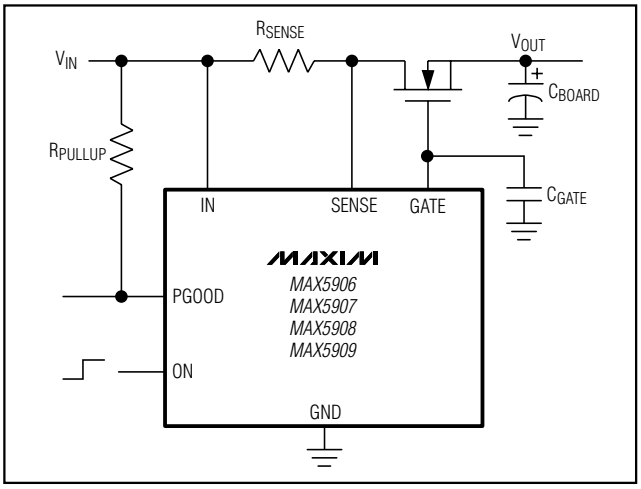


Figure 4. Operating with an External Gate Capacitor

With no gate capacitor the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 0} \times 100\mu A + 0 = 1A$$

$$t_{CHARGE} = \frac{0 \times 10.4V + 60nC}{100\mu A} = 0.6ms$$

$$t_{DISCHARGE\_SLOW} = \frac{0 \times 10.4V + 60nC}{100\mu A} = 0.6ms$$

$$t_{DISCHARGE\_FAST} = \frac{0 \times 10.4V + 60nC}{3mA} = 0.02ms$$

With a 22nF gate capacitor the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 22nF} \times 100\mu A + 0 = 26.5mA$$

$$t_{CHARGE} = \frac{22nF \times 10.4V + 60nC}{100\mu A} = 2.89ms$$

$$t_{DISCHARGE\_SLOW} = \frac{22nF \times 10.4V + 60nC}{100\mu A} = 2.89ms$$

$$t_{DISCHARGE\_FAST} = \frac{22nF \times 10.4V + 60nC}{3mA} = 0.096ms$$

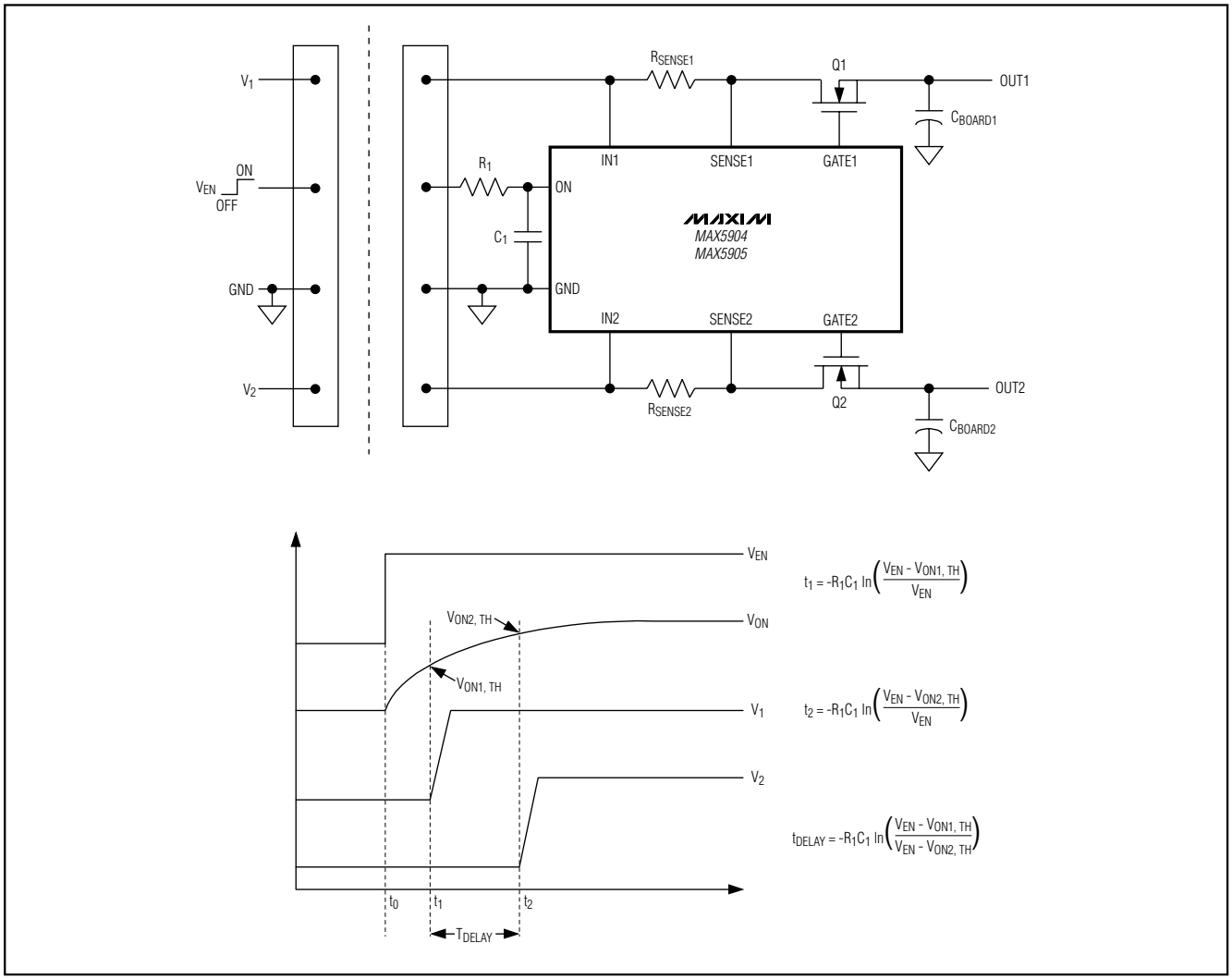


Figure 5. Power Sequencing: Channel 2 Turns On t_{DELAY} After Channel 1

Case B: Fast Turn-On (with current limit)

In applications where the board capacitance (C_{BOARD}) is high, the inrush current causes a voltage drop across R_{SENSE} that exceeds the startup fast-comparator threshold. The fast comparator regulates the voltage across the sense resistor to $V_{SU,TH}$. This effectively regulates the inrush current during startup. In this case, the current charging C_{BOARD} can be considered constant and the turn-on time is:

$$t_{ON} = \frac{C_{BOARD} \times V_{IN} \times R_{SENSE}}{V_{SU,TH}}$$

The maximum inrush current in this case is:

$$I_{INRUSH} = \frac{V_{SU,TH}}{R_{SENSE}}$$

Figure 2 shows the waveforms and timing diagrams for a startup transient with current regulation. (See *Typical Operating Characteristics*.) When operating under this condition, an external gate capacitor is not required.

ON Comparator

The ON comparator controls the on/off function of the MAX5904–MAX5909. ON is the input to a precision

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

three-level voltage comparator that allows individual control over channel 1 and channel 2. Drive ON high (> 2.025V) to enable channel 1 and channel 2. Pull ON low (<0.4V) to disable both channels. To enable channel 1 only, V_{ON} must be between the channel 1 ON threshold (0.825V) and the channel 2 ON threshold (2.025V). The device can be turned off slowly, reducing inductive kickback, by forcing ON between 0.4V and 0.825V until the gates are discharged. The ON comparator is ideal for power sequencing (Figure 5).

Uncommitted Comparator

The MAX5906–MAX5909 feature an uncommitted comparator that increases system flexibility. This comparator can be used for voltage monitoring, or for generating a power-on reset signal for on-card microprocessors (Figure 6).

The uncommitted comparator output (OUTC) is open drain and is pulled low when the comparator input voltage (V_{INC+}) is below its threshold voltage (1.236V). OUTC is high impedance when V_{INC+} is greater than 1.236V.

Using the MAX5904–MAX5909 on the Backplane

Using the MAX5904–MAX5909 on the backplane allows multiple cards with different input capacitance to be inserted into the same slot even if the card does not have on-board hot-swap protection. The startup period can be triggered if IN is connected to ON through a trace on the card (Figure 7).

Input Transients

The voltage at IN1 or IN2 must be above the UVLO during inrush and fault conditions. When a short-circuit condition occurs on the board, the fast comparator trips causing the external MOSFET gates to be discharged at 3mA. The main system power supply must be able to sustain a temporary fault current, without dropping below the UVLO threshold of 2.4V, until the external MOSFET is completely off. If the main system power supply collapses below UVLO, the MAX5904–MAX5909 will force the device to restart once the supply has recovered. The MOSFET is turned off in a very short time resulting in a high di/dt. The backplane delivering the power to the external card must have low inductance to minimize voltage transients caused by this high di/dt.

MOSFET Thermal Considerations

During normal operation, the external MOSFETs dissipate little power. The MOSFET $R_{DS(ON)}$ is low when the MOSFET is fully enhanced. The power dissipated in normal operation is $P_D = I_{LOAD}^2 \times R_{DS(ON)}$. The most power dissipation occurs during the turn-on and turn-off transients when the MOSFETs are in their linear regions. Take into consideration the worst-case scenario of a continuous short-circuit fault, consider these two cases:

1) The single turn-on with the device latched after a fault (MAX5905/MAX5907/MAX5909)
2) The continuous automatic retry after a fault (MAX5904/MAX5906/MAX5908)

MOSFET manufacturers typically include the package thermal resistance from junction to ambient ($R_{\theta JA}$) and thermal resistance from junction to case ($R_{\theta JC}$) which determine the startup time and the retry duty cycle ($d = t_{START} / t_{RETRY}$). Calculate the required transient thermal resistance with the following equation:

$$Z_{\theta JA(MAX)} \le \frac{T_{JMAX} - T_A}{V_{IN} \times I_{START}}$$

where $I_{START} = V_{SU,TH} / R_{SENSE}$

Layout Considerations

To take full tracking advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. Place the MAX5904–MAX5909 close to the card's connector. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections (Figure 8).

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board. See MAX5908 EV Kit.

Chip Information

TRANSISTOR COUNT: 3230

PROCESS: BiCMOS

Selector Guide

PART	OUTPUT UNDERVOLTAGE/OVERVOLTAGE PROTECTION/MONITOR	FAULT MANAGEMENT
MAX5904ESA	—	Auto-Retry
MAX5905ESA	—	Latched
MAX5906EEE	Protection	Auto-Retry
MAX5907EEE	Protection	Latched
MAX5908EEE	Monitor	Auto-Retry
MAX5909EEE	Monitor	Latched

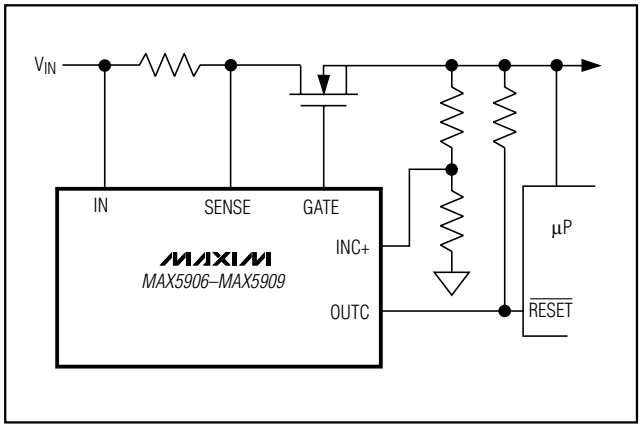


Figure 6. Power-On Reset

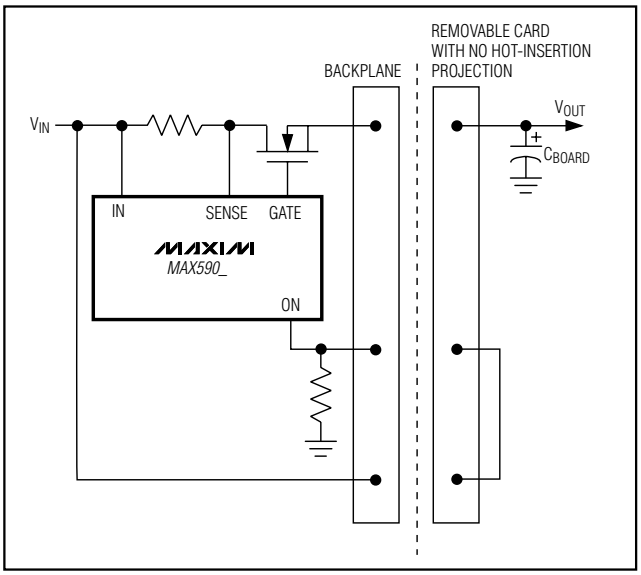


Figure 7. Using the MAX5904–MAX5909 on a Backplane

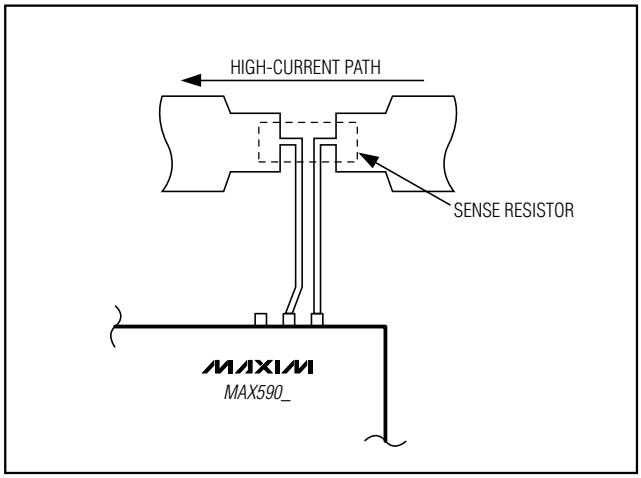
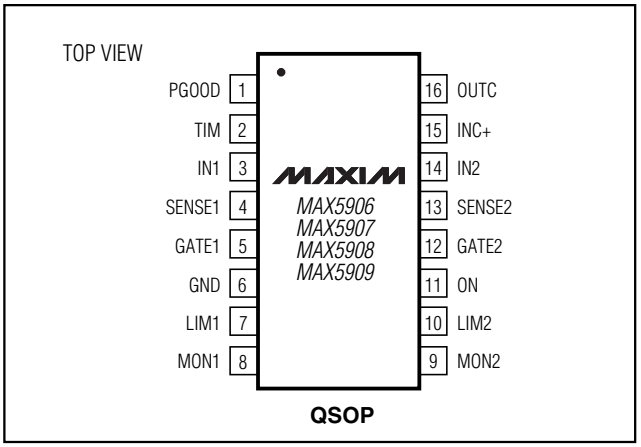


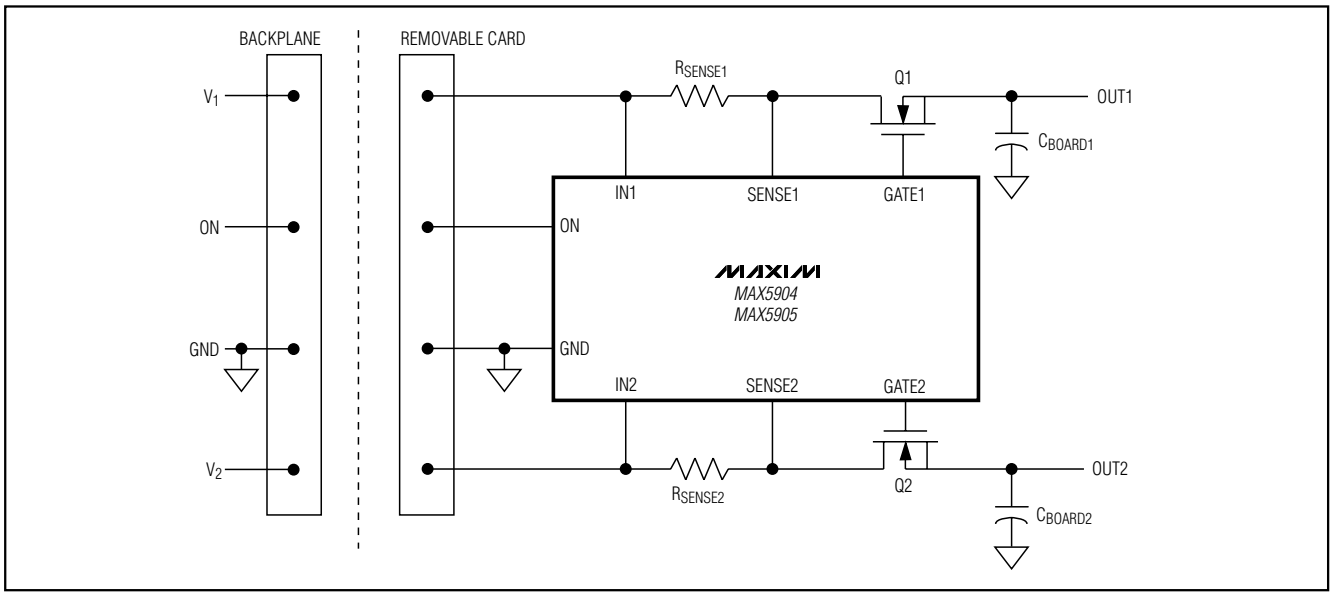
Figure 8. Kelvin Connection for the Current-Sense Resistors

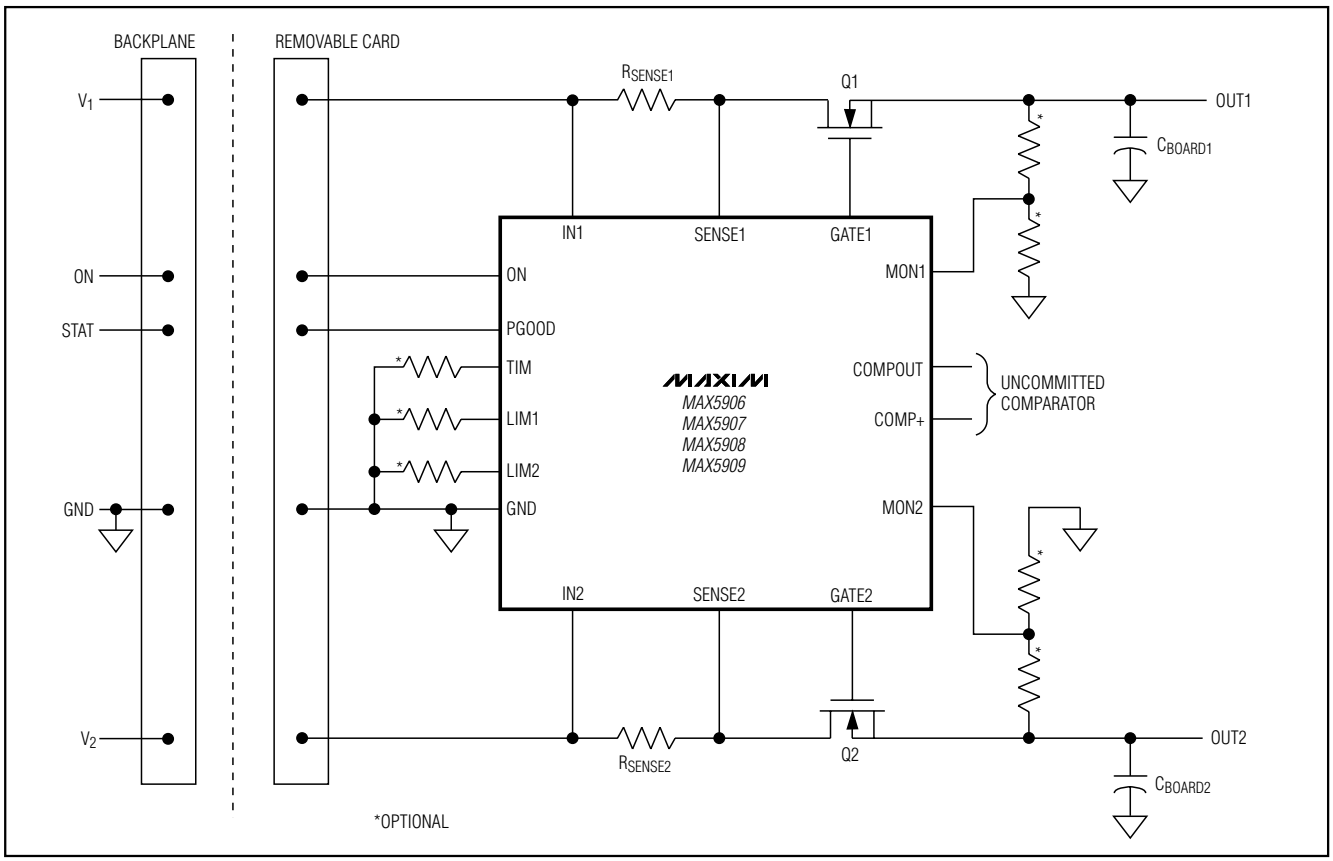
Pin Configurations (continued)



Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

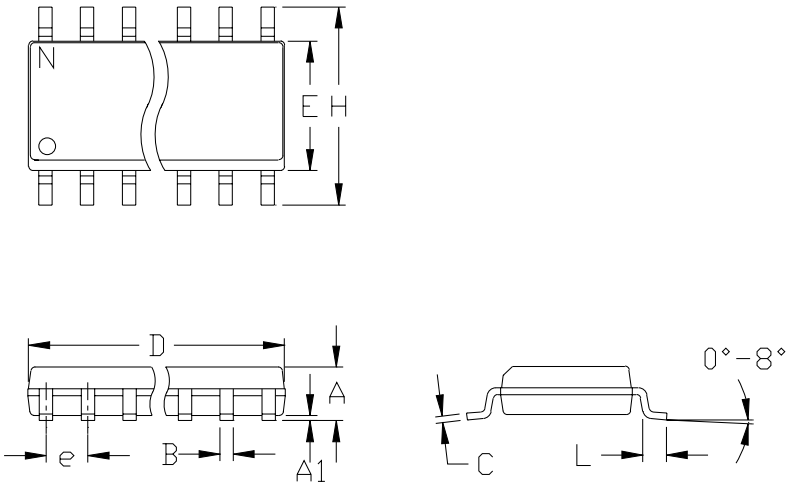
Typical Operating Circuits





Package Information

SOICN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

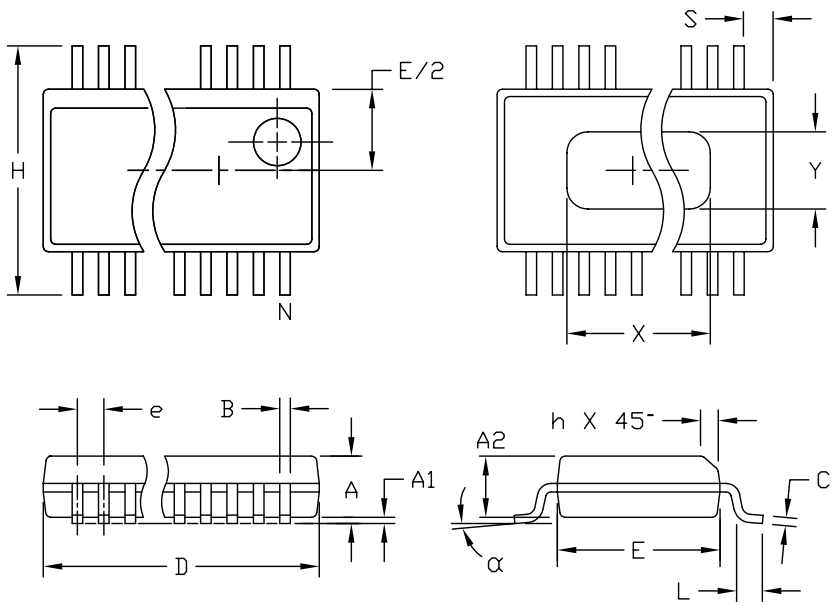
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM	PACKAGE FAMILY OUTLINE: SOIC .150"	1/1	21-0041 A
120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION	TITLE		DOCUMENT CONTROL NUMBER REV

Low-Voltage, Dual Hot-Swap Controllers/Power Sequencers

Package Information (continued)



QSOP.EPS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1