❑ MN102L490A

Type		MN102L490A
ROM (×8-bit / ×16-bit)		External
RAM (×8-bit / ×16-bit)		3 K
Package		LQFP100-P-1414 *Lead-free
Minimum Instruction Execution Time	With Main Clock operated	100 ns (at 4.5 V to 5.5 V, 20 MHz)
Interrupts		• RESET • Watchdog • Timer counter 0 to 5 • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A • Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 4 • Serial ch.0, 1 transmission • Serial ch.0, 1 reception • NMI pin • A/D conversion finish
Timer Counter		Timer counter 0 : 8-bit × 1 (timer output, event count) Clock source ····· 1/1, 1/128 of system clock frequency; 1/4 of low speed clock frequency; external clock Interrupt source ····· underflow of timer counter 0 Timer counter 1 : 8-bit × 1 (timer output, event count, A/D conversion start up) Clock source ····· system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 output Interrupt source ····· underflow of timer counter 1 Timer counter 2 to 3 : 8-bit × 1 (timer output, event count, UART baud rate generator) Clock source ····· system clock; external clock; timer counter 0 output; timer counter 1, 2 output Interrupt source ····· underflow of timer counter 2, 3 Timer counter 4, 5 : 8-bit × 1 (timer output, event count) Clock source ····· 1/4 of low speed clock frequency; external clock; timer counter 0 output; timer counter 3, 4 output Interrupt source ····· underflow of timer counter 4, 5 Timer counter 6, 7 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source ····· system clock; external clock; timer counter 4, 5 output Interrupt source ····· coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7 (Connectable) timer counter 0 to 5
Serial Interface		Serial 0 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source ····· 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 2 frequency Serial 1 : 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source ····· 1/16 of timer counter 2 frequency; 1/16 of timer counter 3 frequency; external clock; 1/2 of timer counter 3 frequency UART × 2 (common use with serial 0, 1) I^2C × 2 (single master)
I/O Pins	**I/O**	48 • Common use : 8 (by 4 bits), 40 (by bit)
A/D Inputs		8-bit × 8-ch. (with S/H)
PWM		16-bit × 2-ch.
Notes		Burst ROM inferface support; ATC (between serial 0ch and internal RAM) support; Main pin inputs : TTL level

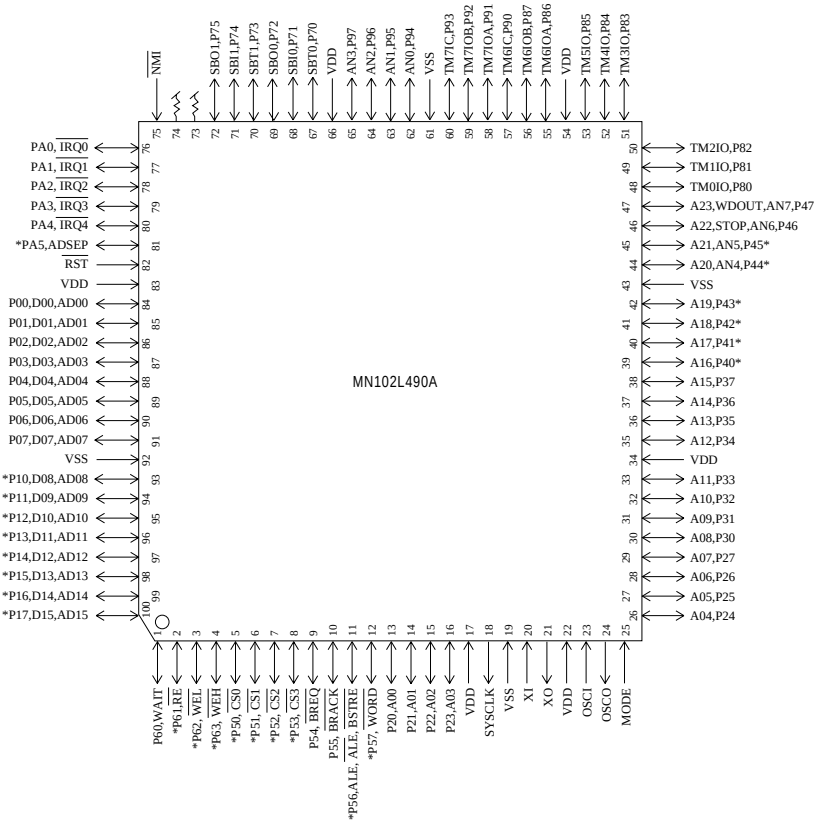
Electric Characteriatics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 20 MHz , VDD = 5.0 V			75	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 20 MHz , VDD = 5.0 V, output open			50	µA
Supply current at HALT	IDDH				30	mA

(Ta = –40°C to +85°C , VDD = 5.0 V , VSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use of these ports are disabled

Support Tool

In-circuit Emulator PX-ICE102L00 + PX-PRB102L49-LQFP100-P-1414

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