MSC1200

SBAS289 – JUNE 2003

Precision Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with 8051 Microcontroller and Flash Memory

FEATURES

ANALOG FEATURES

- 24-BITS NO MISSING CODES
- 22-BITS EFFECTIVE RESOLUTION AT 10Hz
  Low Noise: 75nV
- PGA FROM 1 TO 128
- PRECISION ON-CHIP VOLTAGE REFERENCE:
  Accuracy: 0.2%
  Drift: 5ppm/°C
- 8 DIFFERENTIAL/SINGLE-ENDED CHANNELS
- ON-CHIP OFFSET/GAIN CALIBRATION
- OFFSET DRIFT: 0.02ppm/°C
- GAIN DRIFT: 0.5ppm/°C
- ON-CHIP TEMPERATURE SENSOR
- SELECTABLE BUFFER INPUT
- BURNOUT DETECT
- 8-BIT CURRENT DAC

DIGITAL FEATURES

Microcontroller Core

- 8051 COMPATIBLE
- HIGH SPEED CORE:
  4 Clocks per Instruction Cycle
- DC TO 33MHz
- ON-CHIP OSCILLATOR
- PLL WITH 32kHz CAPABILITY
- SINGLE INSTRUCTION 121ns
- DUAL DATA POINTER

Memory

- UP TO 8kB FLASH DATA MEMORY
- FLASH MEMORY PARTITIONING
- ENDURANCE 1M ERASE/WRITE CYCLES,
  100 YEAR DATA RETENTION
- IN-SYSTEM SERIALLY PROGRAMMABLE
- FLASH MEMORY SECURITY
- 1kB BOOT ROM
- PROGRAMMABLE WAIT STATE CONTROL

Peripheral Features

- 16 I/O PINS
- ADDITIONAL 32-BIT ACCUMULATOR
- TWO 16-BIT TIMER/COUNTERS
- SYSTEM TIMERS
- PROGRAMMABLE WATCHDOG TIMER
- FULL DUPLEX UART
- BASIC SPI™
- BASIC I²C™
- POWER MANAGEMENT CONTROL
- INTERNAL CLOCK DIVIDER
- IDLE MODE CURRENT < 200μA
- STOP MODE CURRENT < 100nA
- PROGRAMMABLE BROWNOUT RESET
- PROGRAMMABLE LOW VOLTAGE DETECT
- 20 INTERRUPT SOURCES

GENERAL FEATURES

- PACKAGE: TQFP-48
- LOW POWER: 4mW
- INDUSTRIAL TEMPERATURE RANGE:
  –40°C to +85°C
- POWER SUPPLY: 2.7V to 5.25V

PRODUCT PREVIEW

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS
- INTELLIGENT SENSORS
- PORTABLE APPLICATIONS
- DAS SYSTEMS

PACKAGE/ORDERING INFORMATION

PRODUCT	FLASH MEMORY	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
MSC1200Y2	4k	TQFP-48	PFB	–40°C to +85°C	MSC1200Y2	MSC1200Y2PFBT	Tape and Reel, 250
MSC1200Y2	4k	"	"	"	"	MSC1200Y2PFBR	Tape and Reel, 2000
MSC1200Y3	8k	TQFP-48	PFB	–40°C to +85°C	MSC1200Y3	MSC1200Y3PFBT	Tape and Reel, 250
MSC1200Y3	8k	"	"	"	"	MSC1200Y3PFBR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com/msc.

ABSOLUTE MAXIMUM RATINGS(1)

Analog Inputs
- Input Current ..... 100mA, Momentary
- Input Current ..... 10mA, Continuous
- Input Voltage ..... AGND – 0.5V to AV_{DD} + 0.5V

Power Supply
- DV_{DD} to DGND ..... –0.3V to 6V
- AV_{DD} to AGND ..... –0.3V to 6V
- AGND to DGND ..... –0.3V to +0.3V
- V_{REF} to AGND ..... –0.3V to AV_{DD} + 0.3V
- Digital Input Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
- Digital Output Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
- Maximum Junction Temperature ..... +150°C
- Operating Temperature Range ..... –40°C to +85°C
- Storage Temperature Range ..... –65°C to +150°C
- Lead Temperature (soldering, 10s) ..... +300°C
- Package Power Dissipation 822mW
- Output Current All Pins 200mA
- Output Pin Short Circuit 10s
- Thermal Resistance, Junction-to-Ambient (θ_{JA}) ..... 73°C/W
- Thermal Resistance, Junction-to-Case (θ_{JC}) ..... 12.8°C/W

Digital Outputs
- Output Current ..... 100mA, Continuous
- I/O Source/Sink Current 100mA
- Power Pin Maximum 300mA

NOTE: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MSC1200Yx FAMILY FEATURES

FEATURES(1)	MSC1200Y2(2)	MSC1200Y3(2)
Flash Program Memory (Bytes)	Up to 4k	Up to 8k
Flash Data Memory (Bytes)	Up to 4k	Up to 8k
Internal Scratchpad RAM (Bytes)	128	128

NOTES: (1) All peripheral features are the same on all devices; the flash memory size is the only difference. (2) The last digit of the part number (N) represents the onboard flash size = (2^N)kBytes.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted.

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Figure 4			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer ON		4		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Sensor Input Open Circuit		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}$/(2 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			1		ppm/°C

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (Cont.)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted.

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise			See Typical Characteristics		
No Missing Codes	Sinc³ Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input			±0.0015	%FSR
Offset Error	After Calibration		7.5		ppm of FS
Offset Drift(1)	Before Calibration		0.02		ppm of FS/°C
Gain Error(2)	After Calibration		0.005		%
Gain Error Drift(1)	Before Calibration		0.5		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS
Common-Mode Rejection	At DC	100	115		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = $-20\log(\Delta V_{OUT}/\Delta V_{DD})$(3)		88		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	0.0		AV_{DD}(2)	V
ADC V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–)	0.3	2.5	AV_{DD}	V
Common-Mode Rejection	At DC		110		dB
Input Current(4)	V_{REF} = 2.5V, ADC Only		10		µA
DAC Reference Current	For Each DAC, 5V Reference		25		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 1 at +25°C, PGA = 1, 2, 4, 8	2.495	2.5	2.505	V
	VREFH = 0		1.25		V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			8		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
IDAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current	Maximum V_{REF} = 2.5V		25		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} – 1.5		V
Relative Accuracy	Over Full Range		0.185		% of FSR
Zero Code Error			0.5		% of FSR
Full-Scale Error			–0.4		% of FSR
Gain Error			–0.6		% of FSR
ANALOG POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	4.75		5.25	V
Analog Current $I_{ADC} + I_{VREF}$	Analog OFF, PDAD = 1		< 1		nA
ADC Current I_{ADC}	PGA = 1, Buffer OFF		200		µA
	PGA = 128, Buffer OFF		500		µA
	PGA = 1, Buffer ON		240		µA
	PGA = 128, Buffer ON		850		µA
VDAC Current I_{VDAC}	Excluding Load Current External Reference		250		µA
V_{REF} Supply Current I_{VREF}	ADC ON, V_{DAC} OFF		250		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result. (4) 12pF switched capacitor at f_{SAMP} clock frequency.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications from T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and V_{REF} ≡ (REF IN+) – (REF IN–) = +1.25V, unless otherwise noted.

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Figure 4			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
Sinc^2 Filter	–3dB		0.318 • f_{DATA}		
Sinc^3 Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer On		4		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Sensor Input Open Circuit		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}/(2 \cdot PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise			See Typical Characteristics		
No Missing Codes	Sinc^3 Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input			±0.0015	%FSR
Offset Error	After Calibration		7.5		ppm of FS
Offset Drift(1)	Before Calibration		0.02		ppm of FS/°C
Gain Error(2)	After Calibration		0.005		%
Gain Error Drift(1)	Before Calibration		1.0		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS
Common-Mode Rejection	At DC	100	115		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = $-20\log(DV_{OUT}/DV_{DD})$(3)		85		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	0.0		AV_{DD}(2)	V
ADC V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.3	1.25	AV_{DD}	V
Common-Mode Rejection	At DC		110		dB
Input Current(4)	V_{REF} = 1.25V, ADC Only		10		µA
DAC Reference Current	For each DAC, 3V Reference		25		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 0 at +25°C, PGA = 1, 2, 4, 8	1.245	1.25	1.255	V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			2.6		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
IDAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current	Maximum V_{REF} = 2.5V		25		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} – 1.5		
Relative Accuracy	Over Full Range		0.185		% of FSR
Zero Code Error			0.5		% of FSR
Full-Scale Error			–0.4		% of FSR
Gain Error			–0.6		% of FSR

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (Cont.)

All specifications from T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, and Bipolar, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +1.25V, unless otherwise noted.

PARAMETER		CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Power-Supply Voltage		AV_{DD}	2.7		3.6	V
Analog Current	$I_{ADC} + I_{VREF}$	Analog OFF, PDAD = 1		< 1		nA
ADC Current	I_{ADC}	PGA = 1, Buffer OFF		200		µA
		PGA = 128, Buffer OFF		500		µA
		PGA = 1, Buffer ON		240		µA
		PGA = 128, Buffer ON		850		µA
VDAC Current	I_{VDAC}	Excluding Load Current External Reference		250		µA
V_{REF} Current	I_{VREF}			250		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result. (4) 12pF switched capacitor at f_{SAMP} clock frequency.

DIGITAL CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

All specifications from T_{MIN} to T_{MAX}, unless otherwise specified.

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
POWER-SUPPLY REQUIREMENTS					
	DV_{DD}	2.7		3.6	V
	Normal Mode, f_{OSC} = 1MHz		1.3		mA
	Normal Mode, f_{OSC} = 8MHz		6		mA
	Stop Mode		100		nA
	DV_{DD}	4.75		5.25	V
	Normal Mode, f_{OSC} = 1MHz		2.2		mA
	Normal Mode, f_{OSC} = 8MHz		14		mA
	Stop Mode		100		nA
DIGITAL INPUT/OUTPUT (CMOS)					
Logic Level: V_{IH} (except XIN pin)		0.6 • DV_{DD}		DV_{DD}	V
V_{IL} (except XIN pin)		DGND		0.2 • DV_{DD}	V
Ports 1 and 3, Input Leakage Current, Input Mode	$V_{IH} = DV_{DD}$ or V_{IH} = 0V	–10	0	+10	µA
Pin XIN Input Leakage Current			0		µA
V_{OL}, Ports 1 and 3, All Output Modes	I_{OL} = 1mA	DGND		0.4	V
V_{OL}, Ports 1 and 3, All Output Modes	I_{OL} = 30mA, 3V (20mA)		1.5		V
V_{OH}, Ports 1 and 3, Strong Drive Output	I_{OH} = 1mA	DV_{DD} – 0.4	DV_{DD} – 0.1	DV_{DD}	V
V_{OH}, Ports 1 and 3, Strong Drive Output	I_{OH} = 30mA, 3V (20mA)		DV_{DD} – 1.5		V
Ports 1 and 3 Pull-Up Resistors			9		kΩ
Pin Pull-Up Resistors	Flash Programming Mode Only		9		kΩ
Pin RST, Pull-Down Resistor			200		kΩ

PRODUCT PREVIEW

FLASH MEMORY CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

t_{USEC} = 1µs, t_{MSEC} = 1ms

PARAMETER	CONDITION	MSC1200Yx MIN	MSC1200Yx TYP	MSC1200Yx MAX	UNITS
Flash Memory Endurance		100,000	1,000,000		cycles
Flash Memory Data Retention		100			Years
Mass and Page Erase Time	Set with FER Value in FTCON	10			ms
Flash Memory Write Time	Set with FWR Value in FTCON	30		40	µs

AC ELECTRICAL CHARACTERISTICS[1][2]: DV_{DD} = 2.7V to 5.25V

SYMBOL	FIGURE	PARAMETER	2.7V to 3.6V		4.75V to 5.25V		UNITS
			MIN	MAX	MIN	MAX	
System Clock							
f_{OSC}[3]	A	External Crystal Frequency (f_{OSC})	1	16	1	33	MHz
$1/t_{OSC}$[3]	A	External Clock Frequency (f_{OSC})	0	16	1	33	MHz
f_{OSC}[3]	A	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz
External Clock							
t_{HIGH}	A	HIGH Time[4]	15		10		ns
t_{LOW}	A	LOW Time[4]	15		10		ns
t_R	A	Rise Time[4]		5		5	ns
t_F	A	Fall Time[4]		5		5	ns

NOTES: (1) Parameters are valid over operating temperature range, unless otherwise specified. (2) Load capacitance for outputs = 80pF. (3) $t_{CLK} = 1/f_{OSC}$ = one oscillator clock period for clock divider = 1. (4) These values are characterized but not 100% production tested.

EXPLANATION OF THE AC SYMBOLS

Each Timing Symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designators are:

C—Clock
D—Input Data
H—Logic Level HIGH
I—Instruction (program memory contents)
L—Logic Level LOW
Q—Output Data
t—Time
V—Valid
X—No Longer a Valid Logic Level
Z—Float

Examples: (1) t_{AVLL} = Time for address valid to ALE LOW. (2) t_{LLPL} = Time for ALE LOW to $\overline{PSEN}$ LOW.

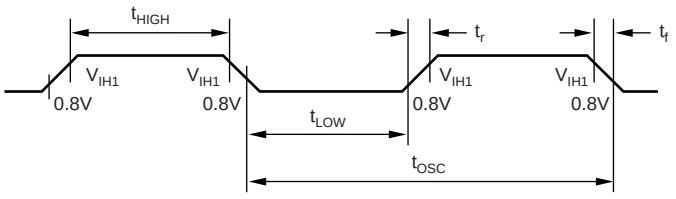
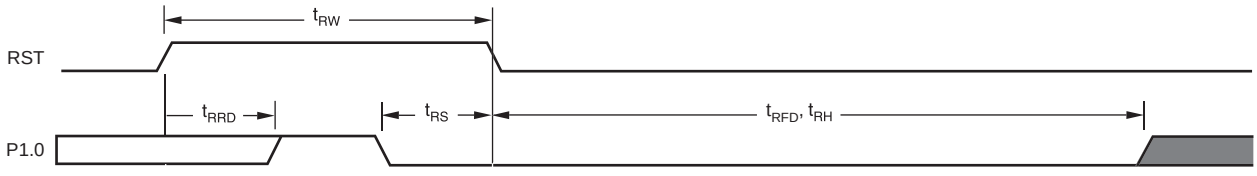


FIGURE A. External Clock Drive CLK.



NOTE: P1.0 is internally pulled-up with ~9kΩ during RST high.

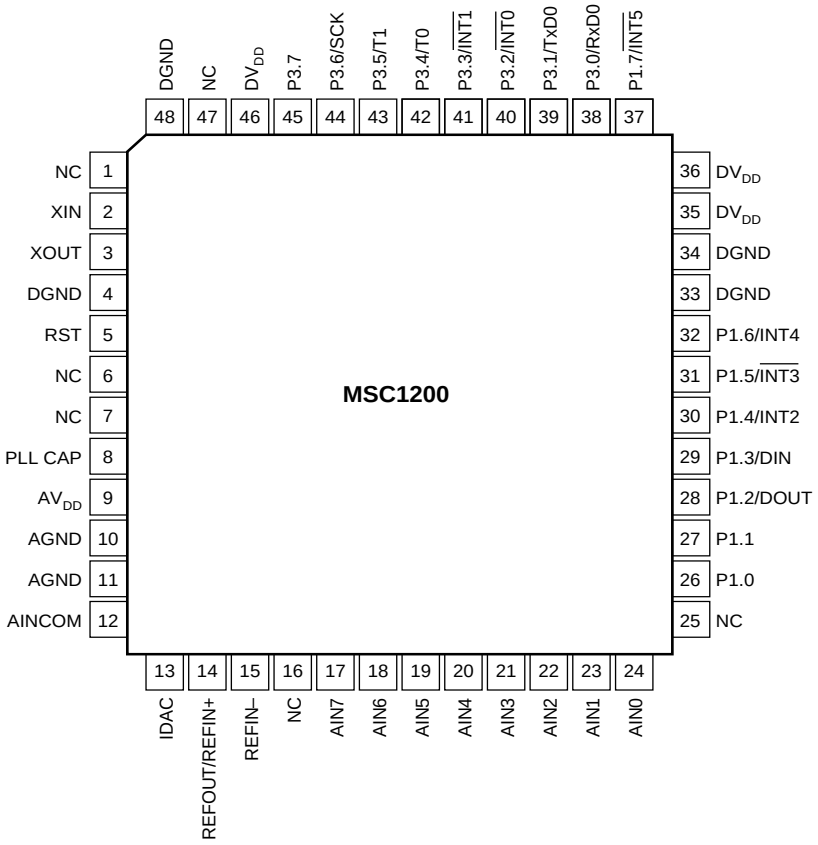
FIGURE B. Serial Flash Programming Power-On Timing.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RW}	RST width	2 t_{OSC}	—	ns
t_{RRD}	RST rise to P1.0 internal pull high	—	5	µs
t_{RFD}	RST falling to p1.0 start	—	$(2^{17} + 512)$ t_{OSC}	ns
t_{RS}	Input signal to RST falling setup time	t_{OSC}	—	ns
t_{RH}	RST falling to input signal hold time	$(2^{17} + 512)$ t_{OSC}	—	ns

PRODUCT PREVIEW

PIN CONFIGURATION

Top View **TQFP**



PRODUCT PREVIEW

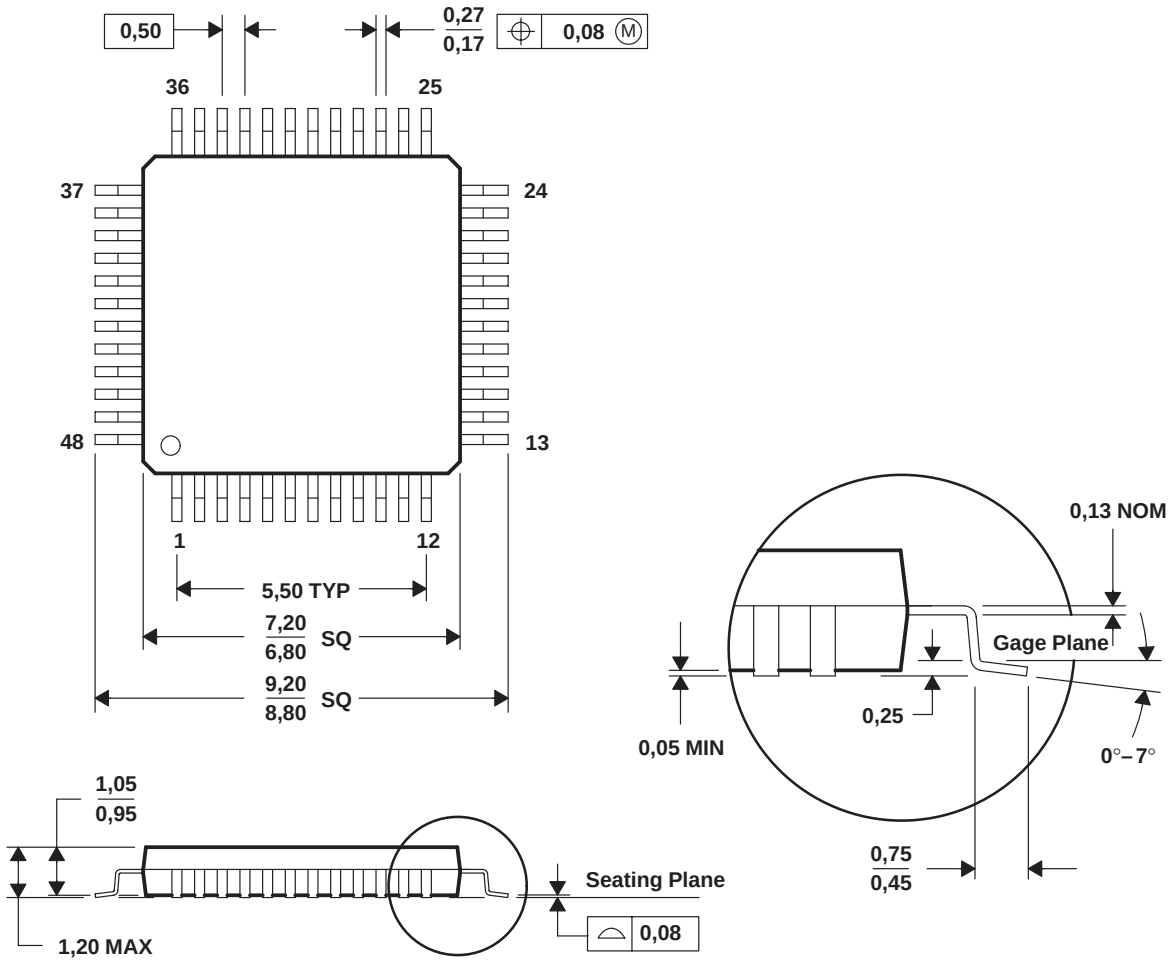
PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1,6,7,16,25,47	NC	No Connection
2	XIN	The crystal oscillator pin XIN supports parallel resonant AT cut crystals and ceramic resonators. XIN can also be an input if there is an external clock source instead of a crystal.
3	XOUT	The crystal oscillator pin XOUT supports parallel resonant AT cut crystals and ceramic resonators. XOUT serves as the output of the crystal amplifier.
4, 33, 34, 48	DGND	Digital Ground
5	RST	A HIGH on the reset input for two t_{OSC} periods will reset the device.
8	PLL CAP	
9	AV_{DD}	Analog Power Supply
10, 11	AGND	Analog Ground
12	AINCOM	Analog Common for Single-Ended Inputs
13	IDAC	IDAC Output
14	REFOUT/REF IN+	Voltage Reference Output/ Voltage Reference Positive Input
15	REF IN–	Voltage Reference Negative Input
17	AIN7	Analog Input Channel 7
18	AIN6	Analog Input Channel 6
19	AIN5	Analog Input Channel 5
20	AIN4	Analog Input Channel 4
21	AIN3	Analog Input Channel 3
22	AIN2	Analog Input Channel 2
23	AIN1	Analog Input Channel 1
24	AIN0	Analog Input Channel 0
26-32, 37	P1.0-P1.7	Port 1 is a bidirectional I/O port. The alternate functions for Port 1 are listed below. Port 1—Alternate Functions:
38-45	P3.0-P3.7	Port 3 is a bidirectional I/O port. The alternate functions for Port 3 are listed below. Port 3—Alternate Functions:
35, 36, 46	DV_{DD}	Digital Power Supply

PORT	ALTERNATE	MODE
P1.0	N/A	
P1.1	N/A	
P1.2	DOUT	Serial Data Out
P1.3	DIN	Serial Data In
P1.4	$\overline{INT2}$	External Interrupt 2
P1.5	$\overline{INT3}$	External Interrupt 3
P1.6	INT4	External Interrupt 4
P1.7	N/A	

PORT	ALTERNATE	MODE
P3.0	RxD0	Serial Port 0 Input
P3.1	TxD0	Serial Port 0 Output
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	SCK	SCK
P3.7	N/A	

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**

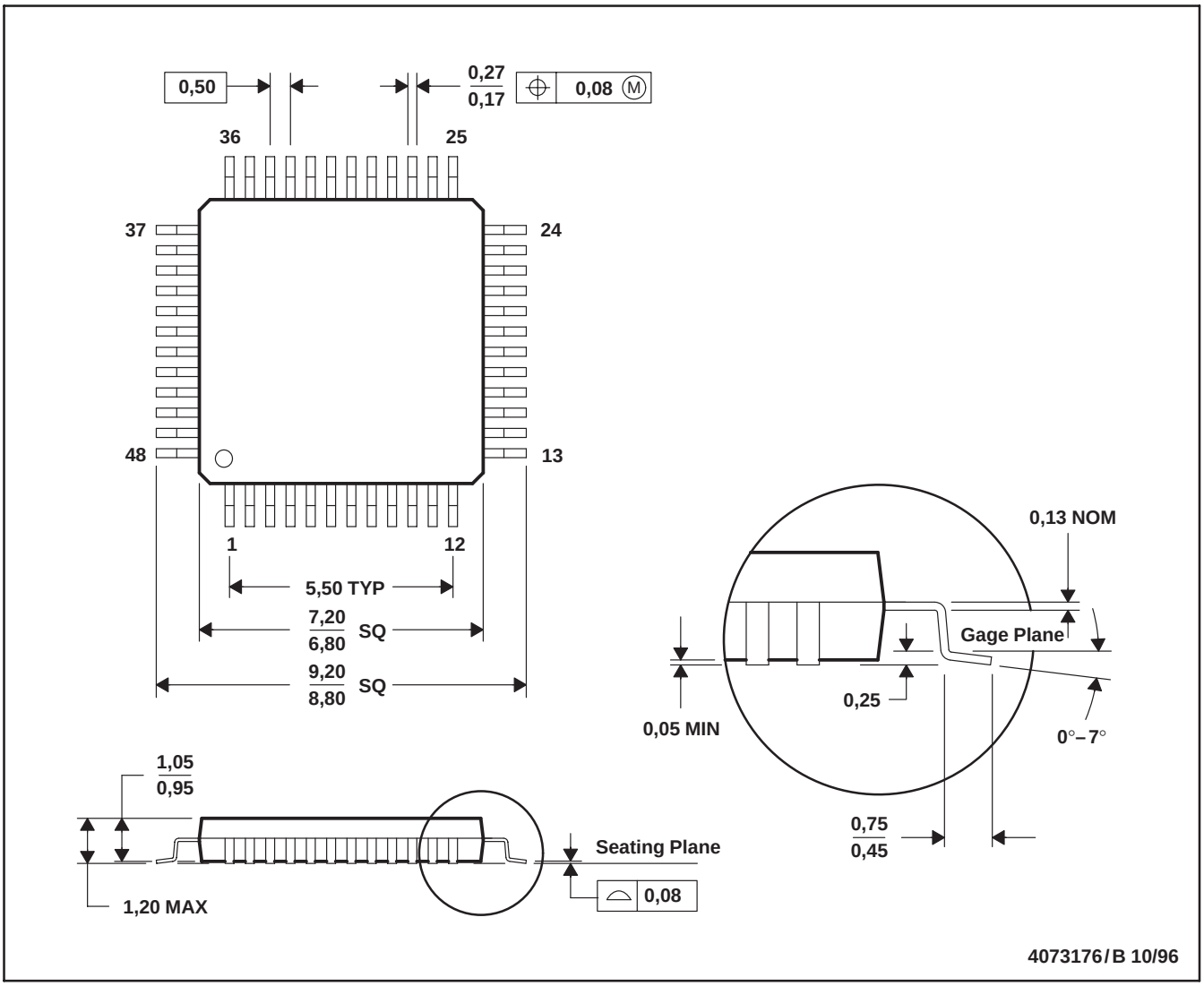


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PRODUCT PREVIEW

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265