NBSG16M

2.5V/3.3V SiGe Differential CML Receiver/Driver

The NBSG16M is a differential current mode logic (CML) receiver/driver. The device is functionally equivalent to the EP16, LVEP16, or SG16 devices with CML output structure and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The CML output structure contains internal 50 Ω source termination resistor to V_{CC}. The device generates 400 mV output amplitude with 50 Ω receiver resistor to V_{CC}.

The V_{BB} pin is internally generated voltage supply available to this device only. For all single−ended input conditions, the unused complementary differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} output should be left open.

- Maximum Input Clock Frequency > 10 GHz Typical
- Maximum Input Data Rate > 10 Gb/s Typical
- 120 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Positive CML Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Negative CML Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- CML Output Level; 400 mV Peak−to−Peak Output with 50 Ω Receiver Resistor to V_{CC}
- 50 Ω Internal Input and Output Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, LVEL and SG Devices
- V_{BB} Reference Voltage Output

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QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NBSG16MMN	3x3 mm QFN−16	123 Units / Rail
NBSG16MMNR2	3x3 mm QFN−16	3000/Tape & Reel

†For additional tape and reel information, refer to Brochure BRD8011/D.

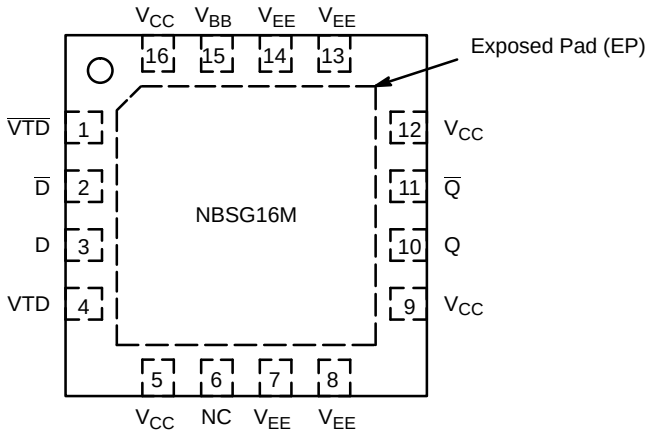


Figure 1. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TD}}$	−	Internal 50 Ω Termination Pin. See Table 2. (Note 3)
2	$\overline{D}$	LVDS, CML, ECL, LVTTL, LVCMOS Input	Inverted Differential Input (Note 3)
3	D	LVDS, CML, ECL, LVTTL, LVCMOS Input	Noninverted Differential Input. (Note 3)
4	V_{TD}	−	Internal 50 Ω Termination Pin. See Table 2. (Note 3)
5	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
6	NC	−	No Connect (Note 1)
7	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
8	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
9	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
10	Q	CML Output	Noninverted CML Differential Output with Internal 50 Ω Source Termination Resistor. (Note 2)
11	$\overline{Q}$	CML Output	Inverted CML Differential Output with Internal 50 Ω Source Termination Resistor. (Note 2)
12	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
13	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
14	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
15	V_{BB}	−	ECL Reference Output Voltage
16	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to Power Supply to guarantee proper operation.
−	EP	−	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat−sinking conduit.

1. The NC pins are electrically connected to the die and MUST be left open.
2. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.
3. In the differential configuration when the input termination pin (V_{TD}, $\overline{V_{TD}}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self−oscillation.

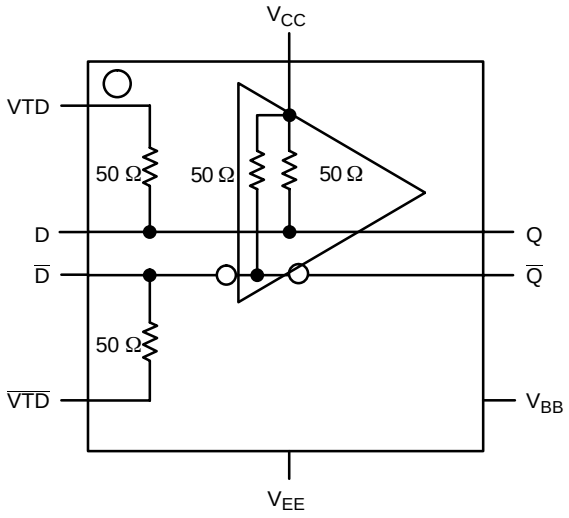


Figure 2. Logic Diagram

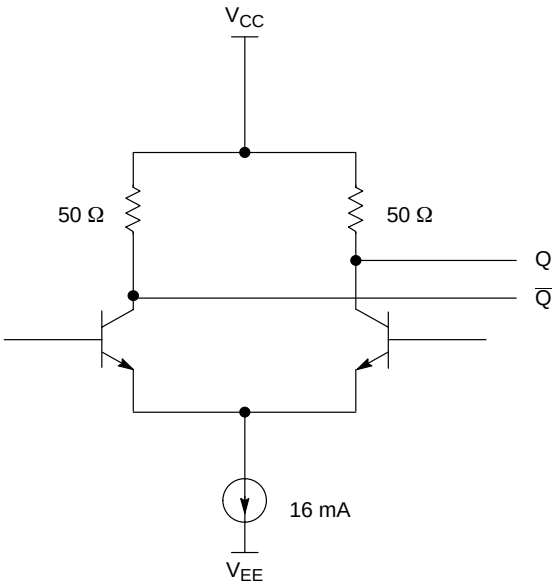


Figure 3. CML Output Structure

Table 2. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ together
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within (V_{IHCMR}) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complimentary differential input. Nominal voltage 1.5 V for LVTTL and V_{CC}/2 for LVCMOS inputs.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 kV > 100 V > 4 kV
Moisture Sensitivity (Note 4)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		145
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

4. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 5)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage |D − $\overline{D}$|	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\|V_{CC} - V_{EE}\|$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 6)	0 LFPM 500 LFPM	16 QFN 16 QFN	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 6)	16 QFN	4.0	°C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

5. Maximum Ratings are those values beyond which device damage may occur.
6. JEDEC standard multilayer board − 1S2P (1 signal, 2 power)

Table 5. DC CHARACTERISTICS, POSITIVE CML OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 7)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
V_{OH}	Output HIGH Voltage (Note 8)	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 7)		V_{CC} − 400	V_{CC}− 330		V_{CC} − 400	V_{CC}− 330		V_{CC} − 400	V_{CC}− 330	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 9)	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE}+ 1..275	V_{CC} − 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 9)	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V
V_{BB}	ECL Reference Voltage Output	1075	1170	1265	1075	1170	1265	1075	1170	1265	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 9) (Differential Configuration)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −0.965 V.
8. All loading with 50 Ω to V_{CC}.
9. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

Table 6. DC CHARACTERISTICS, POSITIVE CML OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 10)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
V_{OH}	Output HIGH Voltage (Note 11)	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 10)		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 12)	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 12)	V_{EE}	V_{CC} − 1.4*	V_{IH} − 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH} − 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH} − 0.150	V
V_{BB}	ECL Reference Voltage Output	1875	1970	2065	1875	1970	2065	1875	1970	2065	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 12) (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to −0.165 V.
11. All loading with 50 Ω to V_{CC}.
12. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

Table 7. DC CHARACTERISTICS, NEGATIVE CML OUTPUT V_{CC} = 0 V; V_{EE} = −3.465 to −2.375 V (Note 13)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC}	Positive Power Supply Current	37	43	51	37	43	51	37	43	51	mA
V_{OH}	Output HIGH Voltage (Note 14)	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	V_{CC} − 40	V_{CC} − 10	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 13)		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330		V_{CC} − 400	V_{CC} − 330	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 14)	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V_{EE} + 1.275	V_{CC} − 1.0*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single Ended) (Note 14)	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V_{EE}	V_{CC} − 1.4*	V_{IH}− 0.150	V
V_{BB}	ECL Reference Voltage Output	−1425	−1330	−1235	−1425	−1330	−1235	−1425	−1330	−1235	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 15) (Differential Configuration)	V_{EE}+1.2		V_{CC}	V_{EE}+1.2		V_{CC}	V_{EE}+1.2		V_{CC}	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		60	100		60	100		60	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

13. Input and output parameters vary 1:1 with V_{CC}.
14. All loading with 50 Ω to V_{CC}.
15. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

*Typicals used for testing purposes.

Table 8. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude (f_{in} < 7 GHz) (See Figure 4) (Note 16) (f_{in} < 10 GHz)	300 200	400 250		300 200	400 250		300 100	400 150		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	110	150	100	120	150	100	125	155	ps
t_{SKEW}	Duty Cycle Skew (Note 17)		3	15		3	15		3	15	ps
t_{JITTER}	RMS Random Clock Jitter (Note 19) f_{in} < 10 GHz Peak−to−Peak Data Dependent Jitter (Note 20) f_{in} < 10 Gb/s		0.2 8	1 15		0.2 8	1 15		0.2 8	1.0 15	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 18)	75		2500	75		2500	75		2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (Q, $\overline{Q}$) (20% − 80%)	21	35	53	21	35	53	21	35	53	ps

16. Measured using a 400 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
17. See Figure 5 $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
18. $V_{INPP(max)}$ cannot exceed $V_{CC} - V_{EE}$. (Applicable only when $V_{CC} - V_{EE}$ < 2500 mV). Input voltage swing is a single−ended measurement operating in differential mode.
19. Additive RMS jitter with 50% duty cycle clock signal at 10GHz.
20. Additive Peak−to−Peak data dependent jitter with NRZ PRBS2^{31}−1 data rate at 10 Gb/s.

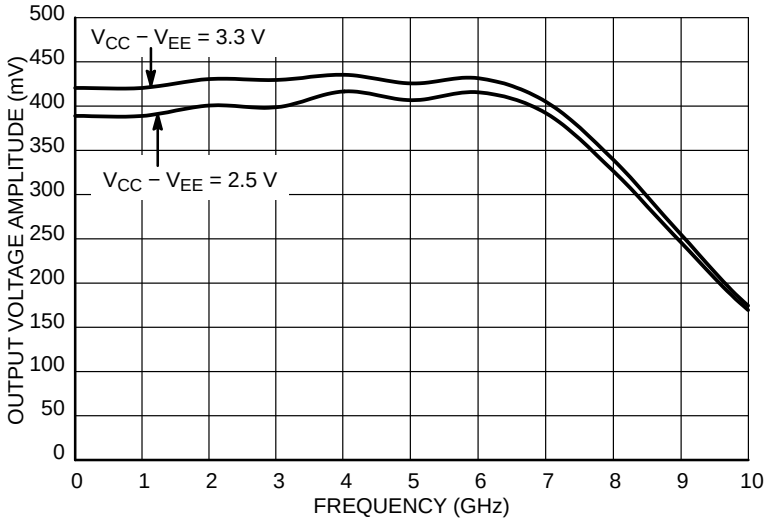


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical)

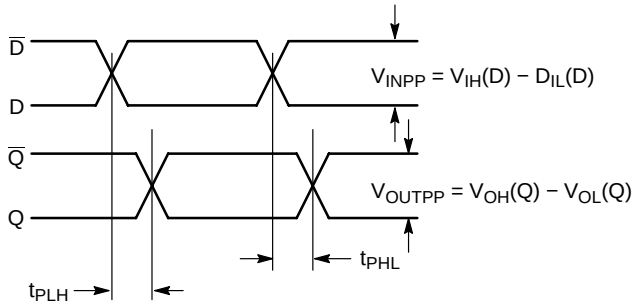


Figure 5. AC Reference Measurement

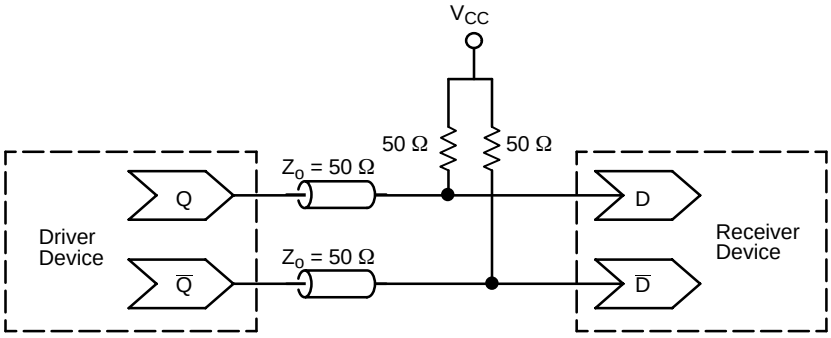


Figure 6. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 − Termination of ECL Logic Devices)

Application Information

All inputs can accept PECL, CML, and LVDS signal levels. The input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω).

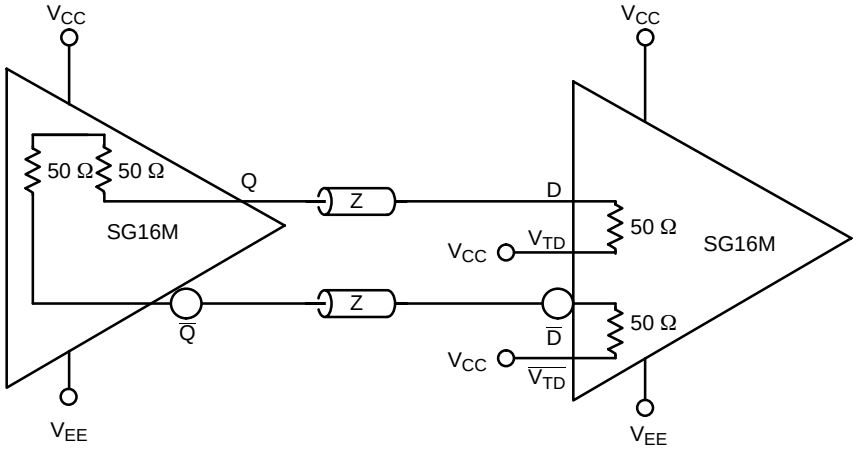
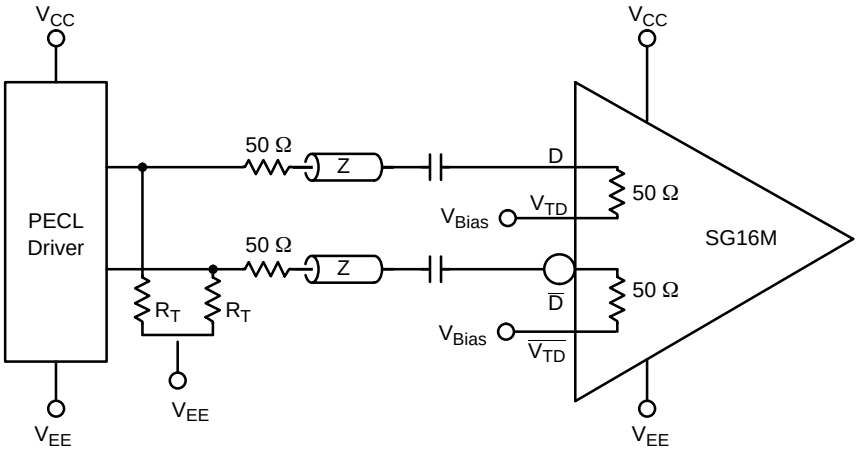


Figure 7. CML to CML Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

Figure 9. PECL to CML Receiver Interface

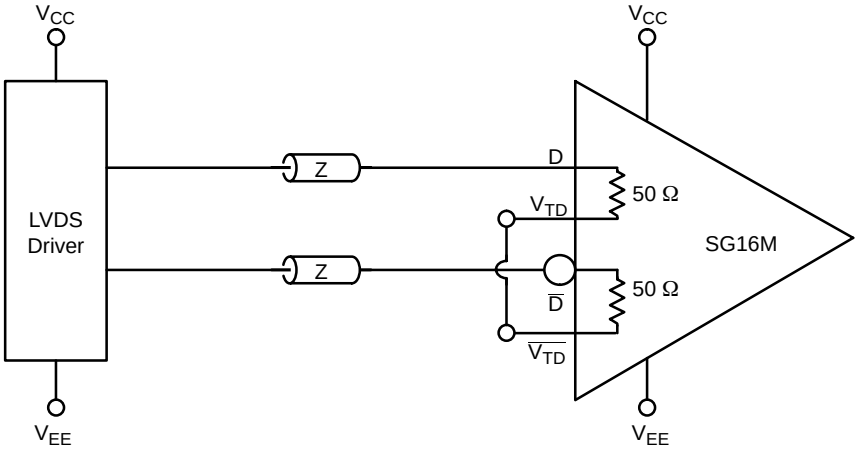
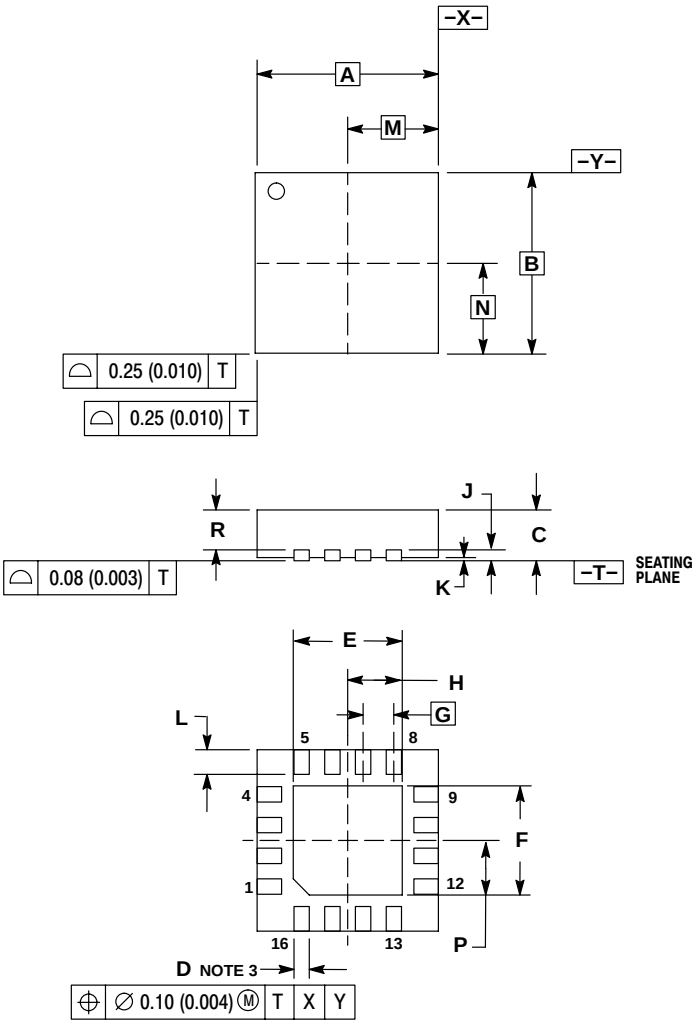


Figure 8. LVDS to CML Receiver Interface

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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