# 38-common x 132-segment+1-icon common Bitmap LCD Driver

## ■ GENERAL DESCRIPTION

The **NJU6674** is a Bitmap LCD Driver to display graphics or characters.

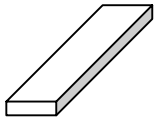
It contains 5,148 bits display data RAM, Microprocessor interface circuits, instruction decoder, 38-common and 132-segment +1-icon common drivers.

The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.

39 x 132 dots graphics or 10-character 3-line by 12 x 13 dot character with icon are displayed by **NJU6674** itself.

The wide operating voltage from 2.4V to 3.3V and low operating current are suitable for small sized battery operated items.

## ■ PACKAGE

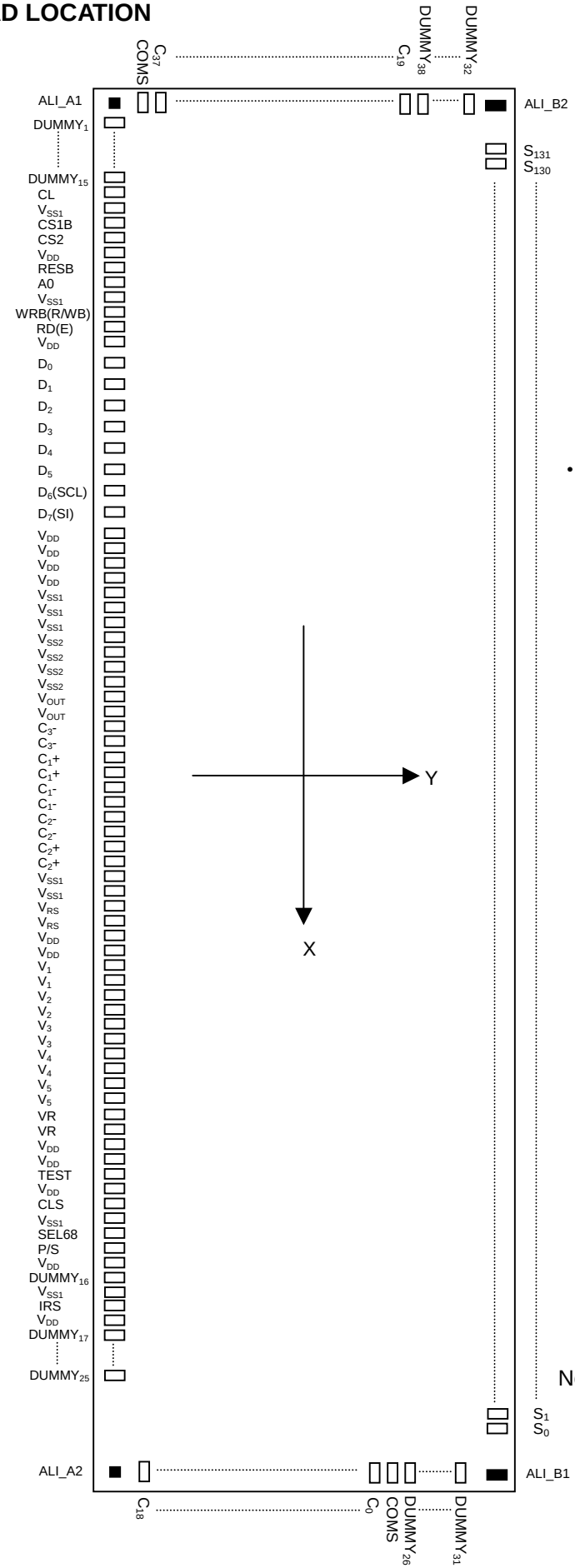


NJU6674CJ

## ■ FEATURES

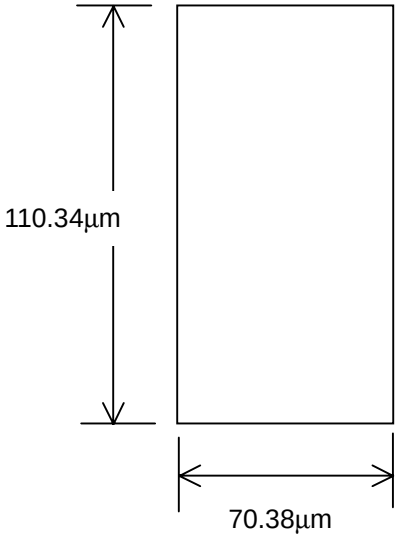
- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM : 5,148-bit
- LCD Drivers : 132-seg, 38-com+1-icon com
- Bias select 1/5 bias or 1/6 bias
- Direct interface with 68 and 80 type MPU
- Serial interface (SI, SCL, A0, $CS_1B$, $CS_2$)
- Useful Instruction Set
  Display ON/OFF ,Display Start Line Set, Page Address Set, Column Address Set, Status Read, Display Data Write, Display Data Read, ADC Select, Inverse Display, Entire display ON/OFF, Bias Select, Read Modify Write, End, Reset, Power control set, Internal resistor ratio set, EVR Register Set, EVR Mode Set, Power saving
- Power Supply Circuits for LCD incorporated
  Step up circuit (x2, x3, x4), Regulator, Voltage Follower x4, $V_5$ level is adjusted by internal bleeder resistancePrecision Electrical Variable Resistance (64-steps)
- Bias Stabilization Capacitor less
- Low power consumption
- Operating Voltage (All the voltages are based on $V_{DD}$=0V.)
  - Logic Operating -2.4 to -3.3V
  - Voltage Booster Operating Voltage -2.4 to -3.3 V
  - LCD Driving voltage -5.0 to -10.0V
- Rectangle outlook for COG
- Package outline: Bump-chip
- C-MOS Technology (Substrate: N)

## ■ PAD LOCATION

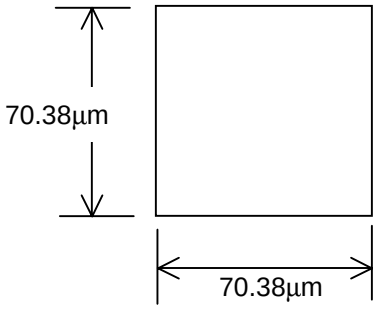



| | |
|---|---|
| Chip Center | :X=0µm,Y=0µm |
| Chip Size | :X=10.38mm, Y= 2.51mm |
| Chip Thickness | :400µm±30µm |
| Bump Size | :78.16µm x 48.10µm |
| PAD Pitch | :72µm(Min) |
| Bump Height | :17.5µm(Typ) |
| Bump Material | :Au |
| Voltage Boosting Polarity | :Negative Voltage($V_{DD}$ common) |
| Substrate | :N |

- Alignment marks




ALI_B1, ALI_B2




ALI_A1, ALI_A2

Note) Alignment Marks are not contains window.

## ■ PAD COORDINATES

Chip Size 10.38x2.51mm(Chip Center X=0μm, Y=0μm)

| PAD No. | Terminal | X= μm | Y= μm |
|---|---|---|---|
| 1 | $DUMMY_1$ | -4949 | -1098 |
| 2 | $DUMMY_2$ | -4877 | -1098 |
| 3 | $DUMMY_3$ | -4805 | -1098 |
| 4 | $DUMMY_4$ | -4733 | -1098 |
| 5 | $DUMMY_5$ | -4661 | -1098 |
| 6 | $DUMMY_6$ | -4589 | -1098 |
| 7 | $DUMMY_7$ | -4517 | -1098 |
| 8 | $DUMMY_8$ | -4445 | -1098 |
| 9 | $DUMMY_9$ | -4373 | -1098 |
| 10 | $DUMMY_{10}$ | -4301 | -1098 |
| 11 | $DUMMY_{11}$ | -4229 | -1098 |
| 12 | $DUMMY_{12}$ | -4157 | -1098 |
| 13 | $DUMMY_{13}$ | -4085 | -1098 |
| 14 | $DUMMY_{14}$ | -4013 | -1098 |
| 15 | $DUMMY_{15}$ | -3941 | -1098 |
| 16 | CL | -3869 | -1098 |
| 17 | $V_{SS1}$ | -3797 | -1098 |
| 18 | CS1B | -3725 | -1098 |
| 19 | CS2 | -3653 | -1098 |
| 20 | $V_{DD}$ | -3581 | -1098 |
| 21 | RESB | -3509 | -1098 |
| 22 | A0 | -3437 | -1098 |
| 23 | $V_{SS1}$ | -3365 | -1098 |
| 24 | WRB | -3293 | -1098 |
| 25 | RDB | -3221 | -1098 |
| 26 | $V_{DD}$ | -3149 | -1098 |
| 27 | $D_0$ | -2879 | -1098 |
| 28 | $D_1$ | -2599 | -1098 |
| 29 | $D_2$ | -2319 | -1098 |
| 30 | $D_3$ | -2039 | -1098 |
| 31 | $D_4$ | -1759 | -1098 |
| 32 | $D_5$ | -1479 | -1098 |
| 33 | $D_6$(SCL) | -1199 | -1098 |
| 34 | $D_7$(SI) | -919 | -1098 |
| 35 | $V_{DD}$ | -710 | -1098 |
| 36 | $V_{DD}$ | -638 | -1098 |
| 37 | $V_{DD}$ | -566 | -1098 |
| 38 | $V_{DD}$ | -494 | -1098 |
| 39 | $V_{SS1}$ | -422 | -1098 |
| 40 | $V_{SS1}$ | -350 | -1098 |
| 41 | $V_{SS1}$ | -278 | -1098 |
| 42 | $V_{SS2}$ | -206 | -1098 |
| 43 | $V_{SS2}$ | -134 | -1098 |
| 44 | $V_{SS2}$ | -62 | -1098 |
| 45 | $V_{SS2}$ | 10 | -1098 |
| 46 | $V_{OUT}$ | 82 | -1098 |
| 47 | $V_{OUT}$ | 154 | -1098 |
| 48 | C3- | 226 | -1098 |
| 49 | C3- | 298 | -1098 |
| 50 | C1+ | 370 | -1098 |

| PAD No. | Terminal | X= μm | Y= μm |
|---|---|---|---|
| 51 | C1+ | 442 | -1098 |
| 52 | C1- | 514 | -1098 |
| 53 | C1- | 586 | -1098 |
| 54 | C2- | 658 | -1098 |
| 55 | C2- | 730 | -1098 |
| 56 | C2+ | 802 | -1098 |
| 57 | C2+ | 874 | -1098 |
| 58 | $V_{SS1}$ | 946 | -1098 |
| 59 | $V_{SS1}$ | 1018 | -1098 |
| 60 | $V_{RS}$ | 1090 | -1098 |
| 61 | $V_{RS}$ | 1162 | -1098 |
| 62 | $V_{DD}$ | 1234 | -1098 |
| 63 | $V_{DD}$ | 1306 | -1098 |
| 64 | $V_1$ | 1378 | -1098 |
| 65 | $V_1$ | 1450 | -1098 |
| 66 | $V_2$ | 1522 | -1098 |
| 67 | $V_2$ | 1594 | -1098 |
| 68 | $V_3$ | 1666 | -1098 |
| 69 | $V_3$ | 1738 | -1098 |
| 70 | $V_4$ | 1810 | -1098 |
| 71 | $V_4$ | 1882 | -1098 |
| 72 | $V_5$ | 1954 | -1098 |
| 73 | $V_5$ | 2026 | -1098 |
| 74 | VR | 2098 | -1098 |
| 75 | VR | 2170 | -1098 |
| 76 | $V_{DD}$ | 2242 | -1098 |
| 77 | $V_{DD}$ | 2314 | -1098 |
| 78 | TEST | 2386 | -1098 |
| 79 | $V_{DD}$ | 2458 | -1098 |
| 80 | CLS | 2530 | -1098 |
| 81 | $V_{SS1}$ | 2602 | -1098 |
| 82 | SEL68 | 2674 | -1098 |
| 83 | P/S | 2746 | -1098 |
| 84 | $V_{DD}$ | 2818 | -1098 |
| 85 | $DUMMY_{16}$ | 2890 | -1098 |
| 86 | $V_{SS1}$ | 2962 | -1098 |
| 87 | IRS | 3034 | -1098 |
| 88 | $V_{DD}$ | 3106 | -1098 |
| 89 | $DUMMY_{17}$ | 3178 | -1098 |
| 90 | $DUMMY_{18}$ | 3250 | -1098 |
| 91 | $DUMMY_{19}$ | 3322 | -1098 |
| 92 | $DUMMY_{20}$ | 3394 | -1098 |
| 93 | $DUMMY_{21}$ | 3466 | -1098 |
| 94 | $DUMMY_{22}$ | 3538 | -1098 |
| 95 | $DUMMY_{23}$ | 3610 | -1098 |
| 96 | $DUMMY_{24}$ | 3682 | -1098 |
| 97 | $DUMMY_{25}$ | 3754 | -1098 |
| 98 | ALI_A2 | 5036 | -1098 |
| 99 | $C_{18}$ | 5036 | -943 |
| 100 | $C_{17}$ | 5036 | -871 |

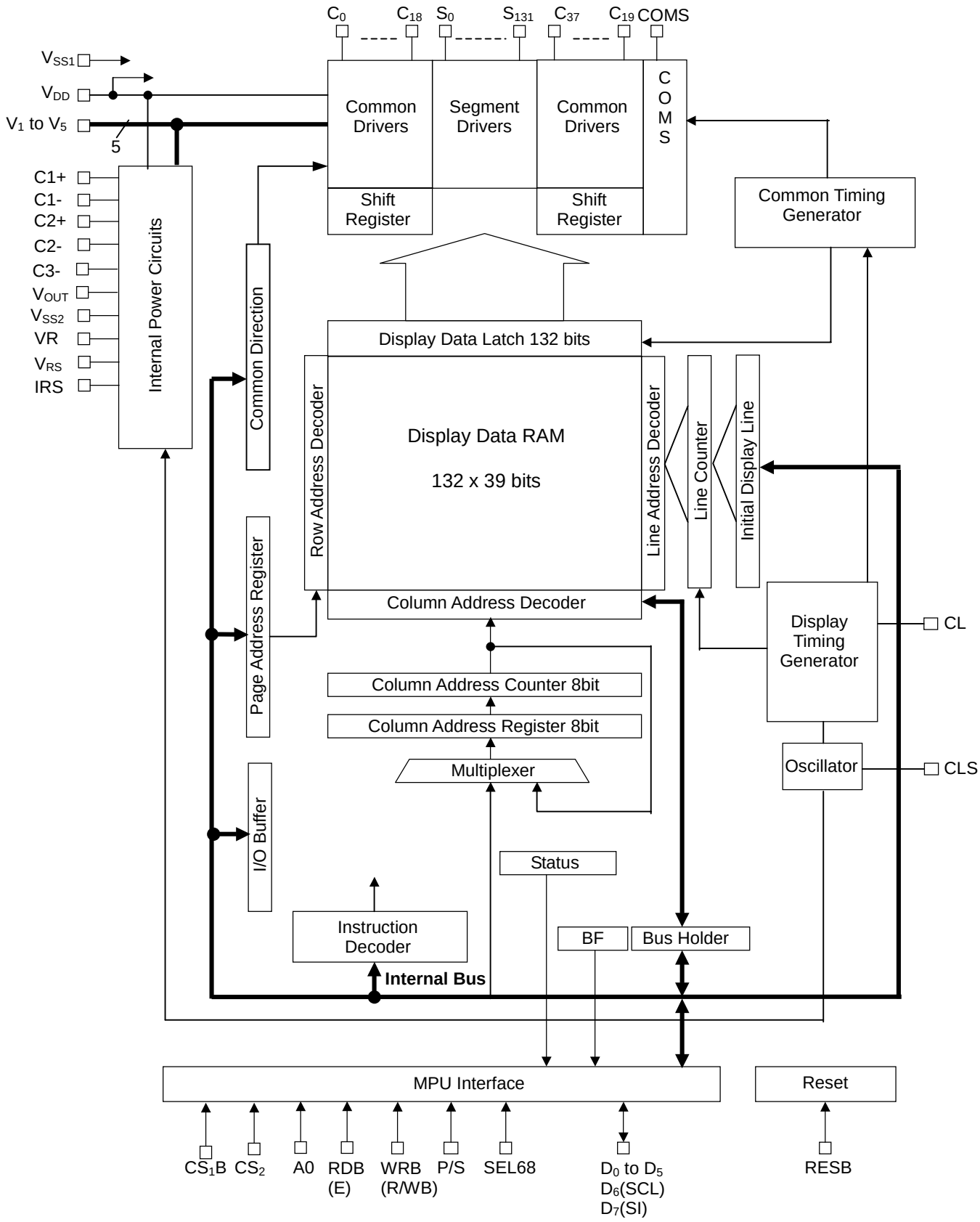
| PAD No. | Terminal | X= µm | Y= µm |
|---|---|---|---|
| 101 | $C_{16}$ | 5036 | -799 |
| 102 | $C_{15}$ | 5036 | -727 |
| 103 | $C_{14}$ | 5036 | -655 |
| 104 | $C_{13}$ | 5036 | -583 |
| 105 | $C_{12}$ | 5036 | -511 |
| 106 | $C_{11}$ | 5036 | -439 |
| 107 | $C_{10}$ | 5036 | -367 |
| 108 | $C_9$ | 5036 | -295 |
| 109 | $C_8$ | 5036 | -223 |
| 110 | $C_7$ | 5036 | -151 |
| 111 | $C_6$ | 5036 | -79 |
| 112 | $C_5$ | 5036 | -7 |
| 113 | $C_4$ | 5036 | 65 |
| 114 | $C_3$ | 5036 | 137 |
| 115 | $C_2$ | 5036 | 209 |
| 116 | $C_1$ | 5036 | 281 |
| 117 | $C_0$ | 5036 | 353 |
| 118 | COMS | 5036 | 425 |
| 119 | $DUMMY_{26}$ | 5036 | 569 |
| 120 | $DUMMY_{27}$ | 5036 | 641 |
| 121 | $DUMMY_{28}$ | 5036 | 713 |
| 122 | $DUMMY_{29}$ | 5036 | 785 |
| 123 | $DUMMY_{30}$ | 5036 | 857 |
| 124 | $DUMMY_{31}$ | 5036 | 929 |
| 125 | ALI_B1 | 5036 | 1089 |
| 126 | $S_0$ | 4716 | 1098 |
| 127 | $S_1$ | 4644 | 1098 |
| 128 | $S_2$ | 4572 | 1098 |
| 129 | $S_3$ | 4500 | 1098 |
| 130 | $S_4$ | 4428 | 1098 |
| 131 | $S_5$ | 4356 | 1098 |
| 132 | $S_6$ | 4284 | 1098 |
| 133 | $S_7$ | 4212 | 1098 |
| 134 | $S_8$ | 4140 | 1098 |
| 135 | $S_9$ | 4068 | 1098 |
| 136 | $S_{10}$ | 3996 | 1098 |
| 137 | $S_{11}$ | 3924 | 1098 |
| 138 | $S_{12}$ | 3852 | 1098 |
| 139 | $S_{13}$ | 3780 | 1098 |
| 140 | $S_{14}$ | 3708 | 1098 |
| 141 | $S_{15}$ | 3636 | 1098 |
| 142 | $S_{16}$ | 3564 | 1098 |
| 143 | $S_{17}$ | 3492 | 1098 |
| 144 | $S_{18}$ | 3420 | 1098 |
| 145 | $S_{19}$ | 3348 | 1098 |
| 146 | $S_{20}$ | 3276 | 1098 |
| 147 | $S_{21}$ | 3204 | 1098 |
| 148 | $S_{22}$ | 3132 | 1098 |
| 149 | $S_{23}$ | 3060 | 1098 |
| 150 | $S_{24}$ | 2988 | 1098 |

| PAD No. | Terminal | X= µm | Y= µm |
|---|---|---|---|
| 151 | $S_{25}$ | 2916 | 1098 |
| 152 | $S_{26}$ | 2844 | 1098 |
| 153 | $S_{27}$ | 2772 | 1098 |
| 154 | $S_{28}$ | 2700 | 1098 |
| 155 | $S_{29}$ | 2628 | 1098 |
| 156 | $S_{30}$ | 2556 | 1098 |
| 157 | $S_{31}$ | 2484 | 1098 |
| 158 | $S_{32}$ | 2412 | 1098 |
| 159 | $S_{33}$ | 2340 | 1098 |
| 160 | $S_{34}$ | 2268 | 1098 |
| 161 | $S_{35}$ | 2196 | 1098 |
| 162 | $S_{36}$ | 2124 | 1098 |
| 163 | $S_{37}$ | 2052 | 1098 |
| 164 | $S_{38}$ | 1980 | 1098 |
| 165 | $S_{39}$ | 1908 | 1098 |
| 166 | $S_{40}$ | 1836 | 1098 |
| 167 | $S_{41}$ | 1764 | 1098 |
| 168 | $S_{42}$ | 1692 | 1098 |
| 169 | $S_{43}$ | 1620 | 1098 |
| 170 | $S_{44}$ | 1548 | 1098 |
| 171 | $S_{45}$ | 1476 | 1098 |
| 172 | $S_{46}$ | 1404 | 1098 |
| 173 | $S_{47}$ | 1332 | 1098 |
| 174 | $S_{48}$ | 1260 | 1098 |
| 175 | $S_{49}$ | 1188 | 1098 |
| 176 | $S_{50}$ | 1116 | 1098 |
| 177 | $S_{51}$ | 1044 | 1098 |
| 178 | $S_{52}$ | 972 | 1098 |
| 179 | $S_{53}$ | 900 | 1098 |
| 180 | $S_{54}$ | 828 | 1098 |
| 181 | $S_{55}$ | 756 | 1098 |
| 182 | $S_{56}$ | 684 | 1098 |
| 183 | $S_{57}$ | 612 | 1098 |
| 184 | $S_{58}$ | 540 | 1098 |
| 185 | $S_{59}$ | 468 | 1098 |
| 186 | $S_{60}$ | 396 | 1098 |
| 187 | $S_{61}$ | 324 | 1098 |
| 188 | $S_{62}$ | 252 | 1098 |
| 189 | $S_{63}$ | 180 | 1098 |
| 190 | $S_{64}$ | 108 | 1098 |
| 191 | $S_{65}$ | 36 | 1098 |
| 192 | $S_{66}$ | -36 | 1098 |
| 193 | $S_{67}$ | -108 | 1098 |
| 194 | $S_{68}$ | -180 | 1098 |
| 195 | $S_{69}$ | -252 | 1098 |
| 196 | $S_{70}$ | -324 | 1098 |
| 197 | $S_{71}$ | -396 | 1098 |
| 198 | $S_{72}$ | -468 | 1098 |
| 199 | $S_{73}$ | -540 | 1098 |
| 200 | $S_{74}$ | -612 | 1098 |

| PAD No. | Terminal | X= μm | Y= μm |
|---|---|---|---|
| 201 | $S_{75}$ | -684 | 1098 |
| 202 | $S_{76}$ | -756 | 1098 |
| 203 | $S_{77}$ | -828 | 1098 |
| 204 | $S_{78}$ | -900 | 1098 |
| 205 | $S_{79}$ | -972 | 1098 |
| 206 | $S_{80}$ | -1044 | 1098 |
| 207 | $S_{81}$ | -1116 | 1098 |
| 208 | $S_{82}$ | -1188 | 1098 |
| 209 | $S_{83}$ | -1260 | 1098 |
| 210 | $S_{84}$ | -1332 | 1098 |
| 211 | $S_{85}$ | -1404 | 1098 |
| 212 | $S_{86}$ | -1476 | 1098 |
| 213 | $S_{87}$ | -1548 | 1098 |
| 214 | $S_{88}$ | -1620 | 1098 |
| 215 | $S_{89}$ | -1692 | 1098 |
| 216 | $S_{90}$ | -1764 | 1098 |
| 217 | $S_{91}$ | -1836 | 1098 |
| 218 | $S_{92}$ | -1908 | 1098 |
| 219 | $S_{93}$ | -1980 | 1098 |
| 220 | $S_{94}$ | -2052 | 1098 |
| 221 | $S_{95}$ | -2124 | 1098 |
| 222 | $S_{96}$ | -2196 | 1098 |
| 223 | $S_{97}$ | -2268 | 1098 |
| 224 | $S_{98}$ | -2340 | 1098 |
| 225 | $S_{99}$ | -2412 | 1098 |
| 226 | $S_{100}$ | -2484 | 1098 |
| 227 | $S_{101}$ | -2556 | 1098 |
| 228 | $S_{102}$ | -2628 | 1098 |
| 229 | $S_{103}$ | -2700 | 1098 |
| 230 | $S_{104}$ | -2772 | 1098 |
| 231 | $S_{105}$ | -2844 | 1098 |
| 232 | $S_{106}$ | -2916 | 1098 |
| 233 | $S_{107}$ | -2988 | 1098 |
| 234 | $S_{108}$ | -3060 | 1098 |
| 235 | $S_{109}$ | -3132 | 1098 |
| 236 | $S_{110}$ | -3204 | 1098 |
| 237 | $S_{111}$ | -3276 | 1098 |
| 238 | $S_{112}$ | -3348 | 1098 |
| 239 | $S_{113}$ | -3420 | 1098 |
| 240 | $S_{114}$ | -3492 | 1098 |
| 241 | $S_{115}$ | -3564 | 1098 |
| 242 | $S_{116}$ | -3636 | 1098 |
| 243 | $S_{117}$ | -3708 | 1098 |
| 244 | $S_{118}$ | -3780 | 1098 |
| 245 | $S_{119}$ | -3852 | 1098 |
| 246 | $S_{120}$ | -3924 | 1098 |
| 247 | $S_{121}$ | -3996 | 1098 |
| 248 | $S_{122}$ | -4068 | 1098 |
| 249 | $S_{123}$ | -4140 | 1098 |
| 250 | $S_{124}$ | -4212 | 1098 |

| PAD No. | Terminal | X= μm | Y= μm |
|---|---|---|---|
| 251 | $S_{125}$ | -4284 | 1098 |
| 252 | $S_{126}$ | -4356 | 1098 |
| 253 | $S_{127}$ | -4428 | 1098 |
| 254 | $S_{128}$ | -4500 | 1098 |
| 255 | $S_{129}$ | -4572 | 1098 |
| 256 | $S_{130}$ | -4644 | 1098 |
| 257 | $S_{131}$ | -4716 | 1098 |
| 258 | ALI_B2 | -5036 | 1089 |
| 259 | $DUMMY_{32}$ | -5036 | 929 |
| 260 | $DUMMY_{33}$ | -5036 | 857 |
| 261 | $DUMMY_{34}$ | -5036 | 785 |
| 262 | $DUMMY_{35}$ | -5036 | 713 |
| 263 | $DUMMY_{36}$ | -5036 | 641 |
| 264 | $DUMMY_{37}$ | -5036 | 569 |
| 265 | $DUMMY_{38}$ | -5036 | 497 |
| 266 | $C_{19}$ | -5036 | 425 |
| 267 | $C_{20}$ | -5036 | 353 |
| 268 | $C_{21}$ | -5036 | 281 |
| 269 | $C_{22}$ | -5036 | 209 |
| 270 | $C_{23}$ | -5036 | 137 |
| 271 | $C_{24}$ | -5036 | 65 |
| 272 | $C_{25}$ | -5036 | -7 |
| 273 | $C_{26}$ | -5036 | -79 |
| 274 | $C_{27}$ | -5036 | -151 |
| 275 | $C_{28}$ | -5036 | -223 |
| 276 | $C_{29}$ | -5036 | -295 |
| 277 | $C_{30}$ | -5036 | -367 |
| 278 | $C_{31}$ | -5036 | -439 |
| 279 | $C_{32}$ | -5036 | -511 |
| 280 | $C_{33}$ | -5036 | -583 |
| 281 | $C_{34}$ | -5036 | -655 |
| 282 | $C_{35}$ | -5036 | -727 |
| 283 | $C_{36}$ | -5036 | -799 |
| 284 | $C_{37}$ | -5036 | -871 |
| 285 | COMS | -5036 | -943 |
| 286 | ALI_A1 | -5036 | -1098 |

## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>1 to 15<br>85<br>89 to 97<br>119 to 124<br>259 to 265</td><td>$DUMMY_1$ to<br>$DUMMY_{38}$</td><td></td><td>Dummy Terminals.<br>These are open terminals electrically.</td></tr>
<tr><td>20,26,<br>35 to 38,<br>62 to 63,<br>76 to 77,<br>79,84,88</td><td>$V_{DD}$</td><td>Power</td><td>Power supply terminals.</td></tr>
<tr><td>17,23,<br>39 to 41,<br>58 to 59,<br>81,86</td><td>$V_{SS1}$</td><td>GND</td><td>Ground terminal.</td></tr>
<tr><td>42 to 45</td><td>$V_{SS2}$</td><td>Power</td><td>Reference voltage for voltage booster</td></tr>
<tr><td>60 to 61</td><td>$V_{RS}$</td><td>I</td><td>External reference voltage input terminal.</td></tr>
<tr><td>64,65<br>66,67<br>68,69<br>70,71<br>72,73</td><td>$V_1$<br>$V_2$<br>$V_3$<br>$V_4$<br>$V_5$</td><td>Power</td><td>LCD Driving Voltage Supplying Terminal. When the internal voltage booster is not used, supply each level of LCD driving voltage from outside with following relation.<br>$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$<br>When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from $V_1$ to $V_4$ terminal.
<table>
<tr><th>Bias</th><th>$V_1$</th><th>$V_2$</th><th>$V_3$</th><th>$V_4$</th></tr>
<tr><td>1/5 Bias</td><td>$V_5$+4/5 $V_{LCD}$</td><td>$V_5$+3/5 $V_{LCD}$</td><td>$V_5$+2/5 $V_{LCD}$</td><td>$V_5$+1/5 $V_{LCD}$</td></tr>
<tr><td>1/6 Bias</td><td>$V_5$+5/6 $V_{LCD}$</td><td>$V_5$+4/6 $V_{LCD}$</td><td>$V_5$+2/6 $V_{LCD}$</td><td>$V_5$+1/6 $V_{LCD}$</td></tr>
</table>
$V_{LCD}=V_{DD}-V_5$</td></tr>
<tr><td>50,51<br>52,53<br>56,57<br>54,55<br>48,49</td><td>C1+<br>C1-<br>C2+<br>C2-<br>C3-</td><td>O</td><td>Boosted capacitor connecting terminals used for voltage booster.</td></tr>
<tr><td>46,47</td><td>$V_{OUT}$</td><td>O</td><td>Voltage booster output terminal. Connect the boosted capacitor between this terminal and $V_{SS1}$.</td></tr>
<tr><td>74,75</td><td>VR</td><td>I</td><td>Voltage adjust terminal. $V_5$ level is adjusted by external bleeder resistance connecting between $V_{DD}$ and $V_5$ terminal.(IRS="L")<br>IRS terminal connect with "H" at the time of built-in resistance used. “H” , this terminal must connect to "H" or "L".</td></tr>
<tr><td>27<br>28<br>29<br>30<br>31<br>32<br>33<br>34</td><td>$D_0$<br>$D_1$<br>$D_2$<br>$D_3$<br>$D_4$<br>$D_5$<br>$D_6$(SCL)<br>$D_7$(SI)</td><td>I/O</td><td>P/S="H": Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.<br>P/S="L" : Serial data input terminal. ($D_7$ )<br>Serial data clock signal input terminal. ($D_6$ ) Data from SI is loaded at the rising edge of SCL and latched as the parallel data at 8th rising edge of SCL.</td></tr>
<tr><td>87</td><td>IRS</td><td>I</td><td>Internal resistor select terminal<br>“H”: Internal<br>“L”: External<br>This terminal must connect to "H" or "L".</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>22</td><td>A0</td><td>I</td><td>Connect to the Address bus of MPU. The data on the $D_0$ to $D_7$ is distinguished between Display data and Instruction by status of A0.
<table>
<tr><td>A0</td><td>H</td><td>L</td></tr>
<tr><td>Discrimination.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>21</td><td>RESB</td><td>I</td><td>Reset terminal. When the RESB terminal goes to “L”, the initialization is performed.<br>Reset operation is executing during “L” state of RESB.</td></tr>
<tr><td>18<br>19</td><td>$CS_1B$<br>$CS_2$</td><td>I</td><td>Chip select terminal. Data Input/Output are available during $CS_1B$=”L” and $CS_2$=”H”.</td></tr>
<tr><td>25</td><td>RDB(E)</td><td>I</td><td><In case of 80 Type MPU><br>RDB signal of 80 type MPU input terminal. Active "L"<br>During this signal is "L" , $D_0$ to $D_7$ terminals are output.<br><In case of 68 Type MPU><br>Enable signal of 68 type MPU input terminal. Active "H"</td></tr>
<tr><td>24</td><td>WRB(R/WB)</td><td>I</td><td><In case of 80 Type MPU><br>Connect to the 80 type MPU WRB signal. Active "L".<br>The data on the data bus input synchronizing the rise edge of this signal.<br><In case of 68 Type MPU><br>The read/write control signal of 68 type MPU input terminal.
<table>
<tr><td>R/WB</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>82</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal.<br>This terminal must connect to $V_{DD}$ or $V_{SS}$.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>83</td><td>P/S</td><td>I</td><td>Serial or parallel interface selection terminal.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>$CS_1B$,<br>$CS_2$</td><td>A0</td><td>$D_0$ to $D_7$</td><td>RDB,<br>WRB</td><td>-</td></tr>
<tr><td>“L”</td><td>$CS_1B$,<br>$CS_2$</td><td>A0</td><td>$SI(D_7)$</td><td>-</td><td>$SCL(D_6)$</td></tr>
</table>
RAM data and status read operation do not work in mode of the serial interface.<br>In case of the serial interface (P/S="L"),RDB and WRB must be fixed "$V_{DD}$" or " $V_{SS}$", and $D_0$ to $D_5$ are high impedance.</td></tr>
<tr><td>80</td><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.<br>CLS=”H” : Internal oscillator circuit is enable<br>CLS=”L” : Internal oscillator circuit is disabled (requires external input)<br>When CLS=”L”, input the display clock through the CL terminal.</td></tr>
<tr><td>16</td><td>CL</td><td>I/O</td><td>Display clock input/output terminal.<br>The following is true depending on the CLS status.
<table>
<tr><td>CLS</td><td>“H”</td><td>“L”</td></tr>
<tr><td>CL</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>117~99<br>266 to 284</td><td>$C_0$ to $C_{18}$<br>$C_{19}$ to $C_{37}$</td><td>O<br>O</td><td rowspan="2">LCD driving signal output terminals.<br>● Common output terminals :$C_0$ to $C_{37}$<br>● Segment output terminals :$S_0$ to $S_{131}$<br>• Common output terminal<br>The following output voltages are selected by the combination of FR and status of common.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>$V_5$</td></tr>
<tr><td>L</td><td>$V_{DD}$</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>$V_1$</td></tr>
<tr><td>L</td><td>$V_4$</td></tr>
<tr><td>Power Save</td><td></td><td>$V_{DD}$</td></tr>
</table>
• Segment output terminal<br>The following output voltages are selected by the combination of FR and data in the RAM.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>$V_{DD}$</td><td>$V_2$</td></tr>
<tr><td>L</td><td>$V_5$</td><td>$V_3$</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>$V_2$</td><td>$V_{DD}$</td></tr>
<tr><td>L</td><td>$V_3$</td><td>$V_5$</td></tr>
<tr><td>Power Save</td><td></td><td colspan="2">$V_{DD}$</td></tr>
</table>
</td></tr>
<tr><td>126 to 257</td><td>$S_0$ to $S_{131}$</td><td>O</td></tr>
<tr><td>118<br>285</td><td>COMS</td><td>O</td><td>COM output terminals for the indicator. Both terminals output the same signal.<br>Leave these open if they are not used.</td></tr>
<tr><td>78</td><td>TEST</td><td>I</td><td>Maker testing terminal. Used for maker test (No connections )</td></tr>
</table>

## ■ Functional description

(1) Block circuits description

(1-1) Busy Flag (BF)

During internal operation, the LSI is being busy and can't accept any instructions except "status read". The BF data is output through $D_7$ terminal by the "status read" instruction.

When the cycle time (tcyc) mentioned in the "AC characteristics" is satisfied, the BF check isn't required after each instruction, so that MPU processing performance can be improved.

(1-2) Initial display line register

The initial display line register assigns a DDRAM line address, which corresponds, to $COM_0$ by "initial display line set" instruction. It is used for not only normal display but also vertical display scrolling and page switching without changing the contents of the DDRAM.

However, the $39^{th}$ address for icon display can't be assigned for initial display line address.

(1-3) Line counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of frame timing signal (FR), and also counts-up in synchronization with common timing signal.

(1-4) Column address counter

The column address counter is an 8-bit preset counter, which provides a DDRAM column address, and it is independent of below-mentioned page address register.

It will increment (+1) the column address whenever "display data read" or "display data write" instructions are issued. However, the counter will be locked when no-existing address above (84)H are addressed. The count-lock will be able to be released by the "column address set" instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of "ADC set" instruction.

(1-5) Page address register

The page address register provides a DDRAM page address.

The page address "1 to 3" should be used the $D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$ , $D_6$, $D_7$ are valid.

The page address "4" should be used the only $D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$ are valid.

The last page address "5" should be used for icon display because the only $D_0$ is valid.

(1-6) Display data RAM (DDRAM)

The DDRAM contains 5,148-bit, and stores display data, which are 1-to-1 correspondents to LCD panel pixels.

When normal display mode, the display data "1" turns on and "0" turns off LCD pixels. When inverse display mode, "1" turns off and "0" turns on.

| Page Address ($D_2$,$D_1$,$D_0$) | Data | Display Pattern | Line Address | Common Driver |
|---|---|---|---|---|
| 0, 0, 0 | $D_0$ | Page 0 | 00 | $C_0$ |
| | $D_1$ | | 01 | $C_1$ |
| | $D_2$ | | 02 | $C_2$ |
| | $D_3$ | | 03 | $C_3$ |
| | $D_4$ | | 04 | $C_4$ |
| | $D_5$ | | 05 | $C_5$ |
| | $D_6$ | | 06 | $C_6$ |
| | $D_7$ | | 07 | $C_7$ |
| 0, 0, 1 | $D_0$ | Page 1 | 08 | $C_8$ |
| | $D_1$ | | 09 | $C_9$ |
| | $D_2$ | | 0A | $C_{10}$ |
| | $D_3$ | | 0B | $C_{11}$ |
| | $D_4$ | | 0C | $C_{12}$ |
| | $D_5$ | | 0D | $C_{13}$ |
| | $D_6$ | | 0E | $C_{14}$ |
| | $D_7$ | | 0F | $C_{15}$ |
| 0, 1, 0 | $D_0$ | Page 2 | 10 | $C_{16}$ |
| | $D_1$ | | 11 | $C_{17}$ |
| | $D_2$ | | 12 | $C_{18}$ |
| | $D_3$ | | 13 | $C_{19}$ |
| | $D_4$ | | 14 | $C_{20}$ |
| | $D_5$ | | 15 | $C_{21}$ |
| | $D_6$ | | 16 | $C_{22}$ |
| | $D_7$ | | 17 | $C_{23}$ |
| 0, 1, 1 | $D_0$ | Page 3 | 18 | $C_{24}$ |
| | $D_1$ | | 19 | $C_{25}$ |
| | $D_2$ | | 1A | $C_{26}$ |
| | $D_3$ | | 1B | $C_{27}$ |
| | $D_4$ | | 1C | $C_{28}$ |
| | $D_5$ | | 1D | $C_{29}$ |
| | $D_6$ | | 1E | $C_{30}$ |
| | $D_7$ | | 1F | $C_{31}$ |
| 1, 0, 0 | $D_0$ | Page 4 | 20 | $C_{32}$ |
| | $D_1$ | | 21 | $C_{33}$ |
| | $D_2$ | | 22 | $C_{34}$ |
| | $D_3$ | | 23 | $C_{35}$ |
| | $D_4$ | | 24 | $C_{36}$ |
| | $D_5$ | | 25 | $C_{37}$ |
| 1, 0, 1 | $D_0$ | Page 5 | | COMM* |

| Column Address(ADC) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $D_0$=0 | 00 | 01 | 02 | 03 | 04 | 05 | ••••••••••••▶ | 82 | 83 |
| | $D_0$=1 | 83 | 82 | 81 | 80 | 7F | 7E | ◀•••••••••••• | 01 | 00 |

| Segment Drivers | $S_0$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | •••••••••••••••• | $S_{130}$ | $S_{131}$ |
|---|---|---|---|---|---|---|---|---|---|

*: COMM is independent of the “Initial display line set” instruction and always corresponds to the 39th line.

**Fig.1 Display data RAM (DDRAM) Map**

(1-7) Common direction register

The common direction register specifies common driver's scanning direction.

**Table 1.**

| | | Common Drivers | | | |
|---|---|---|---|---|---|
| | PAD No. | 117 | 99 | 284 | 266 |
| | Pin name | $C_0$ | $C_{18}$ | $C_{37}$ | $C_{19}$ |
| Common direction select($D_3$) | "L" | $COM_0 \longrightarrow COM_{18}$ | | $COM_{37} \longleftarrow COM_{19}$ | |
| | "H" | $COM_{37} \longleftarrow COM_{19}$ | | $COM_0 \longrightarrow COM_{18}$ | |

The duty ratio setting and output assignment register are so controlled to operate independently that duty ratio setting required to corresponding duty ratio for output assignment.

(1-8) Reset Circuit

The reset circuit initializes the LSI to the following status by using of the reset signal into the RESB terminal.

- Reset status using the RES terminal:
  1. Display off
  2. Normal Display (Non-inverse display)
  3. ADC select : Normal mode ($D_0$=0)
  4. Power control register clear : $D_2$, $D_1$, $D_0$="0, 0, 0"
  5. Serial interface register clear
  6. LCD bias select : $D_0$="0"(1/6 bias)
  7. Entire display off : $D_0$="0" (Normal mode)
  8. Read modify write off
  9. Initial display line address : $00_H$
  10. Column address : $00_H$
  11. Page address : 0 page
  12. Common direction register : Normal mode ($D_3$=0)
  13. $V_5$ level is adjusted by external bleeder resistance : $D_2$, $D_1$, $D_0$="1, 0, 0"
  14. EVR mode off and EVR register : $D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$="1, 0, 0, 0, 0, 0"

The RESB terminal should be connected to MPU's reset terminal, and the reset operation should be executed at the same timing of the MPU reset.

As described in the **"DC characteristics"**, it is necessary to input 10us(min.) or over "L" level signal into the RESB terminal in order to carry out the reset operation. The LSI will return to normal operation after about 1.0us(max.) from the rising edge of the rest signal.

In case of using external power supply for LCD driving voltage, the RESB terminal is required to be being "L" level when the external power supply is turned-on.

The "Reset" instruction in Table.4 can't be substituted for the reset operation by using of the RESB terminal. It executes above-mentioned only 8 to 14 items.

LCD driving circuits

(a) Common and segment drivers

LCD drivers consist of 38-common drivers, 132-segment divers and 1-icon-common driver.

As shown in “LCD driving waveform”, LCD driving waveforms are generated by the combination of display data, common timing signal and internal FR timing signal.

(b) Display data latch circuit

The display data latch circuit temporally stores 132-bit display data transferred from the DDRAM in the synchronization with the common timing signal, and then it transfers these stored data to the segment drivers.

“Display on/off”, “inverse display on/off” and “entire display on/off” instructions control only the contents of this latch circuit, they can’t change the contents of the DDRAM.

In addition, the LCD display isn’t affected by the DDRAM accesses during its displaying because the data read-out timing from this latch circuit to the segment drivers is independent of accessing timing to the DDRAM.

(c) Line counter and latch signal or latch Circuits

The clock line counter and latch signal to the latch circuits are generated from the internal display clock (CL). The line address of display data RAM is renewed synchronizing with display clock (CL).

132bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display timing generator

The display timing generates the timing signal for the display system bay combination of the master clock CL and driving signal FR ( refer to Fig.2 ) The frame signal FR and LCD alternative signal generate LCD driving waveform on the two frame alternative driving method.

(e) Common timing generation

The common timing is generated by display clock CL (refer to Fig.2)

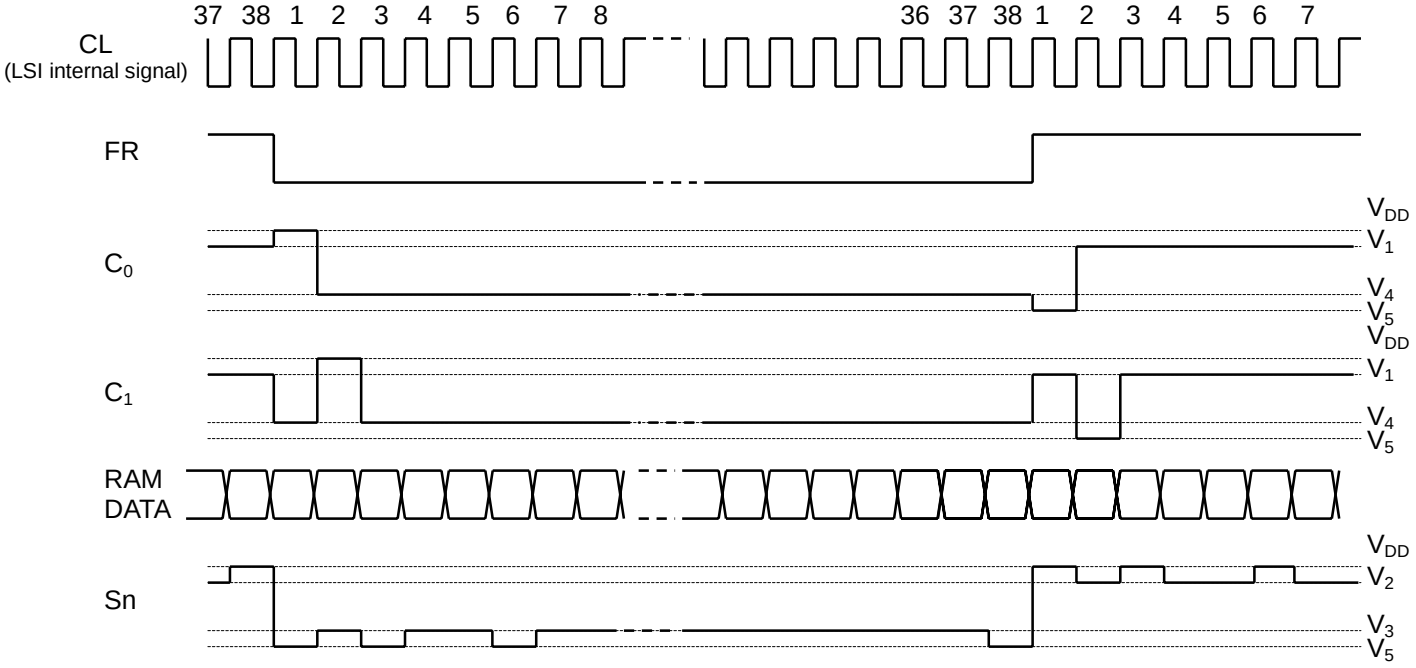



**Fig.2 Waveform of Display Timing**

(f) Oscillator

This is the low power consumption CR oscillator which provides the display clock and voltage converter timing clock. Either external or internal Oscillator can be selected by setting the CLS terminal to “L” or “H” as shown in below.

CLS=”L” : External Oscillator
CLS=”H” : Internal Oscillator

When the internal oscillator is used, the CL terminal fixed to “H” or “L”.
When the external oscillator is used, the CL terminal into display clock.

(g) Internal power circuits

The internal power circuits are composed of x4 boost voltage converter, output voltage regulator including 64-step EVR and voltage followers.

The optimum values of the external passive components for the internal power circuits, such as capacitors for $V_1$ to $V_5$ terminals and feed back resistors for VR terminal, depend on LCD panel size. Therefore, it is necessary to evaluate the actual LCD module with these external components in order to determine the optimum values.

Each portion of the internal power circuits is controlled by “power control set” instruction as shown in Table.2. In addition, the combination of power supply circuits is described in Table.3.

**Table.2 Power control set**

| Bits | Portions | Status | |
|---|---|---|---|
| $D_2$ | Voltage converter | 1 :On | 0: Off |
| $D_1$ | Voltage regulator | 1 :On | 0: Off |
| $D_0$ | Voltage followers | 1 :On | 0: Off |

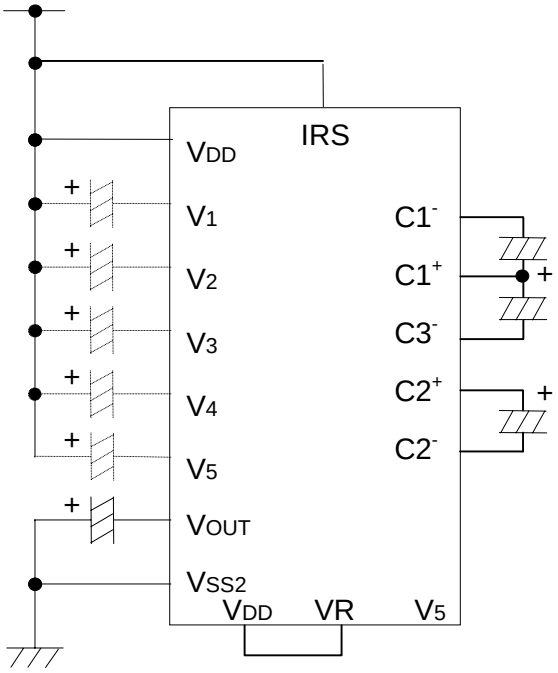
**Table.3 Power supply combinations**

| Status | $D_2$ | $D_1$ | $D_0$ | Voltage converter | Voltage regulator | Voltage followers | External voltage | Capacitor terminals |
|---|---|---|---|---|---|---|---|---|
| Using all internal power circuits | 1 | 1 | 1 | On | On | On | $V_{SS2}$ | Use |
| Using voltage regulator and Voltage followers | 0 | 1 | 1 | Off | On | On | $V_{OUT}$, $V_{SS2}$ | Open |
| Using voltage followers | 0 | 0 | 1 | Off | Off | On | $V_{OUT}$, $V_5$, $V_{SS2}$ | Open |
| Using only external power supply | 0 | 0 | 0 | Off | Off | Off | $V_{OUT}$, $V_1$ to $V_5$ | Open |

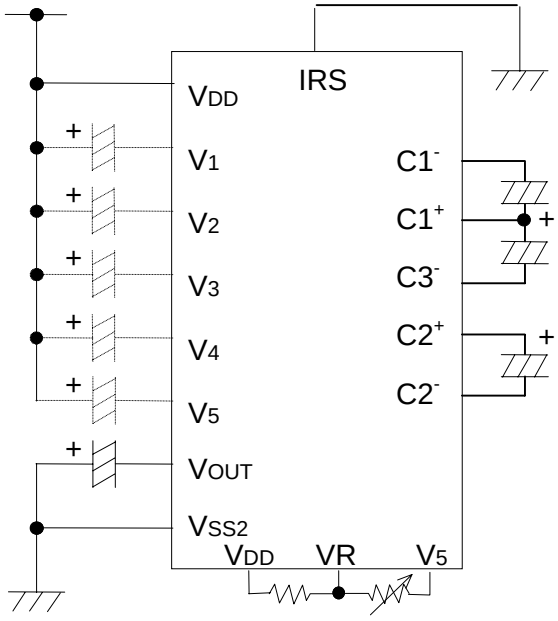
Note1) Capacitor input terminals: C1+, C1-, C2+, C2-, C3-
Note2) Do not use other combinations except examples in Table.3.
Note3) Connect decoupling capacitors on $V_1$ to $V_5$ terminals whenever using the voltage followers.

- Power Supply applications
  Power Control Instruction
  $D_2$ : Boost Circuit
  $D_1$ : Voltage Regulator
  $D_0$ : Voltage Follower

(1) Internal power supply Example.
$V_5$ level is adjusted by internal bleeder resistance (IRS="H")
All of the Internal Booster, Voltage Regulator, Voltage Follower using. ($D_2$,$D_1$,$D_0$) = (1,1,1)

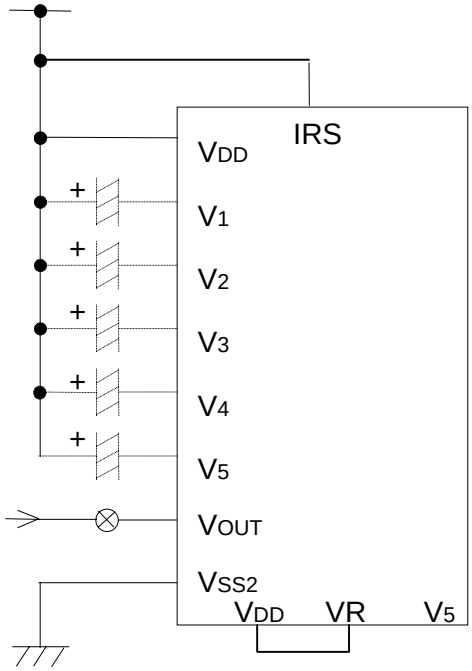



(2) Internal power supply Example.
$V_5$ level is adjusted by internal bleeder resistance (IRS="L")
All of the Internal Booster, Voltage Regulator, Voltage Follower using. ($D_2$,$D_1$,$D_0$) = (1,1,1)

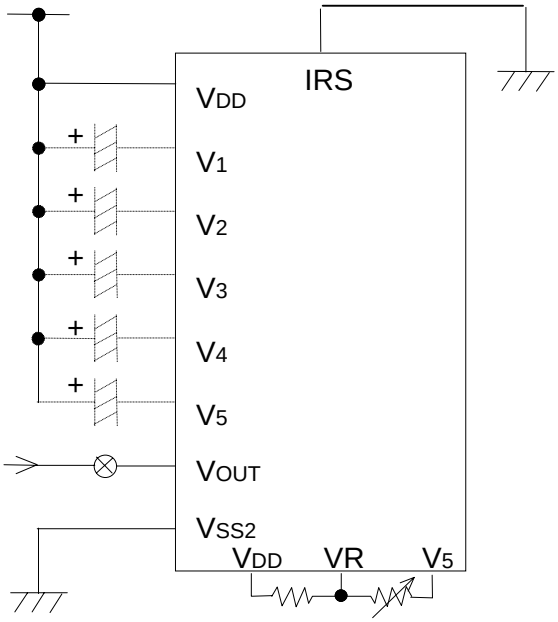



* ⊗ :Bias capacitors are selected depending on the LCD panel.
The evaluation in various display patterns should be experimented in the application.

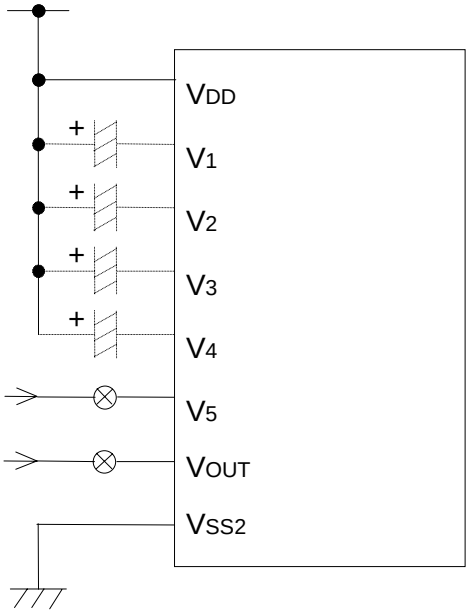
(3) Only $V_{OUT}$ Supply from outside Example.
$V_5$ level is adjusted by internal bleeder resistance (IRS="H")
Internal Voltage Regulator,
Voltage Follower using.
$(D_2,D_1,D_0)$ = (0,1,1)



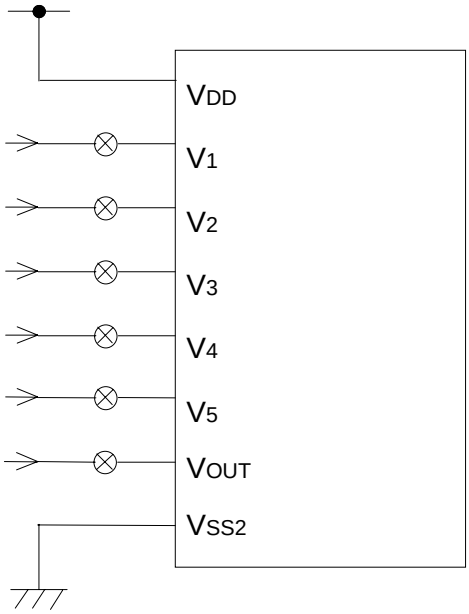

(4) Only $V_{OUT}$ Supply from outside Example.
$V_5$ level is adjusted by internal bleeder resistance (IRS="L")
Internal Voltage Regulator,
Voltage Follower using.
$(D_2,D_1,D_0)$ = (0,1,1)




(5) $V_{OUT}$ and $V_5$ Supply from outside Example.
Internal Voltage Follower using.
$(D_2,D_1,D_0)$ = (0,0,1)




(6) External Power Supply Example.
All of $V_1$ to $V_5$ and $V_{OUT}$ supply from outside
$(D_2,D_1,D_0)$ = (0,0,0)




⊗ : These switches should be open during the power save mode.
⊗ : *Bias capacitors are selected depending on the LCD panel.
The evaluation in various display patterns should be experimented in the application.

## ■ INSTRUCTION SET

The **NJU6674** distinguishes the data on the data bus $D_7$ to $D_0$ as an instruction by combination of A0, RDB(E), WRB(R/W) signals. The decoding of the instruction and execution performs with only high speed internal timing without relation to the external clock. Therefore, no busy flag check required normally. In case of the serial interface, the data input as MSB($D_7$) first serially. Table.4 shows the instruction codes of the NJU6674.

**Table.4 Instruction table**

| Instruction | | Instruction Code | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| (a) | Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | LCD Display ON/OFF<br>$D_0$=0:OFF $D_0$=1:ON |
| (b) | Initial display Line set | 0 | 1 | 0 | 0 | 1 | Start address | | | | | | Determine the Display Line of RAM to COM $_0$ |
| (c) | Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | * | Page Address | | | Set the page of DD RAM to the Page Address Register |
| (d) | Column address set (Upper 4-bit) | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Higher Order Culomn Address | | | | Set the Higher order 4 bits Column Address to the Reg. |
| | Column address set (Lower 4-bit) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Lower Order Culomn Address | | | | Set the Lower order 4 bits Column Address to the Reg. |
| (e) | Status read | 0 | 0(1) | 1 | Status | | | | 0 | 0 | 0 | 0 | Read out the internal Status |
| (f) | Display data write | 1 | 1 | 0 | Write Data | | | | | | | | Write the data into the Display Data RAM |
| (g) | Display data read | 1 | 0 | 1 | Read Data | | | | | | | | Read the data from the Display Data RAM |
| (h) | ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | Set the DD RAM vs Segment<br>$D_0$=0:Normal $D_0$=1:Inverse |
| (i) | Inverse display On/Off | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0/1 | Inverse the ON and OFF Display<br>$D_0$=0:Normal $D_0$=1:Inverse |
| (j) | Entire display On/Off | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | Whole Display Turns ON<br>$D_0$=0:Normal $D_0$=1: Whole Disp. ON |
| (k) | LCD bias select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0/1 | Set the LCD bias ratio<br>$D_0$=0:1/6 $D_0$=1:1/5 |
| (l) | Read modify write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Increment the Column Address Register when writing but no-change when reading |
| (m) | End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Release from the Read Modify write Mode |
| (n) | Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Initialize the Internal Circuits |
| (o) | Common direction select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0/1 | * | * | * | Select common direction<br>$D_3$=0:Normal $D_3$=1:Inverse |
| (p) | Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | $D_2$ | $D_1$ | $D_0$ | Set the status of internal power Circuits |
| (q) | Internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | $D_2$ | $D_1$ | $D_0$ | Set the status of internal resistor ratio (Ra/Rb) |
| (r) | EVR mode set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set EVR mode |
| (s) | EVR register set | 0 | 1 | 0 | * | * | Setting Data | | | | | | Set EVR register |
| (t) | Pawer save mode On/Off | 0<br>0 | 1<br>1 | 0<br>0 | 1<br>1 | 0<br>0 | 1<br>1 | 0<br>0 | 1<br>0 | 1<br>1 | 1<br>0 | 0<br>1 | Set the Power Save Mode (LCD Display OFF) |
| (u) | NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | |
| (v) | Reserve (Inhibited) | 0<br>0 | 1<br>1 | 0<br>0 | 1<br>* | 0<br>* | 1<br>* | 0<br>* | 1<br>* | 1<br>* | 0<br>* | 0<br>* | Inhibited command |
| (w) | Test | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | Inhibited command |

(*Don't Care)

(2) Instruction description

(a) Display On/Off

The “Display ON/OFF” instruction is used to control the display ON or OFF without changing the display data in the DDRAM.

All of the COM terminals at the time of “Display OFF” and SEG terminals are set to $V_{DD}$ level.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

D 0: Display Off
1: Display On

(b) Initial display line set

This instruction specifies the DDRAM line address which corresponds to the $COM_0$ position.

By means of repeating this instruction, the initial display line address will be dynamically changed; it means smooth display scrolling will be enabled.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

| $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Line address (HEX) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| : | : | : | : | : | : | : |
| : | : | : | : | : | : | : |
| 1 | 0 | 0 | 1 | 0 | 1 | 25 |

(c) Page address set

In order to access to the DDRAM for writing or reading display data, both “page address set” and “column address set” instructions are required before accessing.

The last page address “5” should be used for icon display because the only $D_0$ is valid.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | * | $A_2$ | $A_1$ | $A_0$ |

(*: Don’t Care)

| $A_2$ | $A_1$ | $A_0$ | Page |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |

(d) Column address set

As above-mentioned, in order to access to the DDRAM for writing or reading display data, it is necessary to execute both “page address set” and “column address set” before accessing. The 8-bit column address data will be valid when both upper 4-bit and lower 4-bit data are set into the column address register.

Once the column address is set, it will automatically increment (+1) whenever the DDRAM will be accessed, so that the DDRAM will be able to be continuously accessed without “column address set” instruction.

The column address will stop increment and the page address will not be changed when the last address (83)H is addressed.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | $A_7$ | $A_6$ | $A_5$ | $A_4$ | Upper 4-bit |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Lower 4-bit |

| $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Column address (HEX) |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| : | : | : | : | : | : | : | : | : |
| : | : | : | : | : | : | : | : | : |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 |

(e) Status read

This instruction reads out the internal status regarding “busy flag”, “ADC select”, “display on/off” and “reset”.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | BUSY | ADC | ON/OFF | RESET | 0 | 0 | 0 | 0 |

BUSY: When $D_7$ is “1”, the LSI is being busy and can’t accept any instructions.

ADC: It shows the correspondence between the column address and segment drivers.
When $D_6$ is “0”, the column address (131-n) corresponds to segment driver n.
When $D_6$ is “1”, the column address (n) corresponds to segment driver n.
Please be careful that read out data is opposite of “ADC select” instruction data.

ON/OFF: It shows display on or off status.
When $D_5$ is “0”, the LSI is in display-on status.
When $D_5$ is “1”, the LSI is in display-off status.
Please be careful that read out data is opposite of “Display On/Off” instruction data.

RESET: It shows reset status.
When $D_4$ is “0”, the LSI is in normal operation.
When $D_4$ is “1”, the LSI is during reset operation.

(f) Display data write

This instruction writes display data into the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is written by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | Write Data | | | | | | | |

(g) Display data read

This instruction reads out the display data stored in the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is read out by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

After the ”column address set” instruction, a dummy read will be required, please refer to the (4-5).

In case of using serial interface mode, this instruction can’t be used.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | Read Data | | | | | | | |

(h) ADC select

This instruction selects segment driver direction.

The correspondence between the column address and segment driver direction is shown in Fig.1.

Segment Driver Output order is inverse, when this instruction executes, therefore, the placement NJU6674 against the LCD panel becomes easy.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D |

D 0: Clokwise Output(Normal)
1: Counterclockwise Output(Inverse)

(i) Inverse display On/Off

This instruction inverses the status of turn-on or turn-off of entire LCD pixels. It doesn’t change the contents of the DDRAM.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D |

D 0: Normal RAM data “1” correspond to “On”
1: Inverse RAM data “0” correspond to “On”

(j) Entire display On/Off

This instruction turns on entire LCD pixels regardless the contents of the DDRAM. It doesn’t change the contents of DDRAM. This instruction executed prior to the “Normal or Inverse display On/Off Set” Instruction.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

D 0: Normal Display
1: Whole Display turns On

When the “Entire display On” instruction is executed at Display Off states, the NJU6674 operates in Power Save Mode. (Refer “Power Save Mode”)

(k) LCD bias set

This instruction selects LCD bias value.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D |

D 0: 1/6 bias
1: 1/5 bias

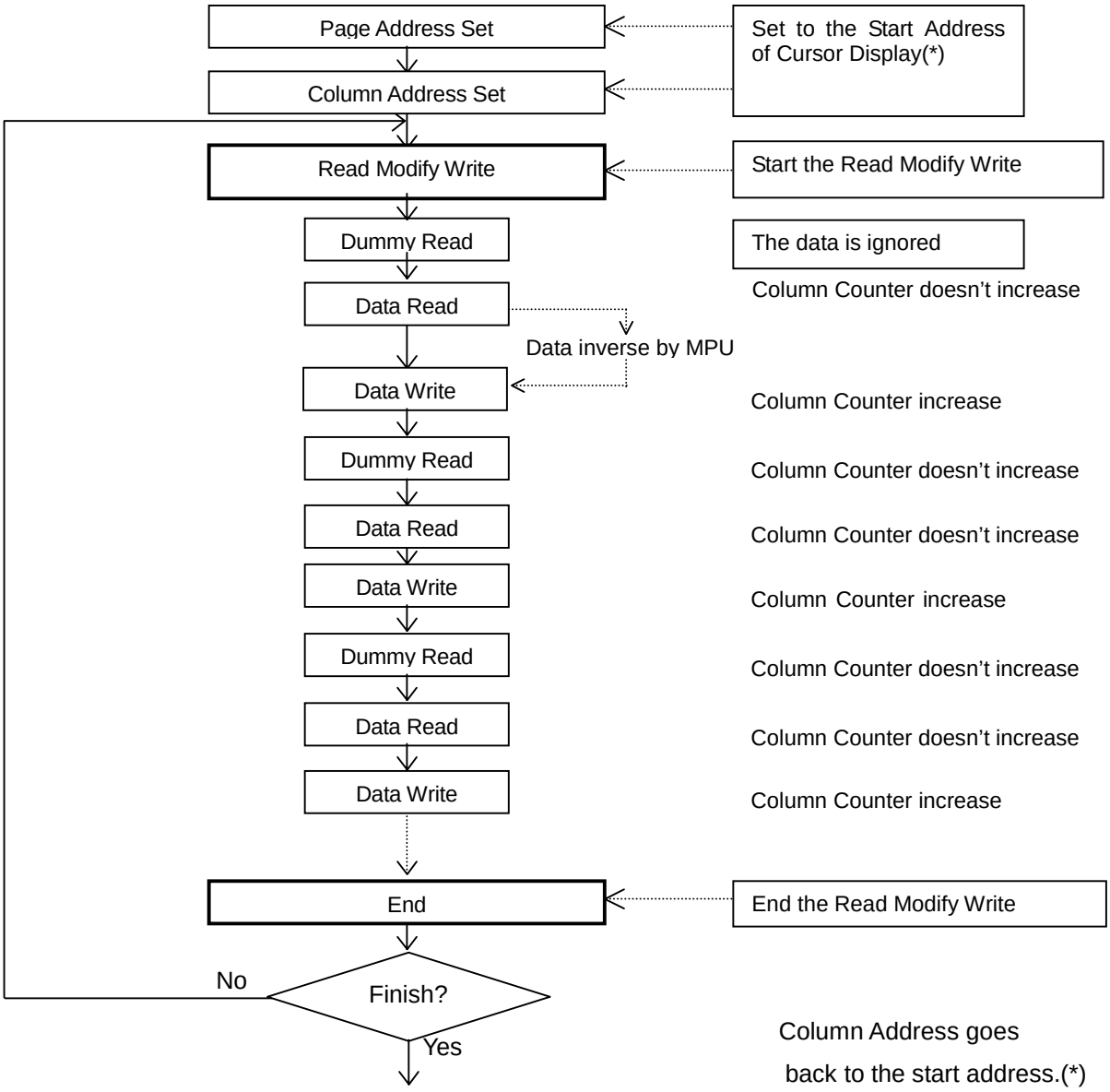
(l) Read modify write

This instruction sets the Read Modify Write controlling the Column Address increment. In this mode, Column Address only increments when execute the display data “Write” instruction; but no change when the display data “Read” Instruction. This states is continued until the End instruction(m) execution. When the End instruction is executed, the Column Address goes back to the start address before the execution of this “Read Modify Write” instruction. This function reduces the load of MPU for repeating display data change of the fixed area.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

*) In this “Read Modify Write” mode, out of display data “Read”/”Write”, any instructions except “Column Address Set” can be executed.

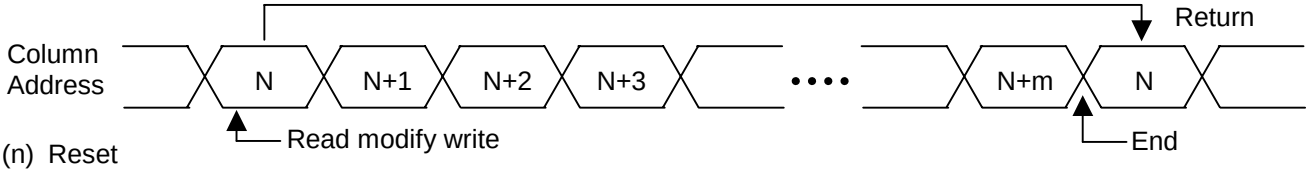
- The sequence of cursor blink display



(m) End

The “end” instruction cancels the read modify write mode and makes the column address return to the initial value just before “read modify write” is started.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |




(n) Reset

This instruction reset the LSI to the following status, however it doesn’t change the contents of the DDRAM. Please be careful that it can’t be substituted for the reset operation by using of the RESB terminal.

Reset status by “reset” instruction:

1: Read modify write off
2: Initial display line address : $(00)_H$
3: Column address : $(00)_H$
4: Page address : (0) page
5: Common direction register : Normal mode ($D_3$=”0”)
6: $V_5$ level is adjusted by external bleeder resistance ($D_2$, $D_1$, $D_0$=”1, 0, 0”)
7: EVR register : ($D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$=”1, 0, 0, 0, 0, 0”)

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

(o) Common driver direction select

This instruction selects common driver direction.
Please refer to (1-7) common driver direction for more detail.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | $D_3$ | * | * | * |

(*: Don’t Care)

$D_3$ 0: Normal ($C_0 \rightarrow C_{37}$)
1: Inverse ($C_{37} \rightarrow C_0$)

(p) Power control set

This instruction controls the status of internal power circuits. Please refer to the (1-9) LCD Driving Circuits (g) internal power circuits for more detail.

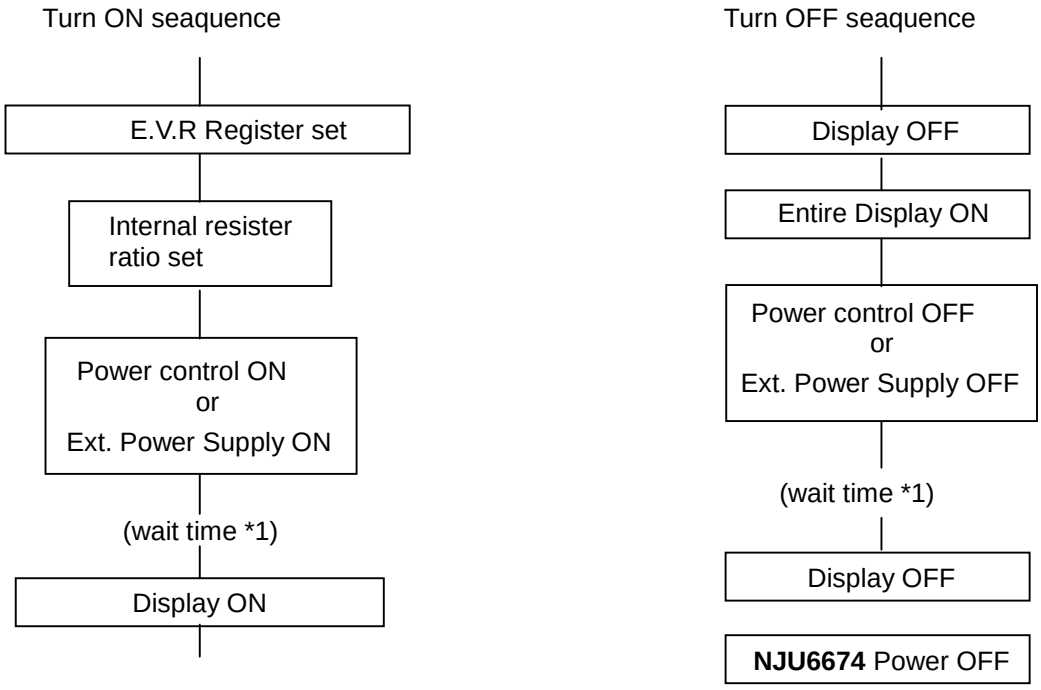
| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | $D_2$ | $D_1$ | $D_0$ |

$D_2$ 0: Voltage converter off
1: Voltage converter on
$D_1$ 0: Voltage regulator off
1: Voltage regulator on
$D_0$ 0: Voltage followers off
1: Voltage followers on

Note) The internal power supply must be Off when external power supply using.

* The wait time depends on the $C_4$ to $C_8$, $C_{OUT}$ capacitors, and $V_{DD}$ and $V_5$ Voltage.
Therefore it requires the actual evaluation using the LCD module to get the correct time.

- LCD Driving power supply ON/OFF sequences.
The sequences below are required when the power supply turns ON/OFF. For the power supply turning on operation after the power-save mode(p), refer the “power save release” mentioned after.




(∗1) The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to $V_1$ to $V_5$. To know the rise time correctly, test by using the actual LCD module. refer to (3-5) “LCD Driving Voltage Generation Circuits”.

(q) Internal resistor ratio set

The “Internal resistor ratio set” instruction is used to determine the internal resistor ratio for the voltage regulator.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | $A_2$ | $A_1$ | $A_0$ |

| $D_2$ | $D_1$ | $D_0$ | Internal resistor ratio(1+Rb/Ra) | Internal resistor ratio(1+Rb/Ra) |
|---|---|---|---|---|
| 0 | 0 | 0 | 3.0 | Minimum |
| 0 | 0 | 1 | 3.5 | : |
| 0 | 1 | 0 | 4.0 | : |
| 0 | 1 | 1 | 4.5 | : |
| 1 | 0 | 0 | 5.0 | : |
| 1 | 0 | 1 | 5.5 | : |
| 1 | 1 | 0 | 6.0 | : |
| 1 | 1 | 1 | 6.4 | Maximum |

(r),(s) EVR set

(r) EVR mode set

This instruction sets the LSI into the EVR mode, and it is always used by the combination with “EVR register set”.

The LSI can’t accept any instructions except the “EVR register set” during the EVR set mode. This mode will be released after the “EVR register set” instruction.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

(s) EVR register set

This instruction sets 6-bit data into the EVR register to determine the output voltage “$V_5$” of the internal voltage regulator.

| A0 | RDB | WRB | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | * | * | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |

(*: Don’t Care)

| $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $V_5$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Minimum |
| 0 | 0 | 0 | 0 | 0 | 1 | : |
| : | : | : | : | : | : | : |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | Maximum |

When EVR doesn’t use, set the EVR register to $D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$ = ”1, 0, 0, 0, 0, 0”.

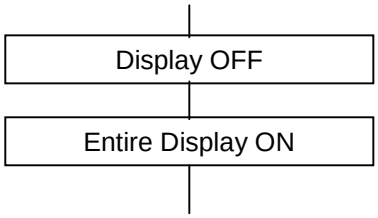
(t) Power Save(complex command)

When Entire Display ON at the Display OFF states(inverse order also same), the internal cirsuits goes to the Power Save Mode and the operating curent is dramatically reduced, almost same as the standby current. The internal states in the Power Save Mode is shown as follows;

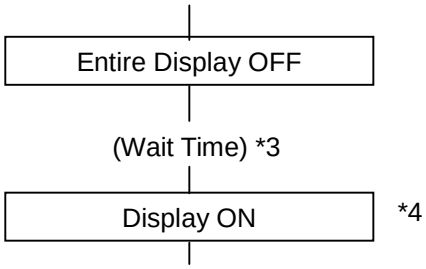
1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drives output $V_{DD}$ level Voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage($V_1$ to $V_5$) is fixed to the $V_{DD}$ level.

The power save and its release perform according to the following sequences.

Power Save Sequence *1




Power Save Releace Sequence *2




*1: In the Power save sequence, the Power Save Mode starts after the Entire Display ON command is executed.
*2: In the Power save Release sequence, Power Save Mode releases just after the Entire Display OFF instruction. The Display ON instruction is allowed to execute at any time after the Entire Display OFF instruction is completed.
*3: The Internal Power Supply rise time depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capactor of Booster, and External Capacitor connected to $V_1$ to $V_5$. To Know the rise time correctly, test by using the actual LCDmodule.
*4: LCD Driving waveform is output after the exection of the Display ON instruction execution.
*5: In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the $V_{DD}$ for fixing the voltage. In this time, $V_{OUT}$ terminal also shold be made condition like as connection to $V_{SS}$.

(u) NOP

This instruction is Non Operation Instruction.

(v) Reserve, (w) Test

This instruction is used only for manufacturer's tests. (Don't Inhibited command)

(3) Internal Power Supply

(3-1) Voltage converter

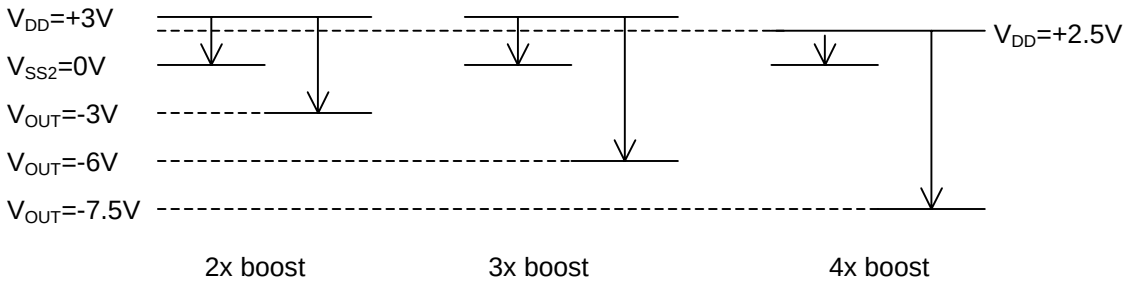
The voltage converter generates maximum 4x boosted negative-voltage from the voltage between $V_{DD}$ and $V_{SS2}$. The boosted voltage is output from the $V_{OUT}$ terminal.

The internal oscillator is required to be operating when using this converter, because the divided signal provided from the oscillator is used for the internal timing of this circuit.

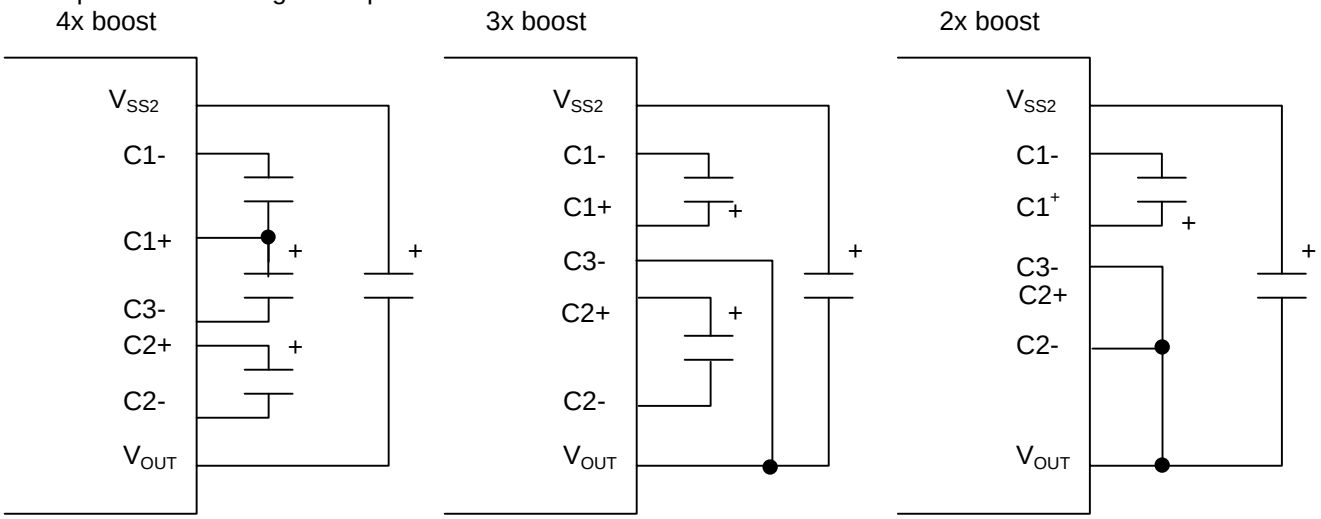
The boosted voltage between $V_{DD}$ and $V_{OUT}$ must not exceed 10.0V.

The voltage converter requires external capacitors for boosting as shown in below.

- The boosted voltage and $V_{DD}$, $V_{SS2}$




- Example for connecting the capacitors



(3-2) Contrast Adjustment by the EVR function

The EVR selects the $V_{REG}$ voltage out of following 64 conditions by setting 6-bit data into the EVR register. When the EVR function, $V_{EV}$ (refer:**Fig-3-a Voltage Adjust Circuit**) is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of $V_{EV}$ bay instruction and change the voltage of $V_5$.

A step with EVR is set like table shown below.

| n | EVR register | | $V_{EV}$ [V] | $V_{LCD}$ |
|---|---|---|---|---|
| 63 | $00_H$ | (0,0,0,0,0,0) | $(99/162)V_{REG}$ | Minimum |
| 62 | $01_H$ | (0,0,0,0,0,1) | $(100/162)V_{REG}$ | : |
| 61 | $02_H$ | (0,0,0,0,1,0) | $(101/162)V_{REG}$ | : |
| : | : | : | : | : |
| : | : | : | : | : |
| : | : | : | : | : |
| 2 | $3D_H$ | (1,1,1,1,0,1) | $(160/162)V_{REG}$ | : |
| 1 | $3E_H$ | (1,1,1,1,1,0) | $(161/162)V_{REG}$ | : |
| 0 | $3F_H$ | (1,1,1,1,1,1) | $(162/162)V_{REG}$ | Maximum |

*1: $V_{LCD}=V_{DD}-V_5$

*2 : In use of the EVR function, the voltage adjustment circuit must turn on by the power control instruction.

(3-3) Setting for internal resistor ratio

Either external or internal feedback resistors can be selected by setting the IRS terminal to “0” or”1”.

The Internal resistor ratio selects 8 conditions of the feedback resistor ratio(1+Rb/Ra).The feed back resistor ratio(1+Rb/Ra) changing 3-bit data into the Internal resistor ratio register.

| IRS | Ra, Rb |
|---|---|
| 0 | External resistors |
| 1 | Internal resistors |

Internal resistor ratio register: (Reference)

| $D_2$ | $D_1$ | $D_0$ | (1+Rb/Ra) |
|---|---|---|---|
| 0 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 3.5 |
| 0 | 1 | 0 | 4.0 |
| 0 | 1 | 1 | 4.5 |
| 1 | 0 | 0 | 5.0 |
| 1 | 0 | 1 | 5.5 |
| 1 | 1 | 0 | 6.0 |
| 1 | 1 | 1 | 6.4 |

(3-4) Voltage Adjust Circuit

The boosted voltage of $V_{OUT}$ outputs $V_5$ for $V_{LCD}$ driving through the voltage adjust circuit.
This circuit is composed of high the $V_{RS}$, 64-level EVR and internal feedback resistor.

(a) Using Internal Resistor Ratio function (IRS="1")

The LCD driving volatge $V_5$ is determined in accordance with the setting for the EVR and the internal resistor ratio Instruction.

The output voltage of $V_5$ adjusted by changing with in the $V_5 > V_{OUT}$.

The output voltage is caluculated by the following formula.

$$V_5=(1+Rb/Ra)V_{EV}=(1+(Rb/Ra))(n/162)V_{REG} \qquad (a\text{-}1)$$

$V_{REG}$ : External Constant voltage ($V_{RS}$)
n : EVR value

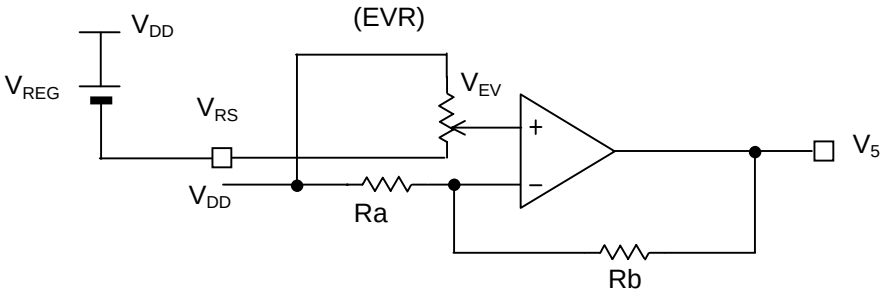



Fig-3-a Voltage Adjust Circuit

(b) Using external Ra and Rb resistors

In case that the external feedback resistors (Ra, Rb) are used by setting the IRS terminal to “0”, these external resistors are required to be placed between the $V_{DD}$ and $V_R$ and between the $V_R$ and $V_5$ terminals. The LCD driving voltage $V_5$ is determined in accordance with the setting for the EVR and the external resistor ratio.

The output voltage of $V_5$ adjusted by changing the Ra and Rb within the $V_5 > V_{OUT}$.

The output voltage is caluculated by the following formula.

$$V_5=(1+(Rb'/Ra'))V_{EV}=(1+(Rb'/Ra'))(1-(n/162))V_{REG} \quad \text{(b-1)}$$

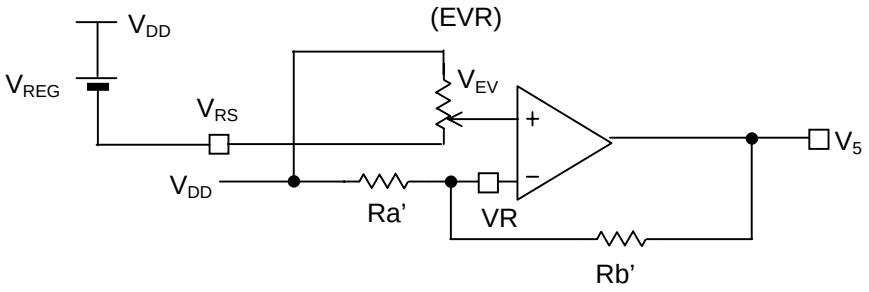



Fig-3-b Voltage Adjust Circuit

< Designe example for R1 and R2 / Reference >

Condition : Ta=25°C, n=31, $V_{REG}$=-2.1V, EVR=1$F_H$ ,

$$V_5=(1+(Rb/Ra))(n/162)V_{REG}$$
$$-7=(1+(Rb'/Ra'))(1-(31/162)\ (-2.1) \quad \text{(b-2)}$$

Determined by the current flown between $V_{DD}$-$V_5$ / 5uA.

$$Ra'+Rb'=1.4M\Omega \quad \text{(b-3)}$$

Ra and Rb caluculated by above conditions and the formula of (b-2, b-3) to mentioned below;

Rb'/Ra'=3.12

Ra=340kΩ

Rb=1060kΩ

The adjustable $V_5$ range and step voltage table shown below.

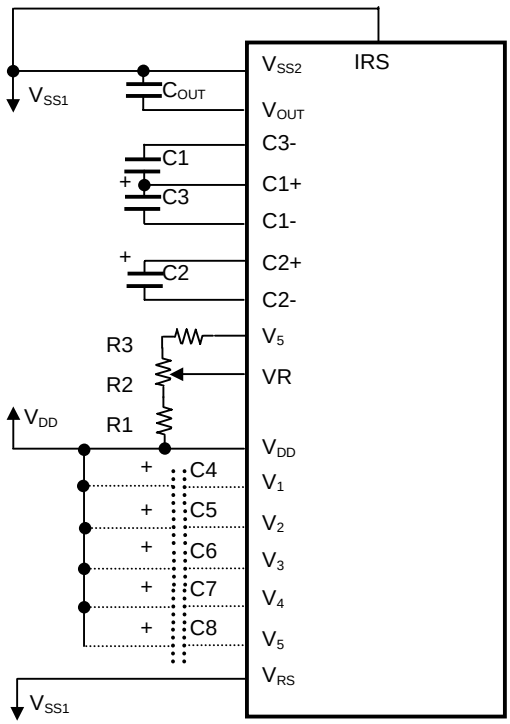
| $V_5$ | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|
| Adjustable Range | -8.6 (63 Step) | -7.0 (32 Step) | -5.3(0 Step) | [V] |
| Step Voltage | | 52 | | [mV] |

(3-5) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of $V_1$,$V_2$,$V_3$,$V_4$ are generated by dividing the $V_5$ voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.

The external capacitors to $V_1$ to $V_5$ for Bias voltage stabilization may be removed in use of small size LCD panel. The equivalent load of LCD panel may be changed depending on display patterns. Therefore, it require display quality check on various display patterns actually without external capacitors. If the display quality is not so good, external capacitors should connects as show in Fig. 4. (If no need external capacitors as result of experiment, the application patterns (wiring) should be prepared for recovery.)

Using the internal Power Supply




Using the external Power Supply

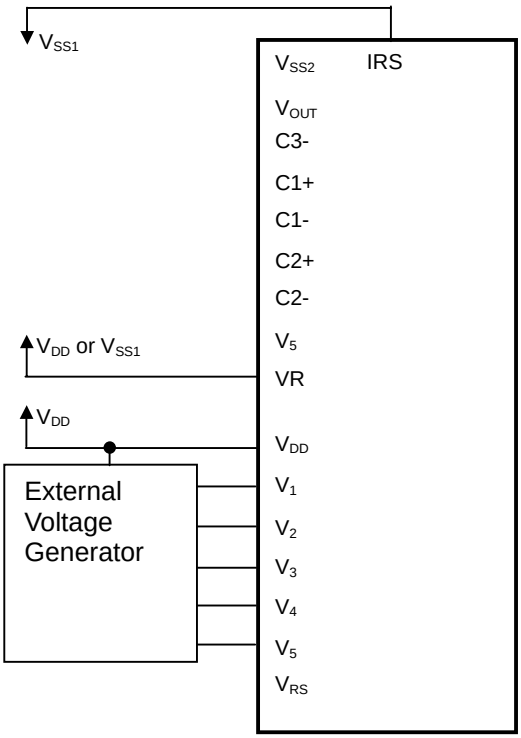



**Fig.4**

Reference set up value $V_{LCD}=V_{DD}-V_5$=5.0 to 9.0V

| | |
|---|---|
| $C_{OUT}$ | ~1.0µF |
| C1, C2, C3 | ~1.0µF |
| C4 to C7 | 0.1 to 0.47 µF |
| $R_1$ | 264kΩ |
| $R_2$ | 211kΩ |
| $R_3$ | 925kΩ |

∗1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

∗2 Following connection of $V_{OUT}$ is required when external power supply using.

When $V_{SS}>V_5$, $V_{OUT}=V_5$

When $V_{SS}\leq V_5$, $V_{OUT}=V_{SS}$

∗3 Bias capacitors are selected depending on the LCD panel. The evaluation in various display patterns should be experimented in the application

(4) MPU Interface

(4-1) Interface type selection

**NJU6674** interfaces with MPU by 8-bit bi-directional data bus ($D_7$ to $D_0$) or serial (SI:$D_7$). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to “H” or “L” level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

**Table 5**

| P/S | I/F type | $CS_1B$ | $CS_2$ | A0 | RDB | WRB | SEL68 | $D_7$ | $D_6$ | $D_5$ - $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| H | Parallel | $CS_1B$ | $CS_2$ | A0 | RDB | WRB | SEL68 | $D_7$ | $D_6$ | $D_5$ - $D_0$ |
| L | Serial | $CS_1B$ | $CS_2$ | A0 | - | - | - | SI | SCL | Hi-Z |

“Hi-Z” mark: Hi-impedance "-" mark: Fix to "H"or "L"

(4-2) Parallel Interface

The **NJU6674** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S=”H” is selected.

The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to “H” or “L” as shown in table 6.

**Table 6**

| SEL68 | Type | $CS_1B$ | $CS_2$ | A0 | RDB | WRB | $D_7$ - $D_0$ |
|---|---|---|---|---|---|---|---|
| H | 68-type MPU | $CS_1B$ | $CS_2$ | A0 | E | R/WB | $D_7$ - $D_0$ |
| L | 80-type MPU | $CS_1B$ | $CS_2$ | A0 | RDB | WRB | $D_7$ - $D_0$ |

(4-3) Discrimination of Data Bus Signal

The **NJU6674** discriminates the mean of signal on the data bus by the combination of A0, E, R/WB, and (RDB, WRB) signals as shown in Table 7.

**Table 7**

| common | 68 type | 80 type | | Function |
|---|---|---|---|---|
| A0 | R/WB | RDB | WRB | |
| H | H | L | H | Read Display Data |
| H | L | H | L | Write Display Data |
| L | H | L | H | Status Read |
| L | L | H | L | Write into the Register(Instruction) |

(4-4) Serial Interface.(P/S="L")

The serial interface of the **NJU6674** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($CS_1B$="L", $CS_2$="H"), the input to $D_7$(SI) and $D_6$(SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.

The data input from the terminal(SI) is MSB first like as the order of $D_7$, $D_6$,------ $D_0$, by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.

It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0="H" and instruction by A0="L" A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.

However,in case of RESB="H" to "L" or $CS_1B$="L" to "H" and $CS_2$="H" to "L" with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.

The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

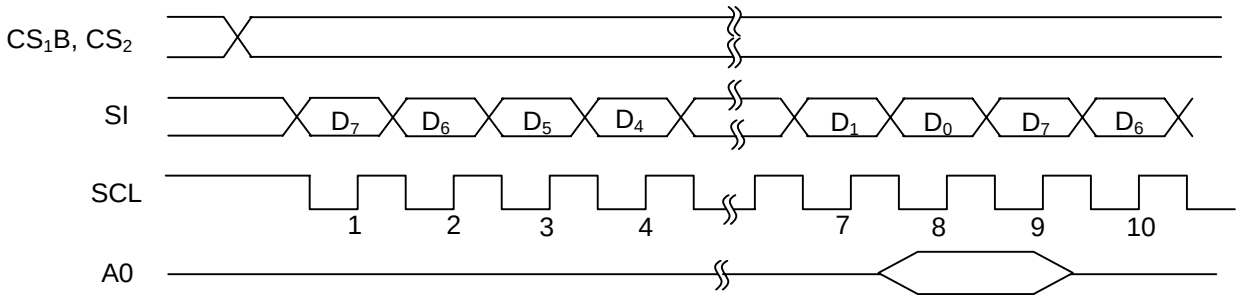



**Fig.5**

(4-5) Access to the Display Data RAM and Internal Register.

The **NJU6674** transfers data to the MPU through the bus holder with the internal data bus.

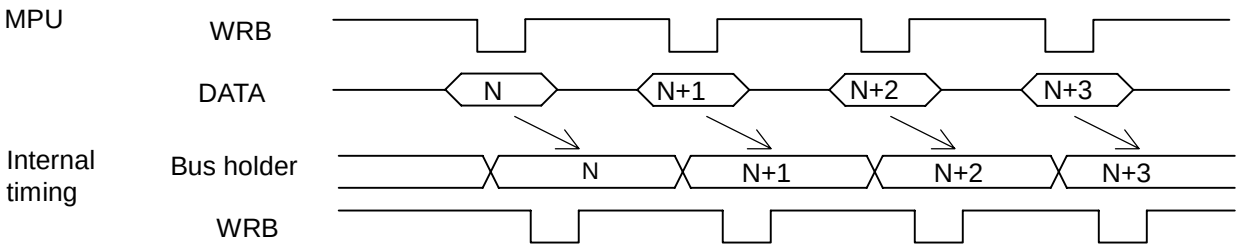
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read ) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6674** from MPU side is not access time ($t_{ACC}$, $t_{DS}$) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the satisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 6)

The example of Read Modify Write operation is mentioned in (3)Instruction -l)The sequence of Inverse Display.

● Write Operation




● Read Operation

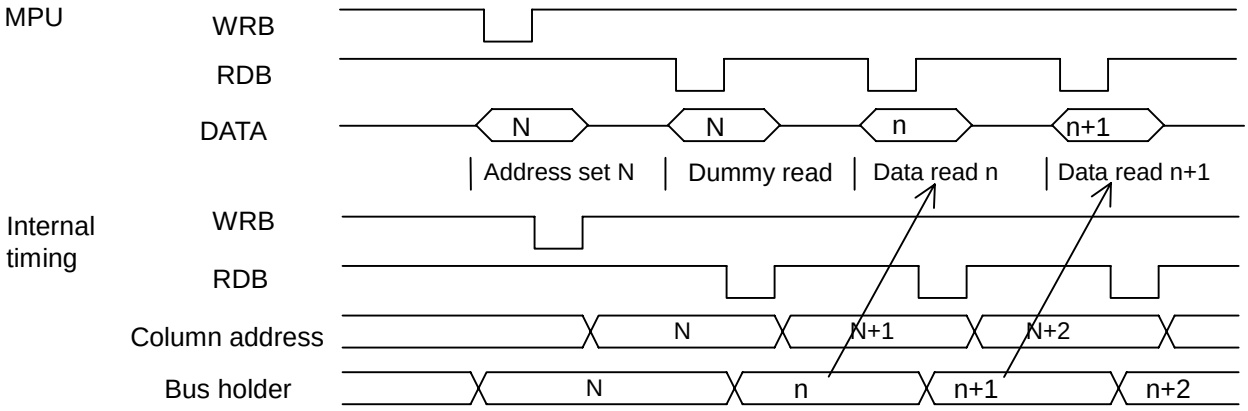


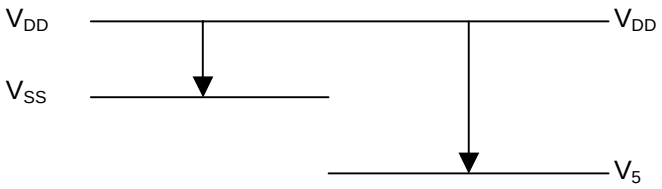

**Fig.6**

(4-6) Chip Select

$CS_1B$, $CS_2$ is Chip Select terminal. In case of $CS_1B$="L" and $CS_2$="H". the interface with MPU is available. In case of $CS_1B$="H" or $CS_2$="L", the $D_0$ to $D_7$ are high impedance and A0, RDB, WRB, SI and SCL inputs are ignored. If the serial interface is selected when $CS_1B$="H" or $CS_2$="L" the shift register and counter are reset. However, the reset is always operated in any conditions of $CS_1B$, $CS_2$.

## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage(1) | $V_{DD}$ | -0.3 to +7.0 | V |
| | | -0.3 to +3.6(Used Tripler) | |
| Supply Voltage(2) | $V_{SS2}$ | -7.0 to +0.3<br>-3.6 to +0.3(Used Tripler) | V |
| Supply Voltage(3) | $V_5$, $V_{OUT}$ | $V_{DD}$-11.0 to $V_{DD}$+0.3 | V |
| Supply Voltage(4) | $V_1$,$V_2$,$V_3$,$V_4$ | $V_5$ to $V_{DD}$+0.3 | V |
| Supply Voltage(5) | $V_{RS}$ | -7.0 to +0.3 | V |
| Input Voltage | $V_{IN}$ | -0.3 to $V_{DD}$+0.3 | V |
| Operating Temperature | $T_{opr}$ | -40 to +85 | °C |
| Strage temperature | $T_{stg}$ | -55 to +125 | °C |




Note 1) All voltage values are specified as $V_{SS1}$=0V.

Note 2) The relation of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 > V_{OUT}$; $V_{DD} > V_{SS1} \geq V_{OUT}$ must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to **NJU6674** at the mean time of turning on $V_{DD}$ power supply or after turned on $V_{DD}$.
In use of the voltage boost circuit, the condition that the supply voltage: 11.0V$\geq$ $V_{DD}$ -$V_{OUT}$ is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between $V_{DD}$ and $V_{SS1}$ due to the stabilized operation for the voltage converter.

## ■ DC Electrical Characteristics

($V_{DD}$=2.4V to 3.3V, $V_{SS}$=0V, Ta=-20 to 75°C)

| PARAMETER | | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Operating voltage (1) | | $V_{DD}$ | | | 2.4 | | 3.3 | V | 1 |
| Operating voltage (2) | | $V_{SS}$ | | | $V_{DD}$-3.3 | | $V_{DD}$-2.4 | V | |
| Operating voltage(3) | Recommend | $V_5$ | | | $V_{DD}$-10.0 | | $V_{DD}$-5.0 | V | |
| | Available | | | | $V_{DD}$-10.0 | | | | |
| | Available | $V_1$,$V_2$ | $V_{LCD}$=$V_{DD}$-$V_5$ | | $V_{DD}$-0.4x$V_5$ | | $V_{DD}$ | | |
| | Available | $V_3$,$V_4$ | | | $V_5$ | | $V_{DD}$-0.6x$V_5$ | | |
| "H" level input voltage | | $V_{IHC}$ | A0, $D_0$ to $D_7$, RDB, WRB, RESB, $CS_1$B, $CS_2$, P/S, SEL68 Terminal | | 0.8 x $V_{DD}$ | | $V_{DD}$ | V | |
| "L" level input voltage | | $V_{ILC}$ | | | $V_{SS}$ | | 0.2 x $V_{DD}$ | | |
| "H" level output voltage | | $V_{OHC}$ | $D_0$ to $D_7$ Terminal | $I_{OH}$=-0.5mA | 0.8 x $V_{DD}$ | | $V_{DD}$ | V | |
| "L" level output voltage | | $V_{OLC}$ | | $I_{OL}$= 0.5mA | $V_{SS}$ | | 0.2 x $V_{DD}$ | | |
| Input Leagage Current | | $I_{LI}$ | All input terminals | | -1.0 | | 1.0 | µA | |
| | | $I_{LO}$ | $D_0$ to $D_7$ terminals, Hi-Z state | | -3.0 | | 3.0 | | |
| Driver On-resistance | | $R_{ON}$ | Ta=25°C, $V_{LCD}$=8.0V | | | 3.0 | 4.5 | kΩ | 2 |
| Stand-by Current | | $I_{DDQ}$ | During Power Save Mode | | | 0.01 | 5.0 | µA | 3 |
| Input Terminal Capacitance | | $C_{IN}$ | Ta=25°C | | | 10.0 | | pF | 4 |
| Oscillation Frequency | | $f_{OSC}$ | $V_{DD}$= 3.0V Ta =25°C | | 10.2 | 12.5 | 14.8 | kHz | |
| Reset Time | | $t_R$ | RESB terminal | | 1.0 | | | µs | 5 |
| Reset "L" level pulse Width | | $t_{RW}$ | | | 10.0 | | | µs | 6 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Voltage booster | Input voltage | $V_{DD1}$ | 3-times boost | | 2.4 | | 3.3 | V | |
| | | $V_{DD2}$ | 4-times boost | | 2.4 | | 2.5 | | 7 |
| | | $V_{RS}$ | | | $V_{DD}$-5.0 | | $V_{DD}$-2.4 | V | |
| | Output voltage | $V_{OUT1}$ | 4-times boost, $V_{DD}$=2.5V | | -10.0 | | -9.5 | V | |
| | On-resistance | $R_{TRI}$ | 3-times boost, $V_{DD}$=3.0V, $C_{OUT}$=1.0µF | | | 1600 | 2600 | Ω | |
| | Adjustment range LCD driving voltage | $V_{OUT2}$ | Voltage boost operation off | | $V_{DD}$-10.0V | | $V_{DD}$-5.0V | V | 8 |
| | Voltage Follower | $V_5$ | Voltage adjustment circuit "OFF" | | $V_{DD}$-10.0V | | $V_{DD}$-5.0V | V | |
| | Int. resistor ratio | INTR | $V_{DD}$=3.0V, $V_{RS}$=$V_{DD}$-2.4V, EVR=$00_H$,$V_{OUT}$=$V_{DD}$-10.0V $V_5$=No load ;Ta =25°C | | | | 3.0 | % | 9 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Operating Current | $I_{DDQ1}$ | Power save mode | | 0.01 | 5 | µA | | |
| | $I_{OUT1}$ | $V_{DD}$=3.0V, $V_{LCD}$=5V, No access Com/Seg terminals non connect Display Checkerd pattern | | 51 | 85 | µA | 10 | |
| | $I_{OUT2}$ | | | 12 | 20 | µA | | |

Note 1) Although the **NJU6674** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

Note 2) $R_{ON}$ is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals ($V_1$,$V_2$,$V_3$,$V_4$) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).

Note 3) Apply no access from MPU.

Note 4) Apply A0, $D_0$ to $D_7$, RDB, WRB, $CS_1$B, $CS_2$, RESB, P/S, CL terminals.

Note 5) $t_R$ ( Reset Time ) refers to the reset completion time of the internal circuits from the rise edge of the RESB signal.

Note 6) Apply minimum pulse width of the RESB signal. To reset, the "L" pulse over $t_{RW}$ shall be input.

Note 7) Apply to the $V_{DD}$ when using 4-times boost.

Note 8) The voltage adjustment circuit controls $V_5$ within the range of the voltage follower operating voltage.

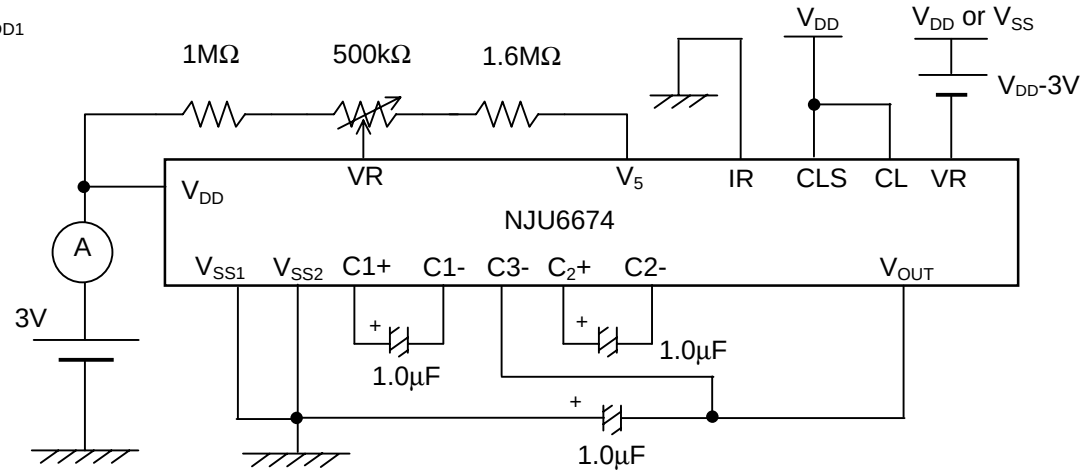
Note 9) INTR : The calculation of ($V_{LCD}$(Ideal)*[1]-($V_{LCD}$(Real))/$V_{LCD}$(Ideal)) x100%

*[1] $V_{LCD}$(Ideal)=Nx(1-63/162)x2.4 (N:Selected by the "Internal resistor ratio" )

Note10) Each operating current shall be defined as being measured in the following condition.

| Symbol | Power Control | | | Operating Condition | | | External Voltage Supply (Input terminal) |
|---|---|---|---|---|---|---|---|
| | $D_2$ | $D_1$ | $D_0$ | Voltage converter | Voltage regulator | Voltage Follower | |
| $I_{DD1}$ | 1 | 1 | 1 | Validity | Validity | Validity | Use($V_{SS2}$) |
| $I_{DD2}$ | 0 | 0 | 0 | Invalidity | Invalidity | Invalidity | Use($V_{OUT}$, $V_1$ to $V_5$) |

:$I_{DD1}$




:$I_{DD2}$

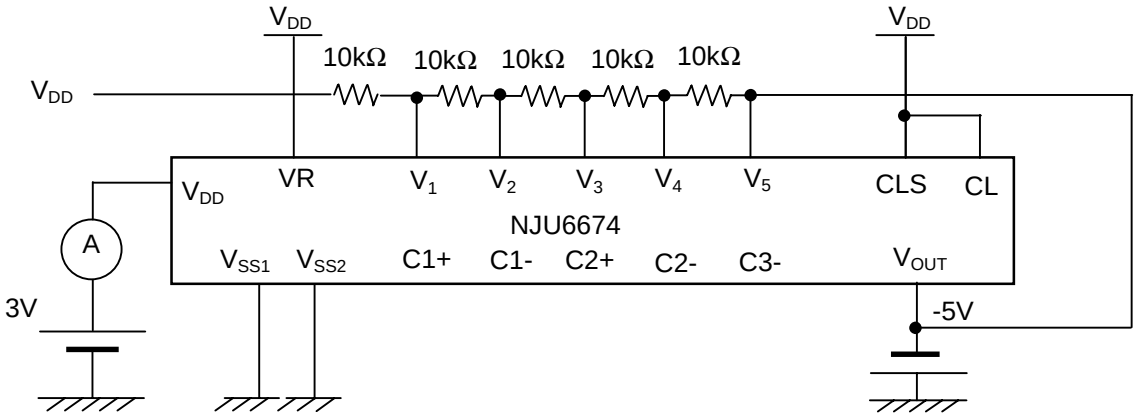
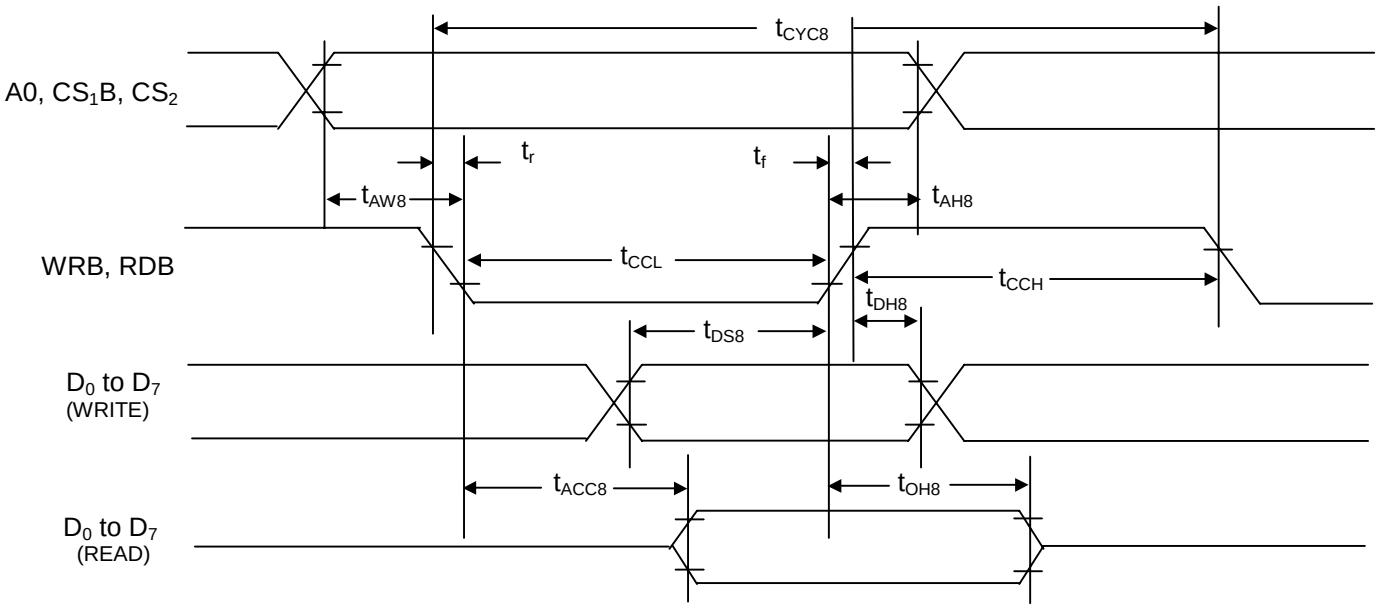



**Fig.7 MEASURMENT BLOCK DIAGRAM**

## ■ BUS TIMING CHARACTERISTICS

- Read and Write characteristics (80 type MPU)

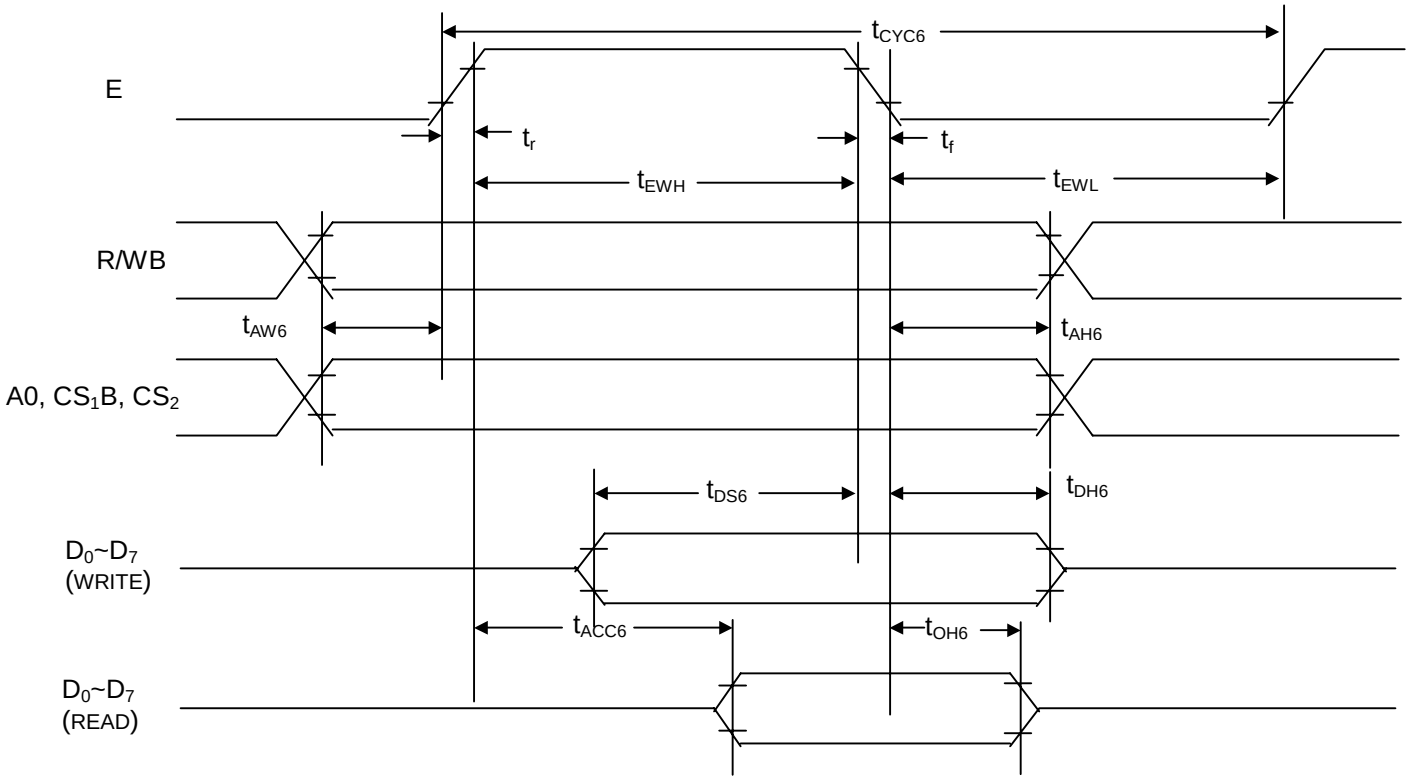



($V_{DD}$=2.7V to 3.3V, Ta=-20 to 75°C)

| Parameter | Terminal | Symbol | Condition | Min. | TYP | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Address hold time | $t_{AH8}$ | A0, $CS_1B$, $CS_2$ | | 0 | | | ns |
| Address set up time | $t_{AW8}$ | | | 0 | | | |
| System cycle time | $t_{CYC8}$ | WRB, RDB | | 300 | | | |
| Control “L” pulse width (Write) | $t_{CCL(W)}$ | | | 60 | | | |
| Control “L” pulse width (Read) | $t_{CCL(R)}$ | | | 120 | | | |
| Control “H” pulse width | $t_{CCH}$ | | | 60 | | | |
| Data set up time | $t_{DS8}$ | $D_0$ to $D_7$ | | 40 | | | |
| Data set up time | $t_{DH8}$ | | | 25 | | | |
| RD access time | $t_{ACC8}$ | | CL=100pF | | | 140 | |
| Output disable time | $t_{OH8}$ | | | 10 | | 100 | |
| Input signal rising, falling edge | $t_r$, $t_f$ | $CS_1B$, $CS_2$, WRB, RDB A0, $D_0$ to $D_7$ | | | | 15 | |

- *:All timing based on 20% and 80% of $V_{DD}$ voltage level.

Read and Write characteristics (68 type MPU)

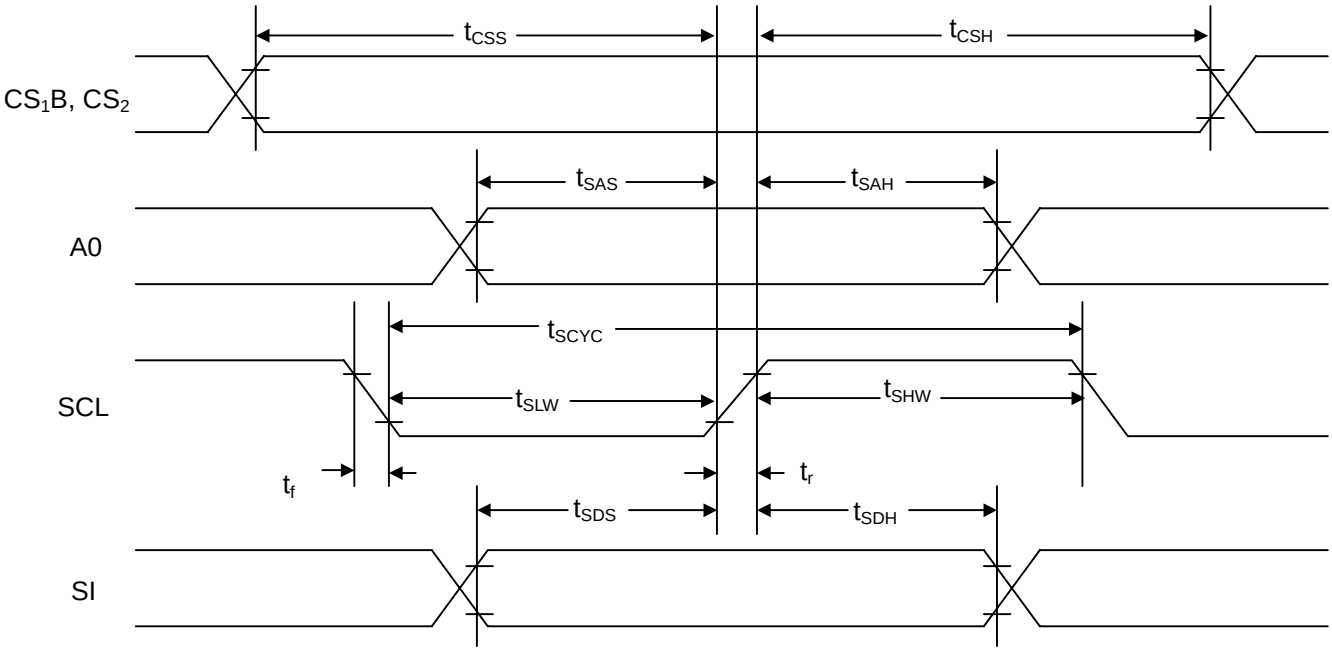



($V_{DD}$=2.7V to 3.3V, Ta=-20 to 75°C)

| Parameter | | Symbol | Terminal | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|---|
| Address hold time | | $t_{AH6}$ | A0, $CS_1B$ $CS_2$, R/WB | | 0 | | | ns |
| Address set up time | | $t_{AW6}$ | | | 0 | | | |
| System cycle time | | $t_{CYC6}$ | E | | 300 | | | |
| Enable "H" pulse width (Read) | WRITE | $t_{EWH}$ | E | | 120 | | | |
| | READ | | | | 60 | | | |
| Enable "L" pulse width (Read) | WRITE | $t_{EWL}$ | E | | 60 | | | |
| | READ | | | | 60 | | | |
| Data set up time | | $t_{DS6}$ | $D_0$ to $D_7$ | | 40 | | | |
| Data hold time | | $t_{DH6}$ | | | 25 | | | |
| RD access time | | $t_{ACC6}$ | | CL=100pF | | | 140 | |
| Output disable time | | $t_{OH6}$ | | | 10 | | 100 | |
| Input signal rising, falling edge | | $t_r$, $t_f$ | E, R/WB, A0, $D_0$ to $D_7$ | | | | 15 | |

*:All timing based on 20% and 80% of $V_{DD}$ voltage level.
*:$t_{CYC6}$ shows the cycle of theE signal in active $CS_1B$ and $CS_2$.

Write characteristics (Serial interface)

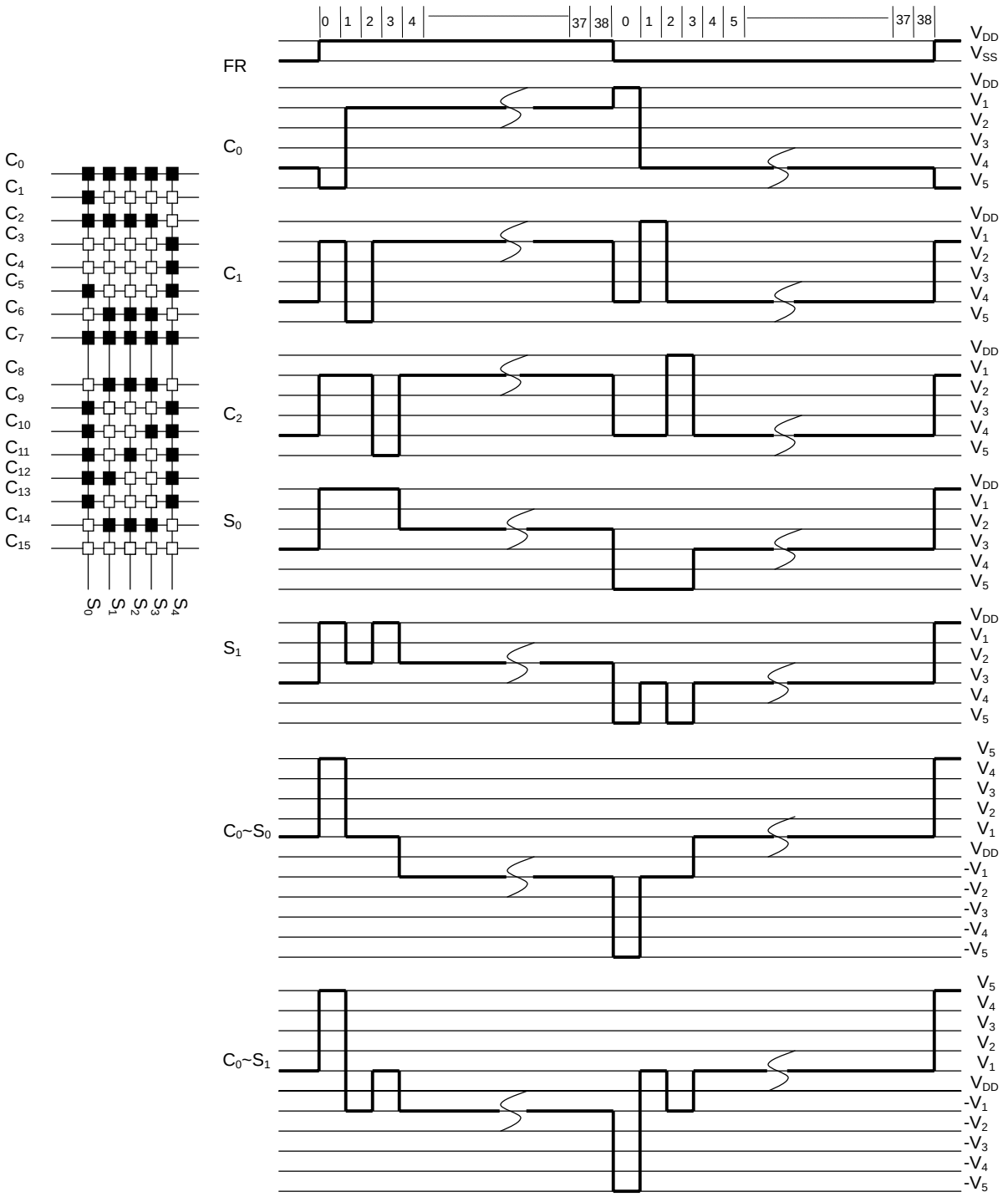



($V_{DD}$=2.7V to 3.3V, Ta=-20 to 75°C)

| Parameter | Symbol | Terminal | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Serial clock cycle | $t_{SCYC}$ | SCL | | 250 | | | ns |
| SCL "H" pulse width | $t_{SHW}$ | | | 100 | | | |
| SCL "L" pulse width | $t_{SLW}$ | | | 100 | | | |
| Address set up time | $t_{SAS}$ | A0 | | 150 | | | |
| Address hold time | $t_{SAH}$ | | | 150 | | | |
| Data set up time | $t_{SDS}$ | SI | | 100 | | | |
| Data hold time | $t_{SDH}$ | | | 100 | | | |
| CS-SCL time | $t_{CSS}$ | $CS_1B$, $CS_2$ | | 150 | | | |
| | $t_{CSH}$ | | | 150 | | | |
| Input signal rising, falling edge | $t_f$, $t_r$ | $CS_1B$, $CS_2$ SCL, SI, A0 | | | | 15 | |

*:All timing based on 20% and 80% of $V_{DD}$ voltage level.

## ■ LCD DRIVING WAVEFORM

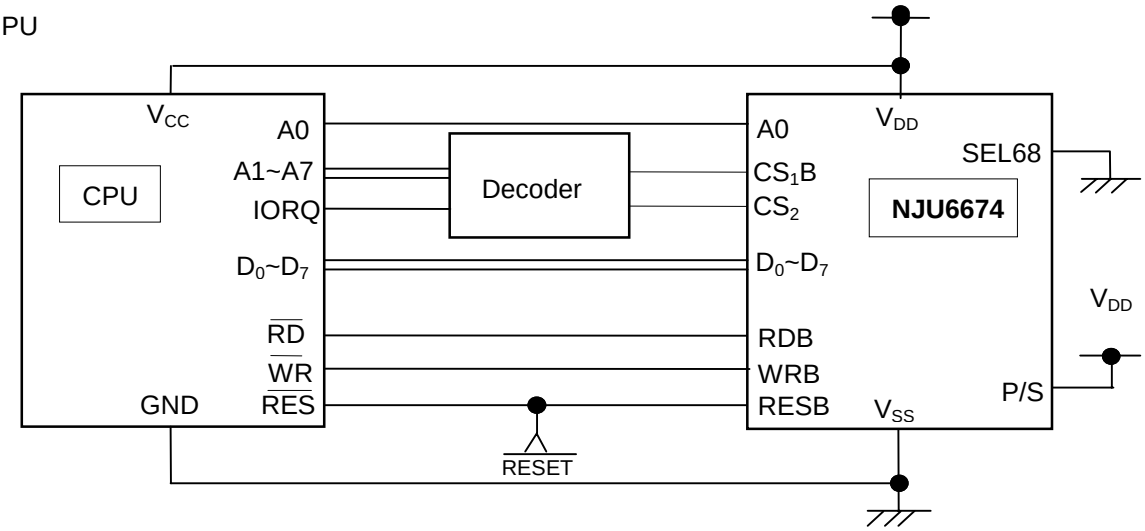


## ■ APPLICATION CIRCUIT

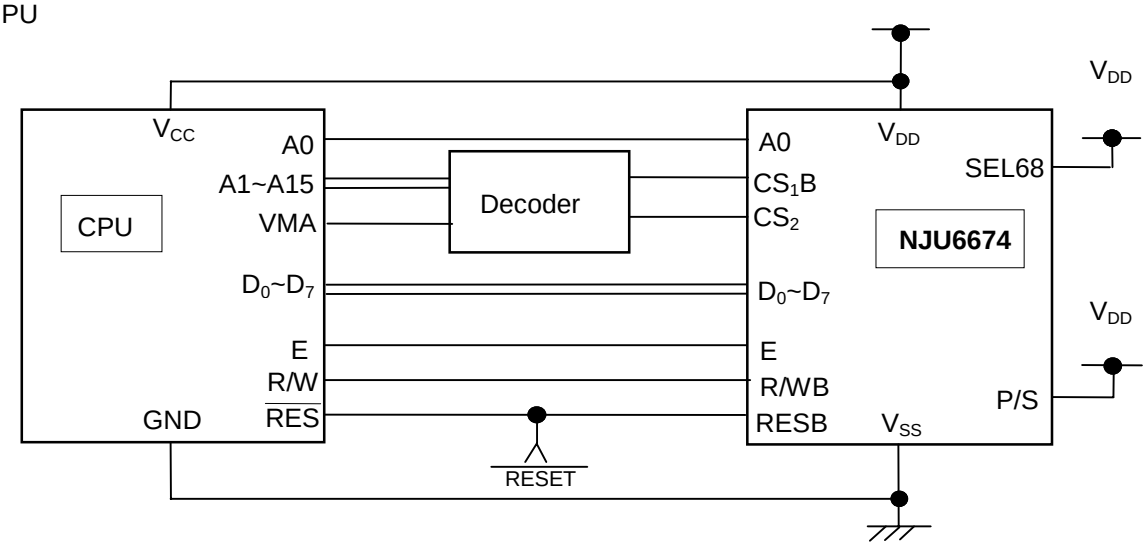
- (1) Microprocessor Interface Example
  The **NJU6674** interfaces to 80 type or 68 type MPU directly.
  And the serial interface also communicate with MPU.

  * : C86 terminal must be fixed $V_{DD}$ or $V_{SS}$.

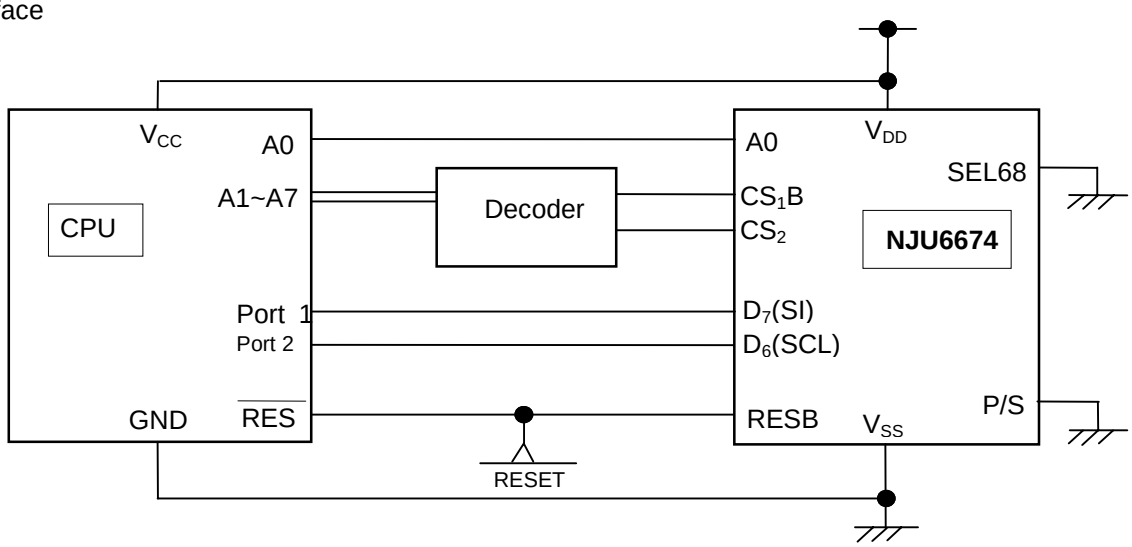
● 80 Type MPU




● 68 Type MPU




● Serial Interface



# MEMO