December 1994

National Semiconductor

LMC6042
CMOS Dual Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

Features

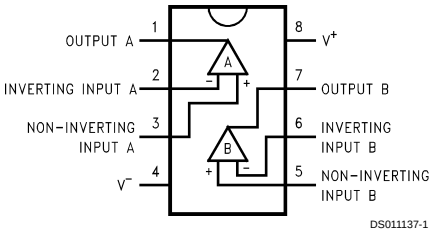
- Low supply current: 10 µA/Amp (typ)
- Operates from 4.5V to 15V single supply
- Ultra low input current: 2 fA (typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



Ordering Information

Package	Temperature Range	NSC Drawing	Transport Media
	Industrial −40˚C to +85˚C		
8-Pin Small Outline	LMC6042AIM	M08A	Rail
	LMC6042IM		Tape and Reel
8-Pin Molded DIP	LMC6042AIN	N08E	Rail
	LMC6042IN		

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature	
(Soldering, 10 seconds)	260˚C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 3)	110˚C
ESD Tolerance (Note 4)	500V
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V

Operating Ratings

Temperature Range	
LMC6042AI, LMC6042I	$-40˚C \le T_J \le +85˚C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101˚C/W
8-Pin SO	165˚C/W

Electrical Characteristics

Unless otherwise spec ified, all limits guaranteed for $T_A = T_J = 25˚C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3	6	mV
					3.3	**6.3**	Max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/˚C
I_B	Input Bias Current			0.002	**4**	**4**	pA (Max)
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA (Max)
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$, $V^+ = 15V$		75	68	62	dB
					66	**60**	Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$		75	68	62	dB
					66	**60**	Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$		94	84	74	dB
					83	**73**	Min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V, For CMRR ≥ 50 dB		−0.4	−0.1	−0.1	V
					0	**0**	Max
				V^+−1.9V	V^+− 2.3V	V^+− 2.3V	V
					V^+− 2.5V	**V^+− 2.4V**	Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400	300	V/mV
					300	**200**	Min
			Sinking	500	180	90	V/mV
					120	**70**	Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200	100	V/mV
					160	**80**	Min
			Sinking	250	100	50	V/mV
					60	**40**	Min

Electrical Characteristics (Continued)

Unless otherwise spec ified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$	4.987	4.970	4.940	V
		$R_L = 100\ k\Omega$ to $V^+/2$		**4.950**	**4.910**	Min
			0.004	0.030	0.060	V
				0.050	**0.090**	Max
		$V^+ = 5V$	4.980	4.920	4.870	V
		$R_L = 25\ k\Omega$ to $V^+/2$		**4.870**	**4.820**	Min
			0.010	0.080	0.130	V
				0.130	**0.180**	Max
		$V^+ = 15V$	14.970	14.920	14.880	V
		$R_L = 100\ k\Omega$ to $V^+/2$		**14.880**	**14.820**	Min
			0.007	0.030	0.060	V
				0.050	**0.090**	Max
		$V^+ = 15V$	14.950	14.900	14.850	V
		$R_L = 25\ k\Omega$ to $V^+/2$		**14.850**	**14.800**	Min
			0.022	0.100	0.150	V
				0.150	**0.200**	Max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16	13	mA
				10	**8**	Min
		Sinking, $V_O = 5V$	21	16	13	mA
				8	**8**	Min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15	15	mA
				10	**10**	Min
		Sinking, $V_O = 13V$ (Note 12)	39	24	21	mA
				8	**8**	Min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	20	34	45	µA
				39	**50**	Max
		Both Amplifiers $V^+ = 15V$	26	44	56	µA
				51	**65**	Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015	0.010	V/µs
				0.010	**0.007**	Min
GBW	Gain-Bandwidth Product		100			kHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	83			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0002			$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -5$ R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

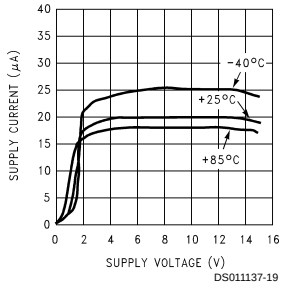
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

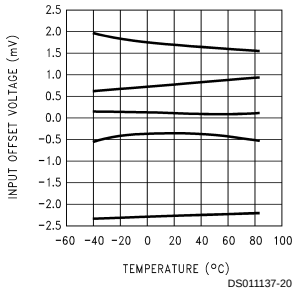
Note 12: Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

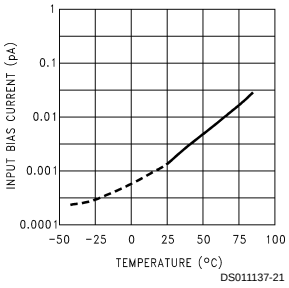
Supply Current vs Supply Voltage



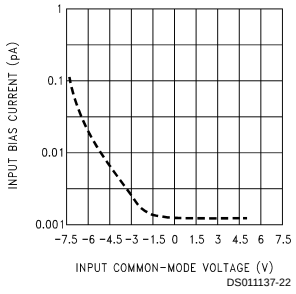
Offset Voltage vs Temperature of Five Representative Units



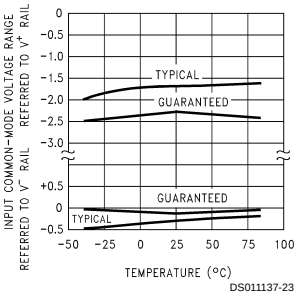
Input Bias Current vs Temperature



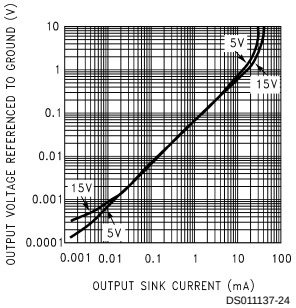
Input Bias Current vs Input Common-Mode Voltage



Input Common-Mode Voltage Range vs Temperature

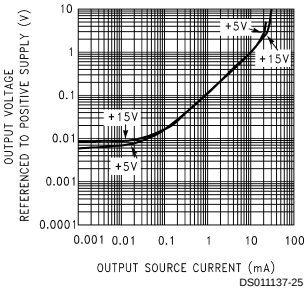


Output Characteristics Current Sinking



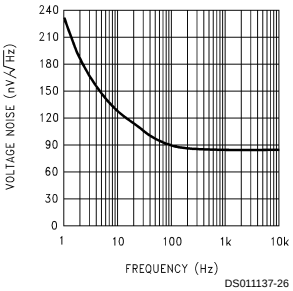
Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

Output Characteristics Current Sourcing



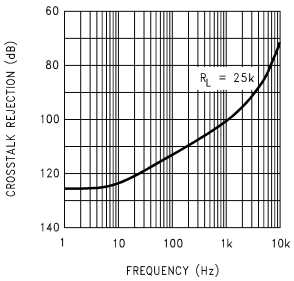
DS011137-25

Input Voltage Noise vs Frequency



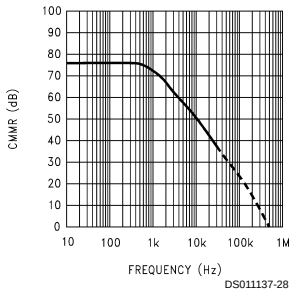
DS011137-26

Crosstalk Rejection vs Frequency



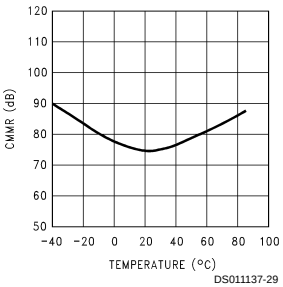
DS011137-27

CMRR vs Frequency



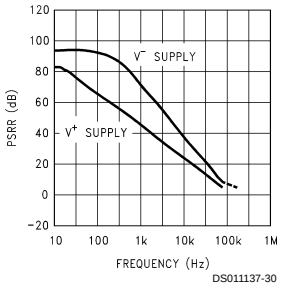
DS011137-28

CMRR vs Temperature



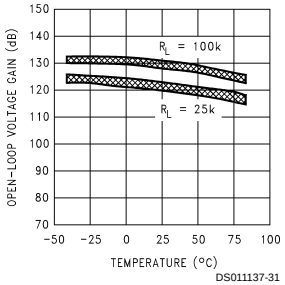
DS011137-29

Power Supply Rejection Ratio vs Frequency



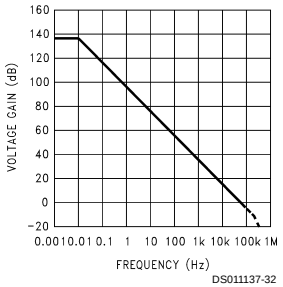
DS011137-30

Open-Loop Voltage Gain vs Temperature



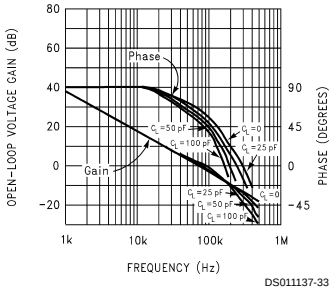
DS011137-31

Open-Loop Frequency Response



DS011137-32

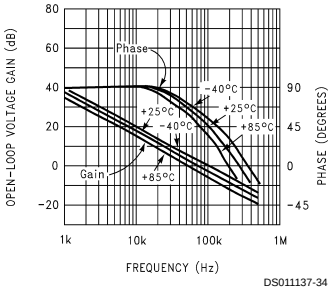
Gain and Phase Responses vs Load Capacitance



DS011137-33

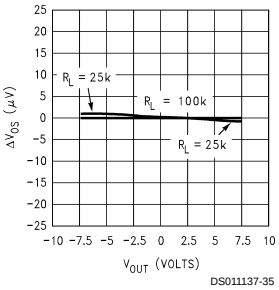
Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

Gain and Phase Response vs Temperature



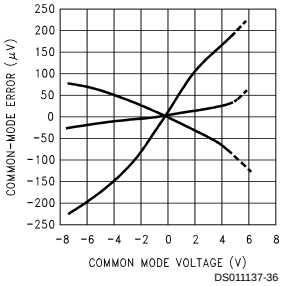
DS011137-34

Gain Error (V_{OS} vs V_{OUT})



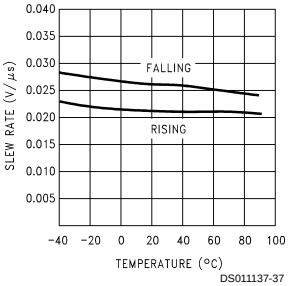
DS011137-35

Common-Mode Error vs Common-Mode Voltage of 3 Representative Units



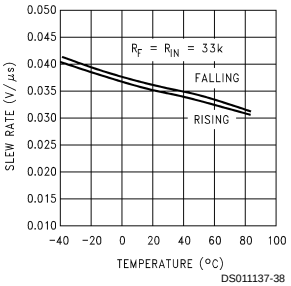
DS011137-36

Non-Inverting Slew Rate vs Temperature



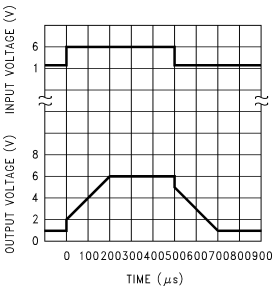
DS011137-37

Inverting Slew Rate vs Temperature



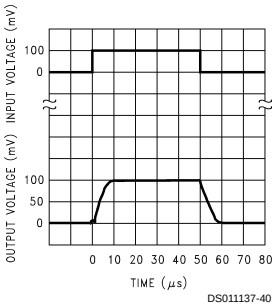
DS011137-38

Non-Inverting Large Signal Pulse Response (A_V = +1)



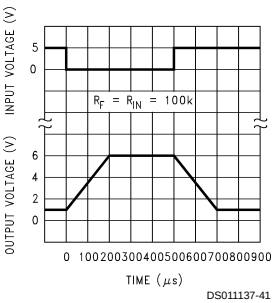
DS011137-39

Non-Inverting Small Signal Pulse Response



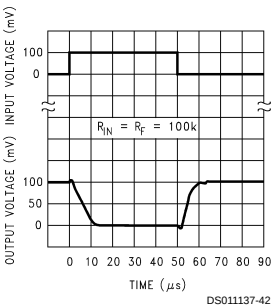
DS011137-40

Inverting Large-Signal Pulse Response



DS011137-41

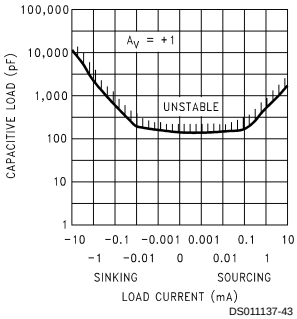
Inverting Small Signal Pulse Response



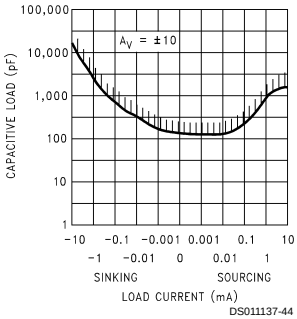
DS011137-42

Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified (Continued)

Stability vs Capacitive Load



Stability vs Capacitive Load



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6042 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6042 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input curent, like the LMC6042.

Although the LMC6042 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6042 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work).**

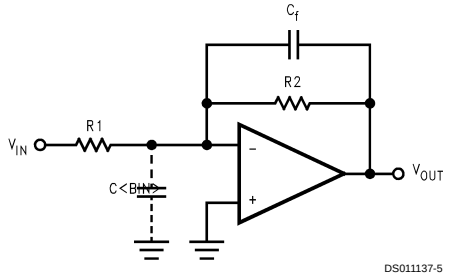


FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R1\, C_{IN}} \geq \frac{1}{2\pi R2\, C_f}$$

or

$$R1\, C_{IN} \leq R2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.

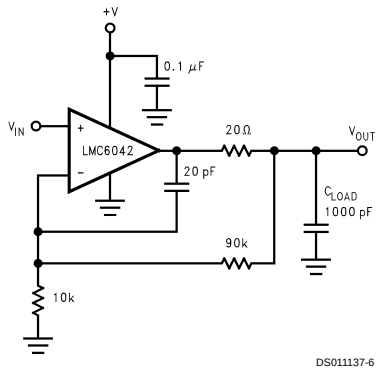


FIGURE 2. LMC6042 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency compo-

Applications Hints (Continued)

nent of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3*). Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

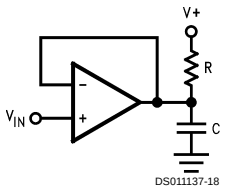


FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6042, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6042's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6042's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 5* for typical connections of guard rings for standard op-amp configurations.

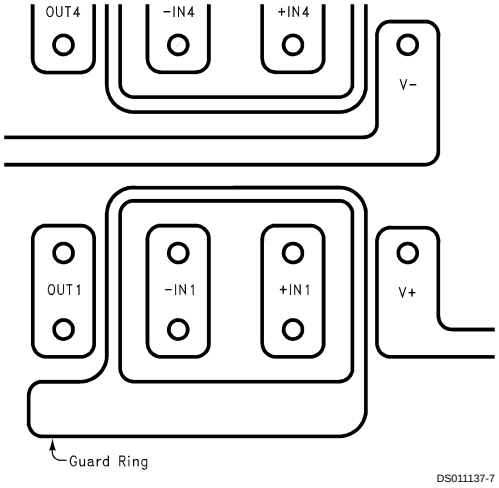
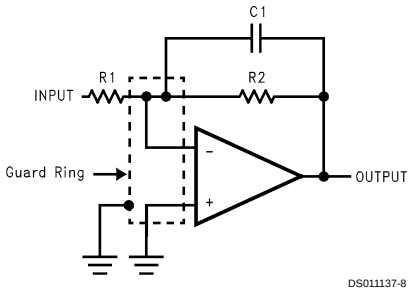
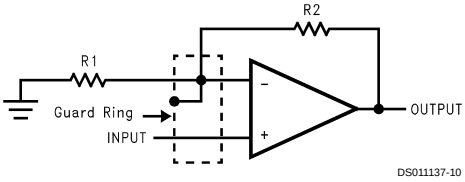


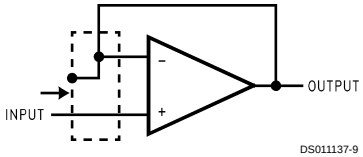
FIGURE 4. Example of Guard Ring in P.C. Board Layout



Inverting Amplifier



Non-Inverting Amplifier

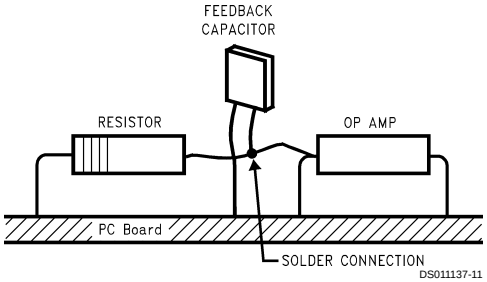


Follower

FIGURE 5. Typical Connections of Guard Rings

Applications Hints (Continued)

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6042 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in *Figure 7* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20 µA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 7*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R0}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R0}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6042, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S − 2.3V, worst case at room temperature. This feature of the LMC6042 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 8*. Provisions have been made for low sensitivity trimming of CMRR and gain.

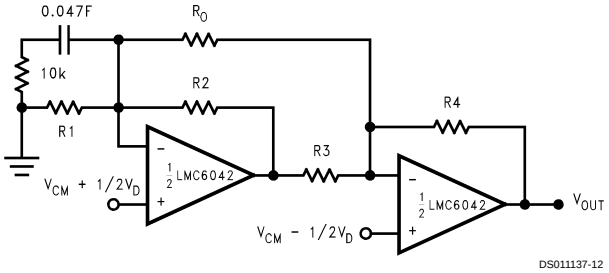


FIGURE 7. Two Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

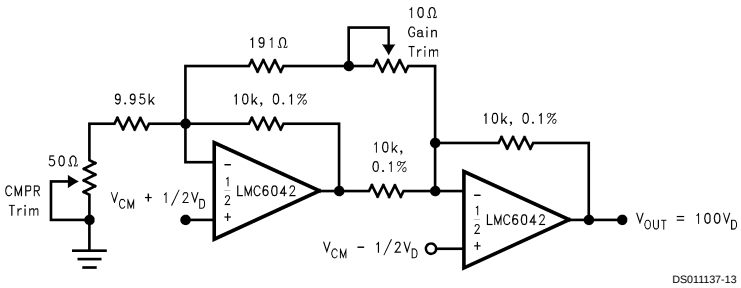


FIGURE 8. Low-Power Two-Op-Amp Instrumentation Amplifier

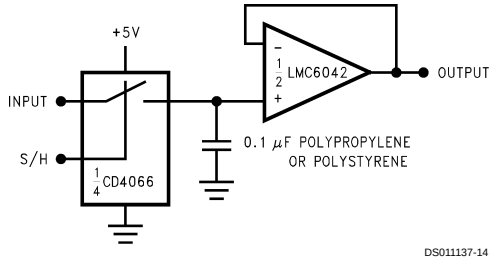


FIGURE 9. Low-Leakage Sample and Hold

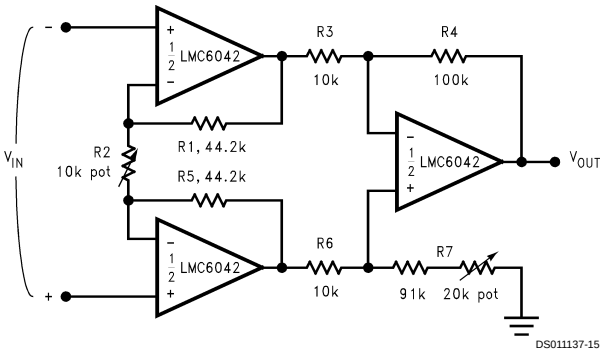


FIGURE 10. Instrumentation Amplifier

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

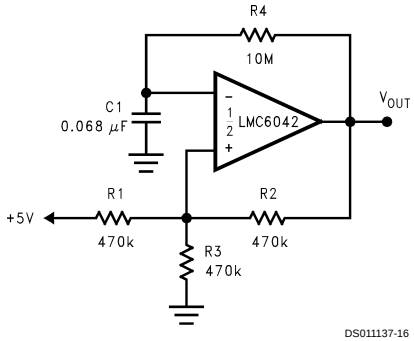


FIGURE 11. 1 Hz Square Wave Oscillator

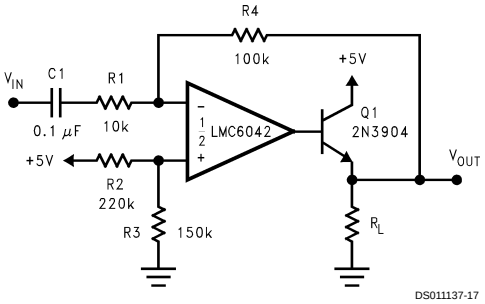
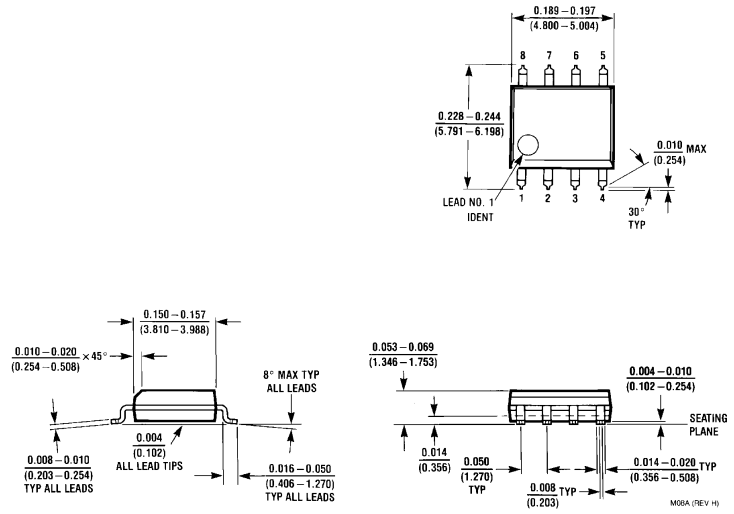
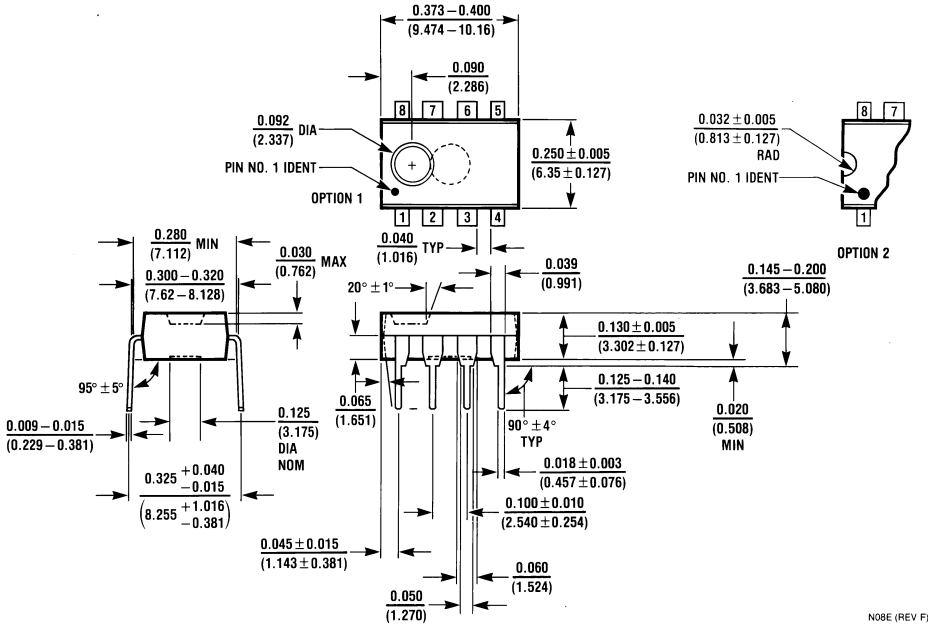


FIGURE 12. AC Coupled Power Amplifier

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Small Outline Package
Order Number LMC6042AIM or LMC6042IM
NS Package Number M08A



8-Pin Molded Dual-In-Line Package
Order Number LMC6042AIN or LMC6042IN
NS Package Number N08E

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