National Semiconductor

MILITARY DATA SHEET

MNDS26LS32-X REV 2B0

Original Creation Date: 10/17/95
Last Update Date: 10/21/96
Last Major Revision Date: 04/08/96

QUAD DIFFERENTIAL LINE RECEIVERS

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have and input sensitivity of 200 mV over the input voltage range of $\pm$ 7V and the DS26LS33 and DS26LS33A have an input senssitivity of 500 mV over the input voltage range of $\pm$ 15V.

Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE outputs with 8mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Industry Part Number

DS26LS32

NS Part Numbers

DS26LS32ME/883
DS26LS32MJ/883
DS26LS32MW/883

Prime Die

DS26LS32

Controlling Document

5962-7802006QEA,QFA,Q2A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32
- ±0.2 sensitivity over the input voltage range on the DS26LS32
- Input fail-safe circuitry on the DS26LS32A.
- DS26LS32 meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32
- Operation from a single 5V supply
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage	7V
Common-Mode Range	± 25V
Differential Input Voltage	± 25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation at 25C (Note 2)	
J package	1666.5 mW
E package	1875 mW
W package	967.74 mW
Storage Temperature Range	-65C to +165C
Lead Temperature (Soldering, 4 Seconds)	260C

Note 1: "Absolute Maximum Rating" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Derate J package 11.11 mW/C above 25C; derate E package 12.5 mW/C above 25C. Derate W package: 6.4516 mW/C above 25C.

Recommended Operating Conditions

Supply Voltage, (Vcc)	4.50V to 5.50V
Temperature, (Ta)	-55C TO +125C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC = 5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIN	Input Current	VCC=5.5V, VIN=15V (Pin under test), other inputs -15V ≤VIN≤ +15V	2			2.3	mA	1, 2, 3
		VCC=5.5V, VIN=-15V(Pin under test), other inputs -15V ≤VIN≤ +15V	2			-2.8	mA	1, 2, 3
IIL	Logical "0" ENABLE Current	VCC=5.5V, VIN= 0.4V	2			-360	uA	1, 2, 3
IIH	Logical "1" ENABLE Current	VCC=5.5V, VIN=2.7V	2			20	uA	1, 2, 3
II	Logical "1" ENABLE Current	VCC=5.5V, VIN=5.5V	2			100	uA	1, 2, 3
VIC	Input Clamp Voltage (ENABLE)	VCC=4.5V, IIN=-18mA	2			-1.5	V	1, 2, 3
VOH	Logical "1" Output Voltage	VCC=4.5V, IOH=-440uA, DELTA VIN = 1V, $\overline{\text{VENABLE}}$ = 0.8V	2		2.5		V	1, 2, 3
VOL	Logical "0" Output Voltage	VCC=4.5V, IOL= 4mA, DELTA VIN = -1V, $\overline{\text{V ENABLE}}$ = 0.8V	2			.4	V	1, 2, 3
		VCC=4.5V, IOL= 8mA, DELTA VIN = -1V, $\overline{\text{V ENABLE}}$ = 0.8V	2			.45	V	1, 2, 3
IOS(MIN)	Output Short Circuit Current	VCC = 5.5V, VO=0V, DELTA VIN = 1V	2		-15		mA	1, 2, 3
IOS(MAX)	Output Short Circuit Current	VCC = 5.5V, VO=0V, DELTA VIN = 1V	2			-85	mA	1, 2, 3
ICC	Supply Current	VCC = 5.5V, All VIN = GND, Outputs Disabled	2			70	mA	1, 2, 3
IOFF	Off-State Output Current	VCC = 5.5V, VO= 0.4V	2			-20	uA	1, 2, 3
		VCC = 5.5V, VO= 2.4V	2			20	uA	1, 2, 3
VTH	Differential Input Voltage	-7V ≤ VCM ≤ 7V	1, 2		-0.2	0.2	V	1, 2, 3
RIN	Input Resistance	-15V ≤ VCM ≤ 15V	2		6		kohm	1, 2, 3
VIL	Logical "0" Input Voltage (ENABLE)	VCC= 4.5V	1, 2			0.8	V	1, 2, 3
VIH	Logical "1" Input Voltage (ENABLE)	VCC= 4.5V	1, 2		2		V	1, 2, 3

Electrical Characteristics

AC PARAMETERS PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VCC=5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Propagation Delay Time	Cl=15pF	3			30	nS	9, 11
			3			120	nS	10
tPHL	Propagation Delay Time	Cl=15pF	3			30	nS	9, 11
			3			120	nS	10
tLZ	Enable Time	$\overline{\text{ENABLE}}$ Cl=5pF	3			34	nS	9
		$\overline{\text{ENABLE}}$ Cl=5pF	3			64	nS	10
		$\overline{\text{ENABLE}}$ Cl=5pF	3			27	nS	11
tHZ	Enable Time	$\overline{\text{ENABLE}}$ Cl=5pF	3			32	nS	9, 11
		$\overline{\text{ENABLE}}$ Cl=5pF	3			35	nS	10
tZL	Disable Time	$\overline{\text{ENABLE}}$ Cl=15pF	3			34	nS	9
		$\overline{\text{ENABLE}}$ Cl=15pF	3			65	nS	10
		$\overline{\text{ENABLE}}$ Cl=15pF	3			27	nS	11
tZH	Disable Time	$\overline{\text{ENABLE}}$ Cl=15pF	3			35	nS	9
		$\overline{\text{ENABLE}}$ Cl=15pF	3			65	nS	10
		$\overline{\text{ENABLE}}$ Cl=15pF	3			27	nS	11

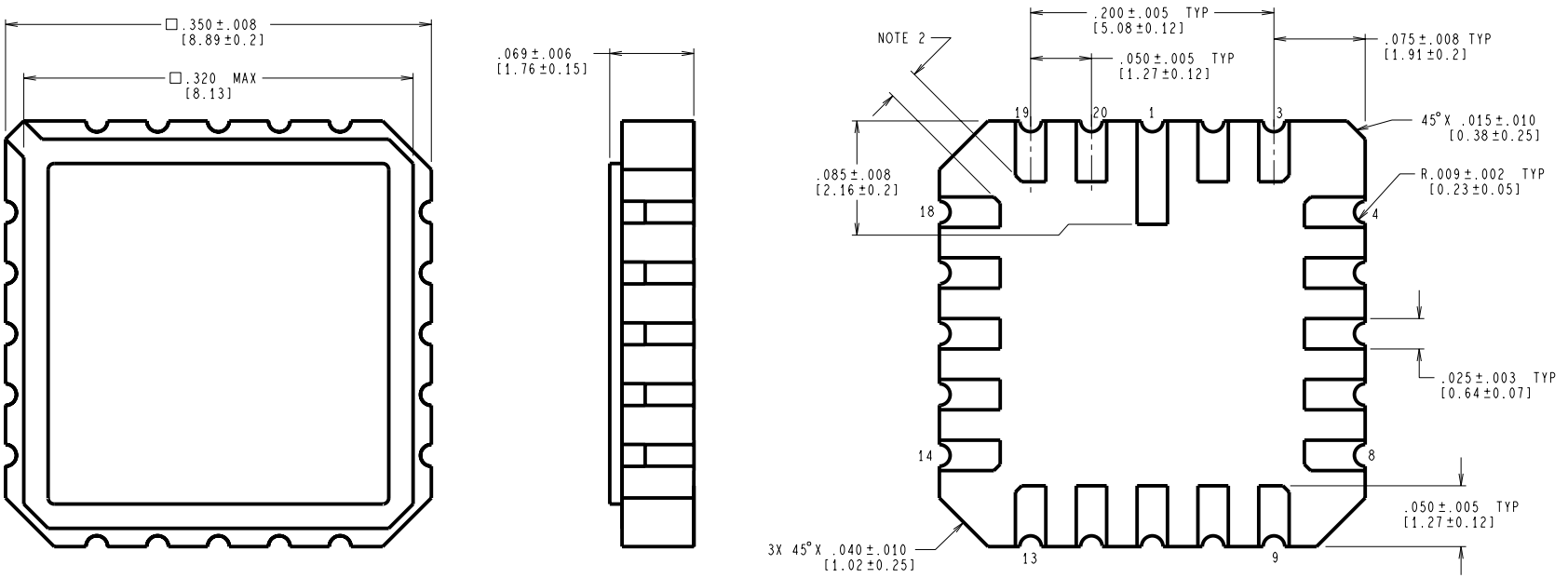
Note 1: Parameter tested go-no-go only.
Note 2: For Subgroups 1 and 2: Power dissipation must be externally controlled at elevated temperatures.
Note 3: Tested at 25C, guaranteed but not tested at +125C & -55C.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPAC (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

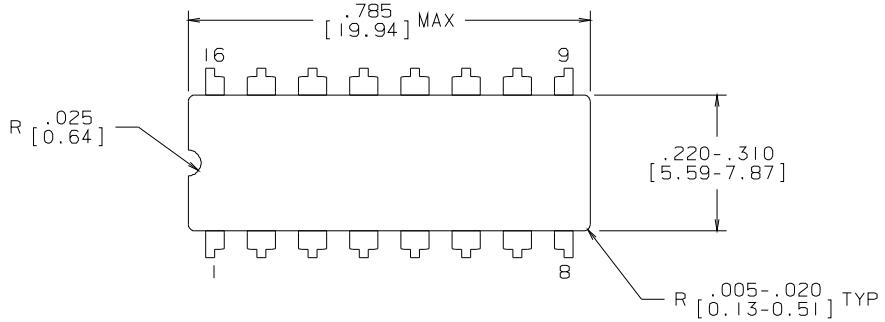
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

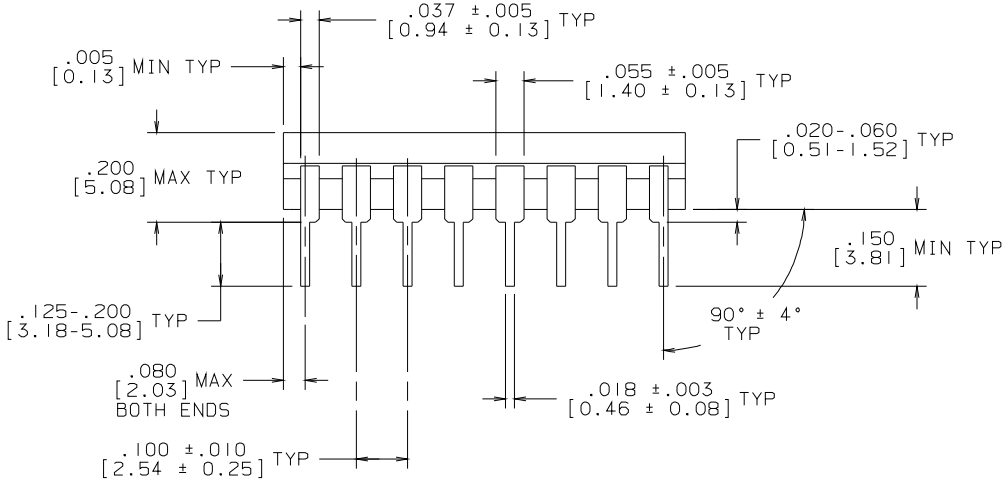
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

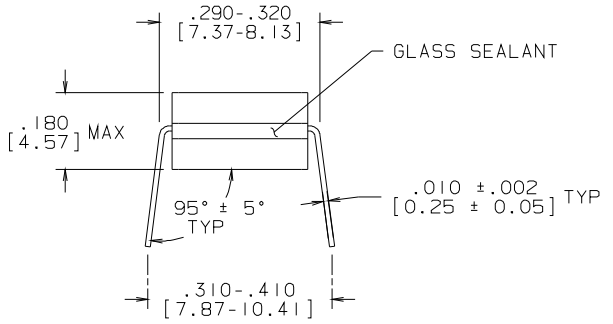
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

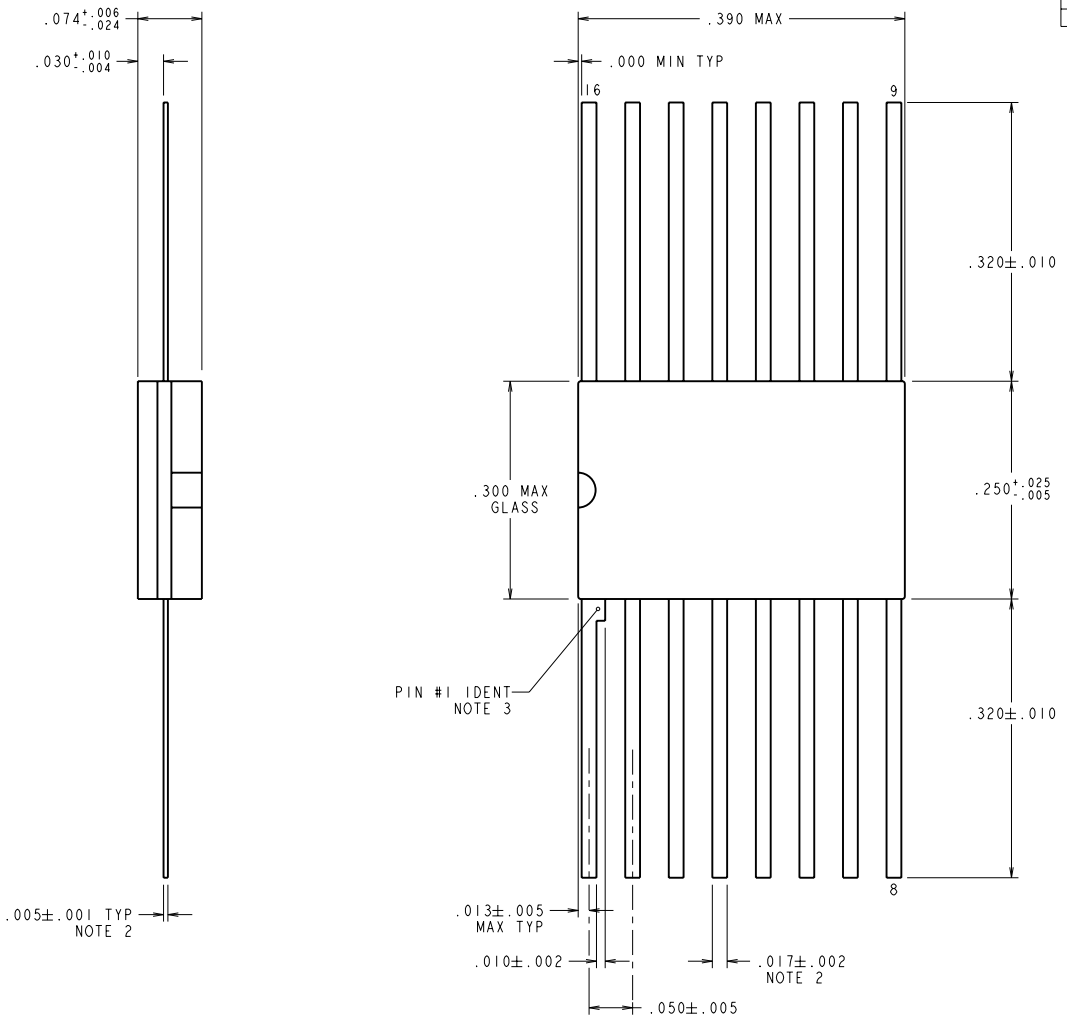
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION

INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1