National Semiconductor

MILITARY DATA SHEET

MNDS3886A-X REV 2B0

Original Creation Date: 09/21/94
Last Update Date: 10/21/96
Last Major Revision Date: 02/22/95

BTL 9-BIT LATCHING DATA TRANSCEIVER

General Description

The DS3886A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3886A is a BTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic-BTL) as specified in the IEEE 896.2 Futurebus+ specification. The DS3886A incorporates an edge-triggered latch in the driver path which can be bypassed during fall-through mode of operation and a transparent latch in the receiver path. Utilization of the DS3886A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3886A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with it's collector to isolate the transistor output capacitance from the bus, thus reducing the bus loading in the inactive state. The combined output capacitance of the driver output and receiver input is less than 5pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V at 25/125 C and 1.1V at -55 C.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QVcc and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE and fully TTL compatible.

The DS3886A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the Vcc pin. The DS3886A also provides glitch free power up/down protection during power sequencing.

The DS3886A has two types of power connections in addition to the LI pin. They are the Logic Vcc (Vcc) and the Quiet Vcc (QVcc). There are two Logic Vcc pins on the DS3886A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the Vcc bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between Vcc and QVcc should never exceed $\pm$0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the T/$\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the Vcc pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on Vcc +0.5V.

General Description (Continued)

There are three different types of ground pins on the DS3886A; the logic ground (GND), BTL grounds (B0GND-B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND-B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3886A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND-B8GND should not exceed $\pm$0.5V including power up/down sequencing.

Additional transceivers included in the Futurebus+ family are; the DS3884A BTL Handshake Transceiver featuring selectable Wired-OR glitch filtering, the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/ABP signal lines.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

All of the transceivers are offered in 48-pin CERPAC package.

Industry Part Number

DS3886A

NS Part Numbers

DS3886AW/883

Prime Die

T3886C

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 9-BIT BTL Latched Transceiver
- Driver incorporates edge triggered latches
- Receiver incorporates transparent latches
- Supports Live Insertion
- Glitch free Power-up/down protection
- Typically less than 5pF Bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80mA
- Open collector Bus-port outputs allows Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible Driver and Control inputs
- Built in Bandgap reference with separate QVcc and QGND pins for precise receiver thresholds
- Individual Bus-port ground pins
- Product offered in CERPAC package style

(Absolute Maximum Ratings)

(Note 1, 2)

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15mA
Bus Termination Voltage	2.4V
Power Dissipation at 25 C (CERPAC) Derate at 11.5mW/ C above 25 C	1.7W
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 4 seconds)	260 C

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed Vcc plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QVcc and Vcc. There is a diode between each input and/or output to Vcc which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50mA. Exception, LI and Bn pins do not have power sequencing requirements with respect to Vcc and QVcc. Furthermore, the difference between Vcc and QVcc should never be greater than 0.5V at any time including power-up.

Recommended Operating Conditions

	Min.	Max.	Units
Supply Voltage (Vcc)	4.5	5.5	V
Bus Termination Voltage (Vt)	2.06	2.14	V
Operating Free Air Temperature	-55	+125	C

Electrical Characteristics

DC: DRIVER AND CONTROL INPUT (CD,T/$\overline{R}$,An,ACLK,LE and RBYP)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical 1 Input Voltage				2		V	1, 2, 3
Vil	Logical 0 Input Voltage					0.8	V	1, 2, 3
Ii	Input Leakage Current	Vcc 5.5V, Vin = 5.5V				100	uA	1, 2, 3
Iih	Input High Current	Vcc 5.5V, Vin=2.4V, An=CD=0.5V, T/R = 2.4V				40	uA	1, 2, 3
Iil	Input Low Current	Vcc 5.5V, Vin=An=CD=0.5V, T/R=2.4V				-100	uA	1, 2, 3
Vcl	Input Clamp Diode Voltage	Vcc 4.5V, Ii = -12mA				-1.2	V	1, 2, 3

DC PARAMETERS: DRIVER OUTPUT/RECEIVER INPUT (Bn)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

Volb	Output Low Bus Voltage	Vcc 4.5V, Io=80mA, CD=0.5V, An=T/$\overline{R}$=2.4V	1		0.75	1.10	V	1, 2
		Vcc 4.5V, Io=80mA, CD=0.5V, An=T/$\overline{R}$=2.4V	1		0.75	1.15	V	3
Iolbz	Output Low Bus Current	Vcc 5.5V, An=0.5V, CD=0V, BN=0.75V, T/$\overline{R}$=2.4V				-100	uA	1, 2, 3
Iohbz	Output High Bus Current	Vcc 5.5V, An=0.5V, CD=0V, BN=2.1V, T/$\overline{R}$=2.4V				100	uA	1, 2, 3
Vth	Receiver Input Threshold	T/$\overline{R}$ = CD = 0.5V			1.47	1.62	V	1, 2, 3
Vclp	Positive Clamp Diode Voltage	Vcc = 5.5 or 0V, Ibn = 1mA			2.0	4.6	V	1, 2, 3
		Vcc = 5.5 or 0V, Ibn = 10mA			2.6	5.1	V	1, 2, 3
Vcln	Negative Clamp Diode Voltage	Vcc = 5.5V, Iclamp = -12mA				-1.2	V	1, 2, 3

Electrical Characteristics

DC PARAMETERS: RECEIVER OUTPUT (AN)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical 1 Output Voltage	Vcc=4.5V, Ioh = -2mA, Bn=1.1V, T/$\overline{R}$=CD=0.5V			2.4		V	1, 2, 3
Vol	Logical 0 Output Voltage	Vcc=4.5V, T/$\overline{R}$=CD=0.5V, Bn=2.1V, Iol=8mA				0.4	V	1, 2, 3
		Vcc=4.5V, T/$\overline{R}$=CD=0.5V, Bn=2.1V, Iol=24mA				0.5	V	1, 2, 3
Ioz	TRI-STATE Leakage Current	Vcc=5.5V, CD=2.4V, T/$\overline{R}$=0.5V, BN=0.75, Vin=2.4V				40	uA	1, 2, 3
		Vcc=5.5V, CD=2.4V, T/$\overline{R}$=0.5V, Bn=0.75, Vin=0.5V				-100	uA	1, 2, 3
Ios	Output Short Circuit Current	Vcc=5.5V, Bn=1.1V, T/$\overline{R}$=CD=0.5V	2		-40	-100	mA	1, 2, 3

DC PARAMETERS: SUPPLY CURRENT

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

IccT	Supply Current Includes Vcc	Vcc=5.5V, T/$\overline{R}$=An=ACLK=RBYP=LE=3.4V, CD=0.5V				70	mA	1, 2, 3
Icc	Supply Current for a TTL High Input	T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, ACLK = RBYP = LE = 0.5V				60	mA	1, 2, 3
Ili	Live Insertion Current	Vcc = 5.5V, T/$\overline{R}$=AN=CD=ACLK=0.5V				6	mA	1, 2, 3
		Vcc = 5.5V, T/$\overline{R}$=AN=RBYP=2.4V, CD=ACLK=0.5V				3	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: DRIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLA	An to Bn Propagation Delay (Fall-through Mode)	CD=0V, RBYP=T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			1	8	nS	9, 10, 11
tPLHA	An to Bn Propagation Delay (Fall-through Mode)	CD=0V, T/$\overline{R}$=RBYP=3V, RL=12.5 Ohm, CL=30pF			1	8	nS	9, 10, 11
tPHLCK	ACLK to Bn Propagation Delay (Latch Mode)	CD=RBYP=0V, T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			1	9	nS	9, 10, 11
tPLHCK	ACLK to Bn Propagation Delay (Latch Mode)	CD=RBYP=0V, T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			1	8	nS	9, 10, 11
tPHLCD	CD to Bn: Enable Time	AN=3V, T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			2	12	nS	9, 10, 11
tPLHCD	CD to Bn: Disable Time	T/$\overline{R}$=3V, An=3V, RL=12.5 Ohm, CL=30pF			2	9	nS	9, 10, 11
tPHLTR	T/$\overline{R}$ to Bn: Enable Time	CD=0V, RBYP=3V			8	25	nS	9, 10, 11
tPLHTR	T/$\overline{R}$ to Bn: Disable Time	CD=0V, RBYP=3V			3	12	nS	9, 10, 11
tR	Transition Time 20% to 80%	CD=RBYP=0V, T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			1	4	nS	9, 10, 11
tF	Transition Time 80% to 20%	CD=RBYP=0V, T/$\overline{R}$=3V, RL=12.5 Ohm, CL=30pF			1	4	nS	9, 10, 11
SR	Slew Rate from 1.3 to 1.8V	CD=RBYP=0V, T/$\overline{R}$=3V			1		nS	9, 10, 11
tskewD	Skew	An to Bn				5	nS	9, 10, 11
		ACLK to Bn				5	nS	9, 10, 11

AC PARAMETERS: DRIVER TIMING REQUIREMENTS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

tsD	An to ACLK Setup Time					3	nS	9, 10, 11
thD	An to ACLK Hold Time					3	nS	9, 10, 11
tpwD	ACLK Pulse Width					3	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS: RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLB	Bn to An Propagation Delay (Bypass Mode)	LE=3V, CD=T/$\overline{R}$=0V, RL=1k, CL=50pF			2	9	nS	9, 10, 11
tPLHB	Bn to An Propagation Delay (Bypass Mode)	CD=T/$\overline{R}$=0V, LE=3V, CL=30pF			2	9	nS	9, 10, 11
tPHLLE	LE to An Propagation Delay (Latch Mode)	CD=T/$\overline{R}$=0V, RL=1k, CL=50pF			3	11	nS	9, 10, 11
tPLHLE	LE to An Propagation Delay (Latch Mode)	CD=T/$\overline{R}$=0V, CL=50pF			3	11	nS	9, 10, 11
tPLZCD	CD to An: Disable Time	LE=3V, Bn=2.1V, T/$\overline{R}$=0V, RL=500 Ohm, CL=50pF			1	18	nS	9, 10, 11
tPZLCD	CD to An: Enable Time	Bn=2.1V, T/$\overline{R}$=0V, LE=3V, RL=500 Ohm, CL=50pF			3	13	nS	9, 10, 11
tPHZCD	CD to An: Disable Time	LE=3V, Bn=1.1V, T/$\overline{R}$=0V, RL=500 Ohm, CL=50pF			3	11	nS	9, 10, 11
tPZHCD	CD to An: Enable Time	Bn=1.1V, T/$\overline{R}$=0V, RL=500 Ohm, CL=50pF			3	11	nS	9, 10, 11
tPLZTR	T/$\overline{R}$ to An: Disable Time	LE=3V, CD=0V			3	18	nS	9, 10, 11
tPZLTR	T/$\overline{R}$ to An: ENable Time	LE=3V, CD=0V			3	18	nS	9, 10, 11
tPHZTR	Disable Time	LE=3V, Bn=1.1V, CD=0V, RL=500 Ohm, CL=50pF			3	11	nS	9, 10, 11
tPZHTR	T/$\overline{R}$ to An Enable Time	CD=0V, LE=3V, Bn=1.1V, RL=500 Ohm, CL=50pF			3	11	nS	9, 10, 11
tskewR	Skew	Bn to An	3			5	nS	9, 10, 11
		LE to An	3			5	nS	9, 10, 11

AC PARAMETERS: RECEIVER TIMING REQUIREMENTS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

tsBn	Bn to LE Set-up Time	CD = T/$\overline{R}$ = 0V				3	nS	9, 10, 11
thLe	LE to Bn Hold Time	CD = T/$\overline{R}$ = 0V				3	nS	9, 10, 11
tpwLE	LE Pulse Width	CD = T/$\overline{R}$ = 0V				5	nS	9, 10, 11

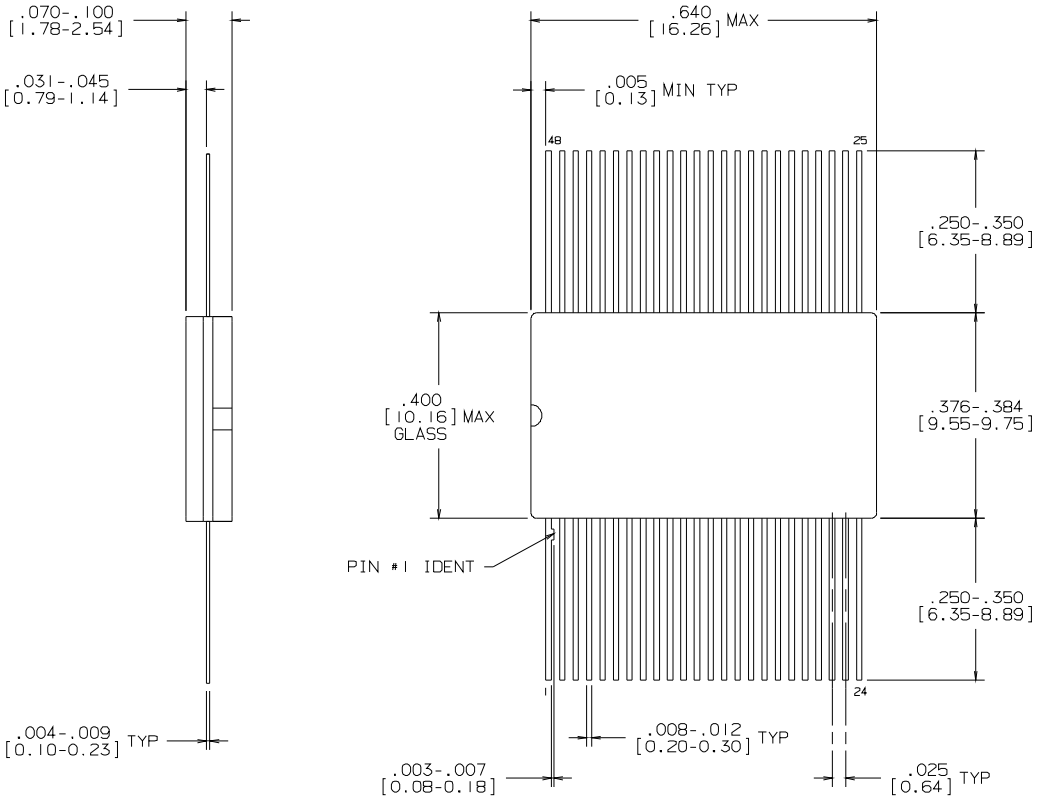
Note 1: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of pkg.
Note 2: Only one output at a time should be shorted, and duration of the short should not exceed one second.
Note 3: tskew is an absolute value defined as differences seen in prop delaysbetween drivers/receivers in the same pkg.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
6300HRC1	CERPAC, 48 LEAD, .025 LEAD PITCH (B/I CKT)
WA48ARB	CERPAC, 48 LEAD, .025 LEAD PITCH (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	09283	08/11/92	MS/SL
B	DIM .003-.007[0.08-0.18] WAS .006-.010[0.15-0.25]; DIM .031-.045[0.79-1.14] WAS .040-.054[1.02-1.37]	09489	01/25/93	MS/



MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES/ 5.08 MICROMETERS MINIMUM SOLDER
   MEASURED AT THE CREST OF THE MAJOR FLATS.
2. THE LEAD FINISH, NICKEL UNDERPLATE, AND BASIS METAL
   SHALL CONFORM TO THE REQUIREMENTS OF MIL-M-38510.
3. REFERENCE JEDEC METRIC BALLOT JC-11.10-92-75, ITEM 10-320,
   VARIATION AA, DATED JULY 9,1992.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN MARTA SUCHY	08/11/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERPAC, 48 LEAD,
.025 LEAD PITCH

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-WA48A	B

DO NOT SCALE DRAWING | SHEET 1 OF 1