MICROCIRCUIT DATA SHEET

MNDS90LV031A-X REV 0A0

Original Creation Date: 02/09/99
Last Update Date: 07/30/99
Last Major Revision Date:

3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031A is a quad CMOS differential line driver utilizing Low Voltage Differentional Signaling (LVDS) technology. It is designed for applications requiring low power dissipation and high data rates.

The DS90LV031A accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output siginals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to a low idle power state.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Industry Part Number

DS90LV031A

NS Part Numbers

DS90LV031AW-QML

Prime Die

DS90LV031A

Controlling Document

5962-9865101QFA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 3.3V power supply design
- +/- 350mV differential signaling
- Low power dissipation.
- Low differential skew.
- Low propagation delay
- Interoperable with existing 5V LVDS devices
- Military operating temprature range
- Pin compatible with DS26C31.
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with proposed TIA/EIA-644 LVDS standard
- Typical Rise/Fall times of 800pS.
- Typical Tri-State Enable/Disable Delays of less than 5nS.

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.3 to +4V
Input Voltage (Din)	-0.3 to (Vcc+0.3V)
Enable Input Voltage (EN, EN*)	-0.3 to (Vcc+0.3V)
Output Voltage (Dout+, Dout-)	-0.3 to +3.9V
Storage Temperature Range	-65C to +150C
Lead Temperature Soldering (4 sec)	260C
ESD Rating.	6000 Volts.
Maximum Junction Temperature	+150C
Maximum Power Dissipation @ +25C (Note 2)	845mW
Thermal Resistance	
(Theta Ja)	148C/W
(Theta Jc)	22C/W

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Derate at 6.8mW/C for temperatures above +25C.

Recommended Operating Conditions

Supply Voltage	3.0 to 3.6V
Operating Free Air Temperature	-55 to +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 3.0/3.6V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vod1	Differential Ouput Voltage	RL = 100 Ohms		Dout-, Dout+	250	450	mV	1, 2, 3
DVod1	Change in Magnitude of Vod1 for complementary output States	RL = 100 Ohms		Dout-, Dout+		50	mV	1, 2, 3
Vos	Offset Voltage	RL = 100 Ohms		Dout-, Dout+	1.125	1.625	V	1, 2, 3
DVos	Change in Magnitude of Vos for Complementary Output States	RL = 100 Ohms		Dout-, Dout+		50	mV	1, 2, 3
Voh	Output Voltage High	RL = 100 Ohms		Dout-, Dout+		1.85	V	1, 2, 3
Vol	Output Voltage Low	RL = 100 Ohms		Dout-, Dout+	.9		V	1, 2, 3
Vih	Input Voltage High		1	Din, EN, EN*	2.0	Vcc	V	1, 2, 3
Vil	Input Voltage Low		1	Din, EN, EN*	Gnd	0.8	V	1, 2, 3
IIH	Input Current	Vin = Vcc or 2.5V, Vcc = 3.6V		Din, EN, EN*		±10	uA	1, 2, 3
IIL	Input Current	Vin = Gnd or 0.4V, Vcc = 3.6V		Din, EN, EN*		±10	uA	1, 2, 3
Vcl	Input Clamp Voltage	Icl = -8mA, Vcc = 3.0V		Din, EN, EN*		-1.5	V	1, 2, 3
Ios	Output Short Circuit Current	ENABLED Din = Vcc, Dout + = 0V or Din = Gnd, Dout- = 0V		Dout-, Dout+		-9.0	mA	1, 2, 3
Ioff	Power-off Leakage	Vout = 0V or 3.6V Vcc = 0V or Vcc = Open		Dout-, Dout+		±20	uA	1, 2, 3
Ioz	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V VOUT = 0V or VCC, VCC = 3.6V		Dout-, Dout+		±10	uA	1, 2, 3
Icc	No Load Drivers Enabled Supply Current	Din = Vcc or Gnd		Vcc		18	mA	1, 2, 3
Iccl	Loaded Drivers Enabled Supply Current	Rl = 100 ohms All Channels, Din = Vcc or Gnd (all inputs)		Vcc		35	mA	1, 2, 3
Iccz	Loaded or No Load Drivers Disabled Supply Current	Din = Vcc or Gnd, En = Gnd, En* = Vcc		Vcc		12	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VCC = 3.0/3.3/3.6V, RL = 100 Ohms, CL = 20pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLD	Differential Propagation Delay High to Low				0.3	3.5	ns	9, 10, 11
tPLHD	Differential Propagation Delay Low to High				0.3	3.5	ns	9, 10, 11
tSKD	Differential Skew tPHLD-tPLHD					1.5	ns	9, 10, 11
tSK1	Channel to Channel Skew		2			1.75	ns	9, 10, 11
tSK2	Chip to Chip Skew		3			3.2	ns	9, 10, 11

Note 1: Tested during VOH/VOL tests.
Note 2: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
Note 3: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

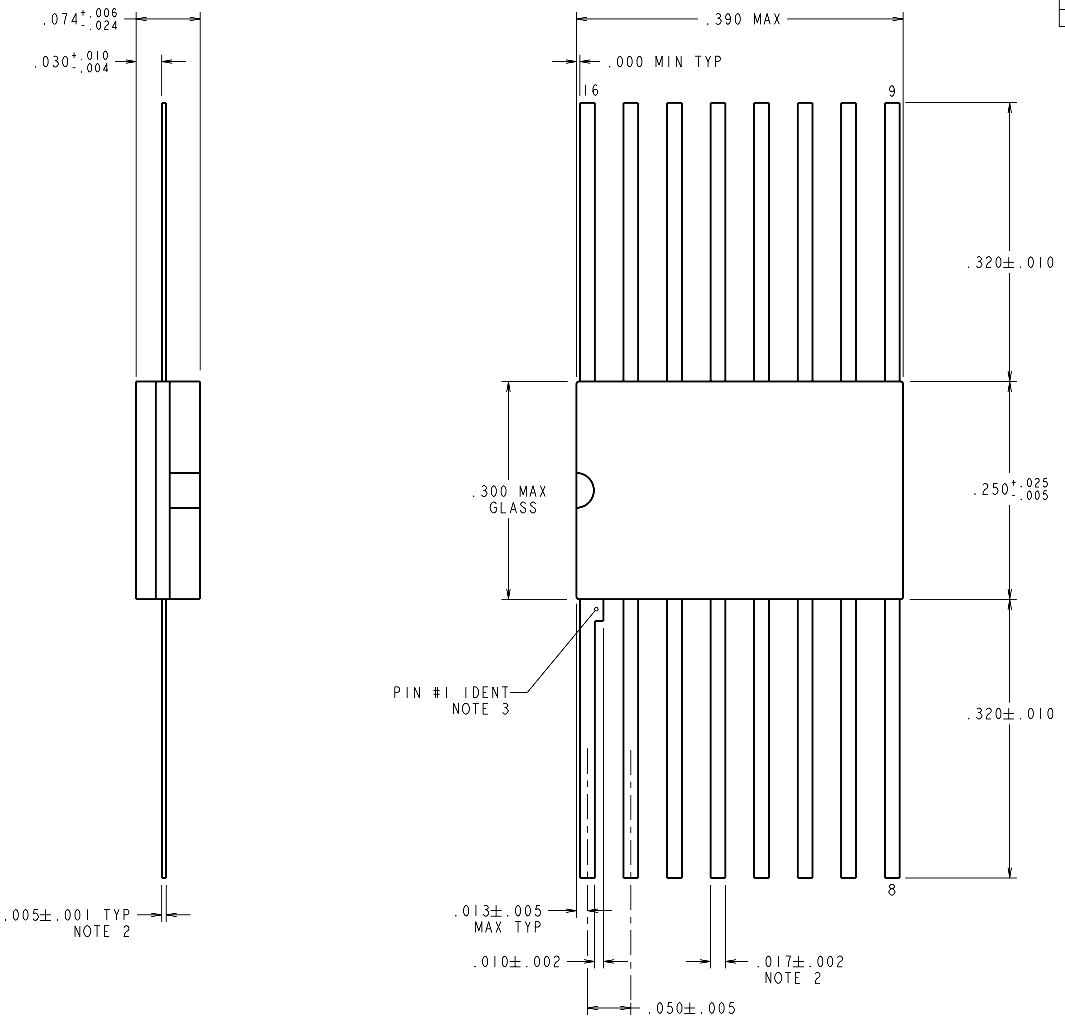
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003265	07/30/99	Mike Fitzgerald	Initial MDS Release