National Semiconductor

MILITARY DATA SHEET

MNLM139-X REV 0A0

Original Creation Date: 09/13/95
Last Update Date: 06/28/96
Last Major Revision Date: 09/13/95

LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

General Description

The LM139 consists of four independent precision voltage comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and the time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic-where the low power drain of the LM139 is a distinct advantage over standard comparators.

Industry Part Number

LM139

Prime Die

LM139F

NS Part Numbers

LM139E/883
LM139F-MLS
LM139J/883
LM139W-MLS
LM139W/883
LM139WG/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range
  2Vdc to 36Vdc or ±1Vdc to ±18Vdc
- Very low supply current drain (0.8mA) - independent of supply voltage
- Low input biasing current 25nA
- Low input offset current ±5nA
  and offset voltage ±3mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250mV at 4mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage, V+		36 Vdc or ± 18 Vdc
Differential Input Voltage (Note 5)		36 Vdc
Input Voltage		-0.3 Vdc to +36 Vdc
Input Current (Vin < -0.3 Vdc) (Note 6)		50mA
Power Dissipation (Note 2, 3)		
LCC		1250mW
CERDIP		1200mW
CERPACK		680mW
CERAMIC S.O.I.C.		680mW
Output Short-Circuit to GND (Note 4)		Continuous
Maximum Junction Temperature		150 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		260 C
Operating Temperature Range		-55 C to +125 C
Thermal Resistance		
ThetaJA		
LCC	(Still Air)	100 C/W
	(500LF/Min Air flow)	73 C/W
CERDIP	(Still Air)	103 C/W
	(500LF/Min Air flow)	65 C/W
CERPACK	(Still Air)	183 C/W
	(500LF/Min Air flow)	120 C/W
CERAMIC S.O.I.C.	(Still Air)	183 C/W
	(500LF/Min Air flow)	120 C/W
ThetaJC		
LCC		28 C/W
CERDIP		23 C/W
CERPACK		23 C/W
CERAMIC S.O.I.C.		23 C/W
ESD Tolerance (Note 7)		600V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade

Note 2: Maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100mW), provided the output transistors are allowed to saturate.

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.

(Continued)

Note 5: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains witin the common-mode range, the comparator will provide a proper output state. The low input voltge state must not be less than -3.0 Vdc (or 0.3 Vdc below the magnitude of the negative power supply, if used) (at 25 C).

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and therby acting as input diode clamps. In addition to the diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 Vdc (at 25 C).

Note 7: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	Rl = Infinity				2	mA	1, 2, 3
		V+ = 30V, Rl = Infinity				2	mA	1, 2, 3
Vio	Input Offset Voltage	V+ = 30V			-5	5	mV	1
					-9	9	mV	2, 3
		V+ = 30V, Vcm = 28.5V			-5	5	mV	1
		V+ = 30V, Vcm = 28.0V			-9	9	mV	2, 3
					-5	5	mV	1
					-9	9	mV	2, 3
CMRR	Common Mode Rejection Ratio	V+ = 30V, Vcm = 0V to 28.5V			60		dB	1
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V			60		dB	1
+Ibias	Input Bias Current	Vo = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
-Ibias	Input Bias Current	Vo = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
Iio	Input Offset Current	Vo = 1.5V			-25	25	nA	1
					-100	100	nA	2, 3
Icex	Output Leakage Current	V+ = 30V, Vo = 30V				1	uA	1, 2, 3
Isink	Output Sink Current	Vo = 1.5V			6		mA	1
Vsat	Saturation Voltage	Isink = 4mA				400	mV	1
						700	mV	2, 3
Av	Voltage Gain	V+ = 15V, Rl $\geq$ 15K Ohms, Vin = 1V to 11V			50		V/mV	1
Vcm	Common Mode Voltage Range	V+ = 30V	1		0	V+ - 1.5	V	1
			1		0	V+ - 2.0	V	2, 3
Vdiff	Differential Input Voltage	V+ = 30V, Vdiff = 36V	2			500	nA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = 5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tRLH	Response Time	Vod = 5mV				5	uS	9
		Vod = 50mV				.8	uS	9
tRHL	Response Time	Vod = 5mV				2.5	uS	9
		Vod = 50mV				.8	uS	9

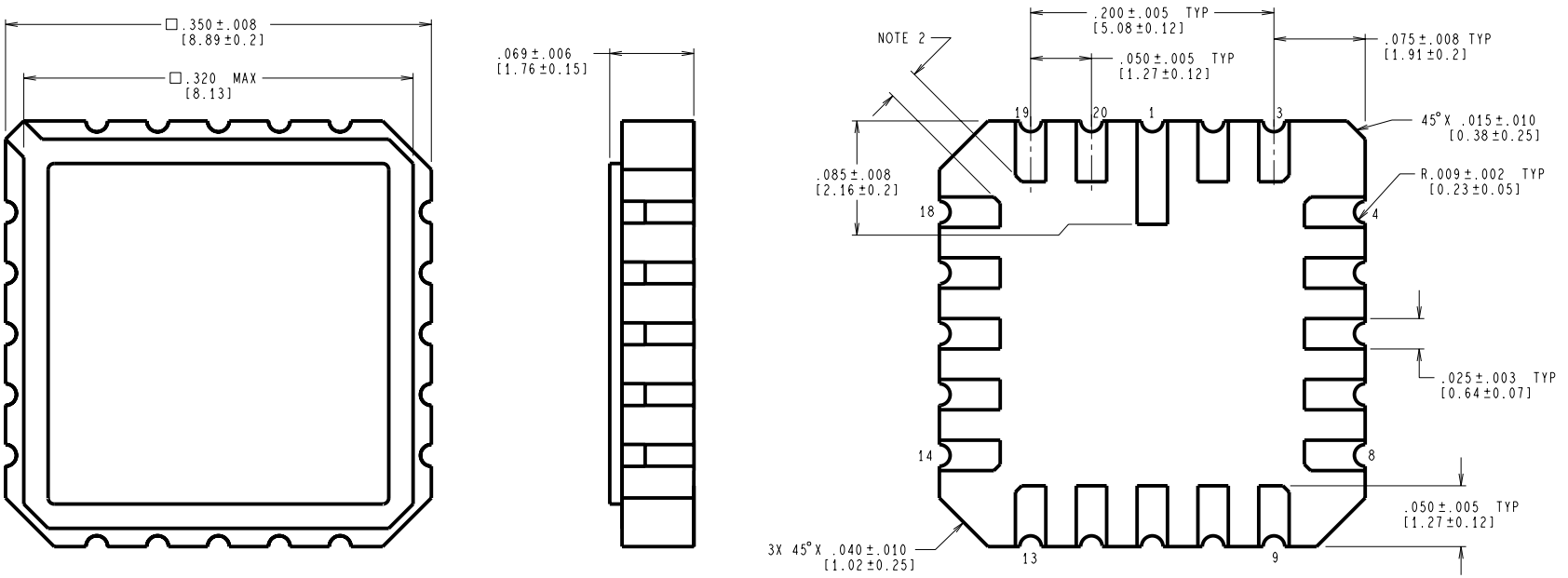
Note 1: Parameter guaranteed by Vio tests.
Note 2: Vdiff is measured by applying +36V/-36V, with reference to gnd, to the two inputs.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W14BRN	CERPAC (W), 14 LEAD (P/P DWG)
WG14ARB	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

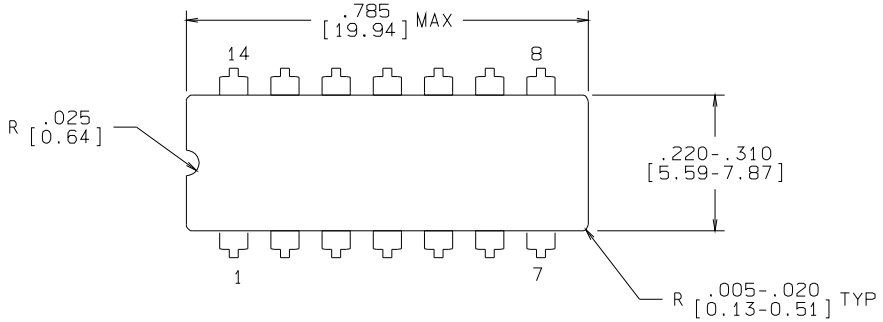
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

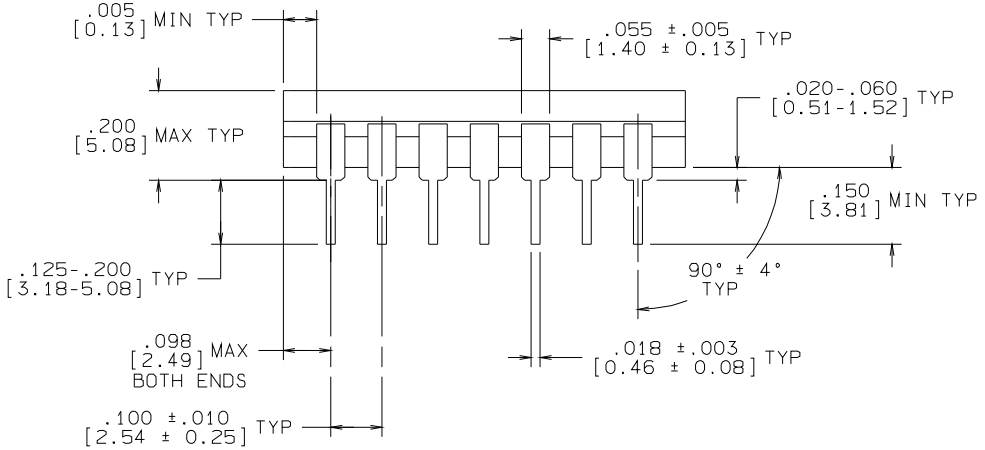
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

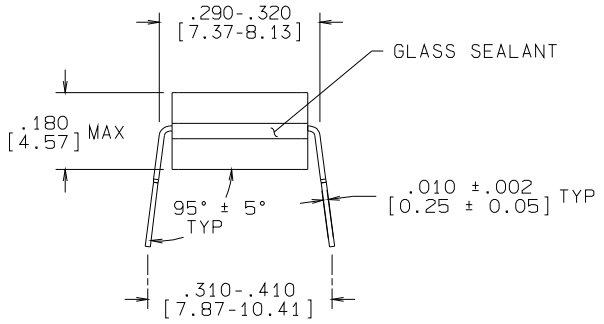
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH [MM]

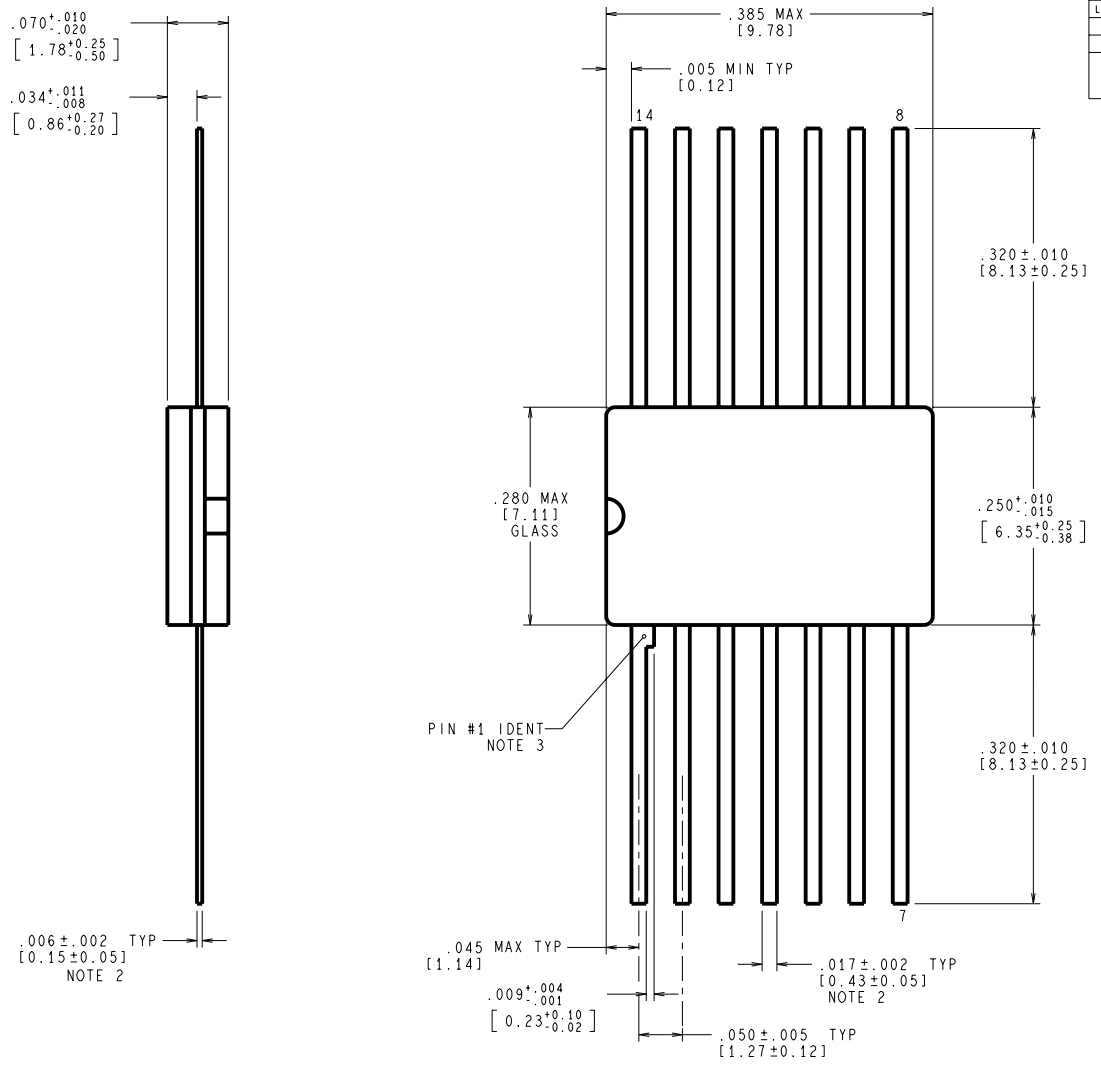
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

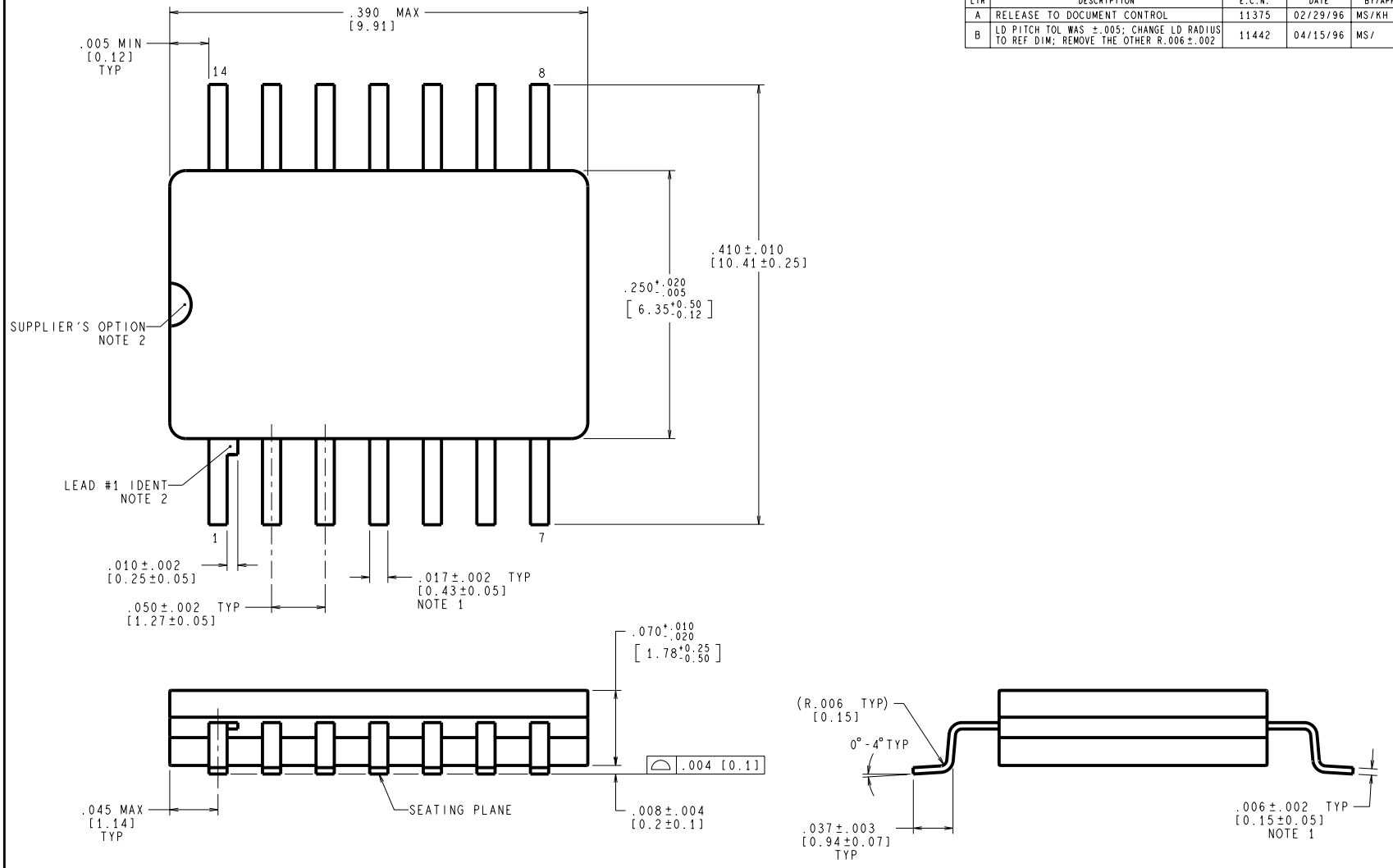
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/96	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002	11442	04/15/96	MS/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
14 LEAD,
GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-WG14A	B

DO NOT SCALE DRAWING | SHEET 1 of 1