

**MC100EPT23**



**SO-8, D SUFFIX**  
8-LEAD PLASTIC SOIC PACKAGE  
CASE 751

**ORDERING INFORMATION**  
MC100EPT23D SOIC

**ECLIPS Plus™**

*Product Preview*

**Dual Differential LVPECL  
to LVTTTL Translator**

- 2.0ns Typical Propagation Delay
- Maximum Frequency > 275MHz
- Differential LVPECL Inputs
- Small Outline SOIC Package
- 24mA LVTTTL Outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on  $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1.2KV HBM, >150V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 91 devices

**PIN DESCRIPTION**

PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D0, D1, $\overline{D0}$ , $\overline{D1}$	Diff LVPECL Inputs
VCC	Positive Supply
GND	Ground

The MC100EPT23 is a dual differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package and the dual gate design of the EPT23 makes it ideal for applications which require the translation of a clock and a data signal.

The EPT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external  $V_{BB}$  reference, the EPT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100EPT23 can accept any standard differential LVPECL input referenced from a  $V_{CC}$  of +3.3V.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

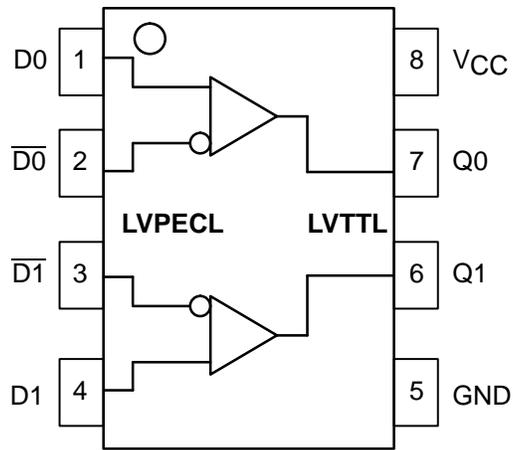


Figure 1. 8-Lead Pinout and Logic Diagram

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit	
$V_{CC}$	Power Supply (GND = 0V)	0 to 3.8	VDC	
$V_I$	Input Voltage (GND = 0V, $V_I$ not more positive than $V_{CC}$ )	0 to 3.8	VDC	
$I_{out}$	Output Current	Continuous Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C	
$T_{stg}$	Storage Temperature	-65 to +150	°C	
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	Still Air 500lfpm	190 130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%		°C/W
$T_{sol}$	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C	

\* Maximum Ratings are those values beyond which damage to the device may occur.

**DC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 0.3V$ ;  $GND = 0V$ ;  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CCH}$	Power Supply Current (Outputs set to HIGH)	TBD	20	TBD	mA
$I_{CCL}$	Power Supply Current (Outputs set to LOW)	TBD	28	TBD	mA
$V_{IH}$	Input HIGH Voltage ( $V_{CC} = 3.3$ ) (Note 1.)	2135		2420	mV
$V_{IL}$	Input LOW Voltage ( $V_{CC} = 3.3$ ) (Note 1.)	1490		1825	mV
$I_{IH}$	Input HIGH Current			150	$\mu A$
$I_{IL}$	Input LOW Current	$\frac{D}{\bar{D}}$			$\mu A$
$V_{OH}$	Output HIGH Voltage ( $I_{OH} = -3.0mA$ ) (Note 2.)	2.4			V
$V_{OL}$	Output LOW Voltage ( $I_{OL} = 24mA$ ) (Note 2.)			0.5	V
$I_{OS}$	Output Short Circuit Current	-80		-130	mA
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

- All values vary 1:1 with  $V_{CC}$ .
- All loading with 500 ohms to GND,  $CL = 20pF$ .
- $V_{IHCMR}$  min varies 1:1 with GND, max varies 1:1 with  $V_{CC}$ .

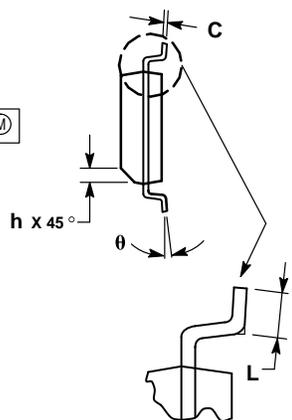
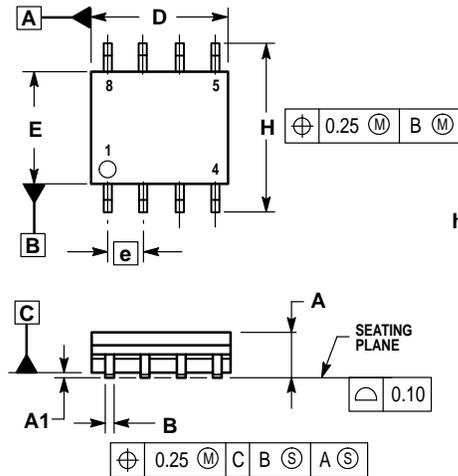
**AC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 0.3V$ ;  $GND = 0V$ )

Symbol	Characteristic	$-40^{\circ}C$			$25^{\circ}C$			$85^{\circ}C$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency (Note 4.)	275			275			275			MHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	1.0	1.7		1.0	1.7		1.0	1.7		ns
$t_{SK++}$ , $t_{SK--}$ , $t_{SKPP}$	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Voltage Swing (Differential) (Note 6.)	100	800	1200	100	800	1200	100	800	1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) $Q, \bar{Q}$	330		700	330		700	330		700	ps

- $F_{max}$  guaranteed for functionality only.  $V_{OL}$  and  $V_{OH}$  levels are guaranteed at DC only.
- Skews are measured between outputs under identical transitions.
- 200mV input guarantees full logic swing at the output.

OUTLINE DIMENSIONS

SO-8, D SUFFIX  
 PLASTIC SOIC PACKAGE  
 CASE 751-06  
 ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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