MOTOROLA

MC33291

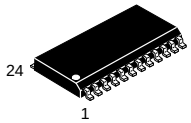
Basic Octal Serial Switch with Serial Peripheral Interface I/O

BASIC OCTAL SERIAL SWITCH (SPI Input/Output)

SEMICONDUCTOR TECHNICAL DATA

The MC33291 is an eight output low side power switch with 8–bit serial input control. The MC33291 is a versatile circuit designed for automotive applications, but is well suited for other environments. The MC33291 incorporates *SMARTMOS*™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The MC33291 interfaces directly with a microcontroller to control various inductive or incandescent loads. The circuit's innovative monitoring and protection features are: very low standby current, SPI cascadable fault reporting, internal 53 V clamp on each output, output specific diagnostics, and independent shutdown of outputs. The device is parametrically specified over an ambient temperature range of $-40°C \le T_A \le 125°C$ and $9.0\ V \le V_{PWR} \le 16\ V$ supply. The economical SO–24 wide body surface mount plastic packages make the MC33291 a very cost effective solution for many applications.

- Designed to Operate Over Wide Supply Voltages of 5.5 to 26.5 V
- Interfaces Directly with Microprocessor Using 8–Bit SPI I/O Protocol to 3.0 MHz
- 1.0 A Peak Current Outputs with Maximum $R_{DS(on)}$ of 1.2 Ω at $T_J = 150°C$
- Outputs Current Limited to 1.0 to 3.0 A for Switching Incandescent Loads
- Output Voltages Clamped to 53 V During Inductive Switching
- Maximum Sleep Current (I_{PWR}) of 25 μA with $\overline{\text{Reset}}$ Low
- Maximum of 4.0 mA I_{DD} During Operation
- Maximum of 2.0 mA I_{PWR} During Operation with All Outputs ON
- Open Load Detection (Outputs OFF)
- Overvoltage Detection and Shutdown
- Outputs have Independent Over Temperature Detection and Shutdown
- Output Mode Programmable for Sustained Current Limit or Shutdown
- Independent Output Short Circuit Detect and Latch–Off for Every Write Cycle
- Designed for –40 to 125°C Ambient Temperature Operation

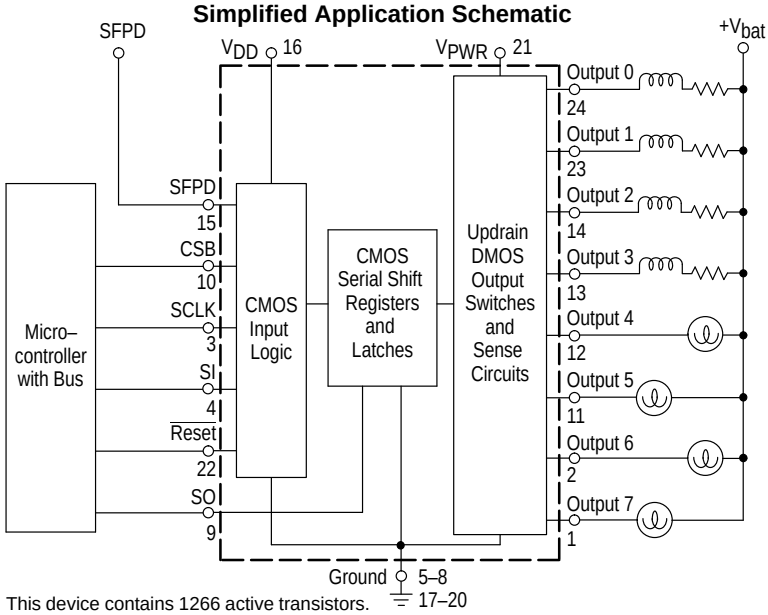


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
SOP (16+4+4)L

PIN CONNECTIONS

SOP–24L	Function
1	Output 7
2	Output 6
3	SCLK
4	SI
5	Ground
6	Ground
7	Ground
8	Ground
9	SO
10	CSB
11	Output 5
12	Output 4
13	Output 3
14	Output 2
15	SFPD
16	V_{DD}
17	Ground
18	Ground
19	Ground
20	Ground
21	V_{PWR}
22	$\overline{\text{Reset}}$
23	Output 1
24	Output 0

Simplified Application Schematic

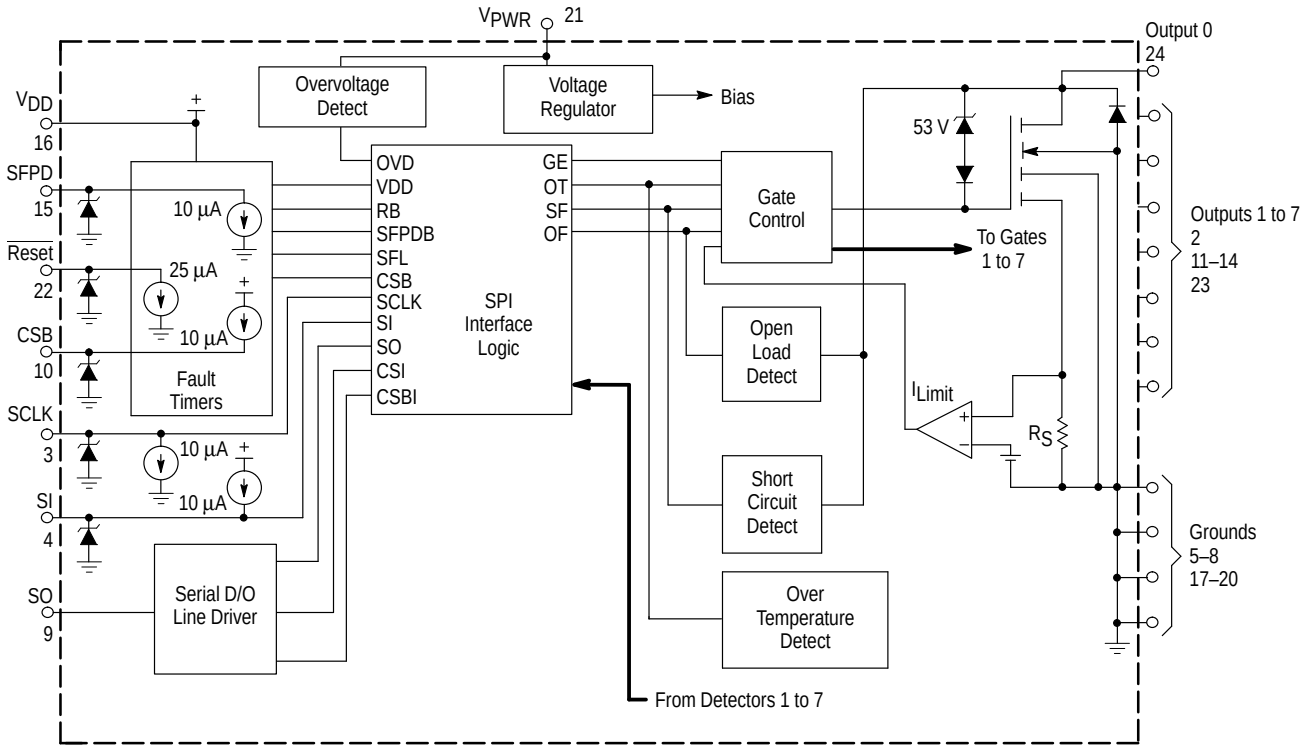


This device contains 1266 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33291DW	$T_C = –40$ to 125°C	SOP–24L

Figure 1. Internal Block Diagram



FAULT OPERATION

SERIAL OUTPUT (SO) PIN REPORTS

Overvoltage	Overvoltage condition reported.
Over Temperature	Fault reported by Serial Output (SO) pin.
Over Current	SO pin reports short to battery/supply or over current condition.
Output ON, Open Load Fault	Not reported.
Output OFF, Open Load Fault	SO pin reports output OFF open load condition.

DEVICE SHUTDOWNS

Overvoltage	Total device shutdown at V_{PWR} = 28 to 36 V. All outputs are latched off and SPI register is reset (cleared). Outputs can be turned back on with a new SPI command after V_{PWR} has decayed below 26.5 V.
Over Temperature	Only the output experiencing an over temperature condition turns off.
Over Current	Only the output experiencing an over current condition shuts down at 1.0 to 3.0 A after a 70 to 250 µs delay, with SFPD pin grounded. All other outputs will continue to operate in a current limit mode, with no shutdown, if the SPFD pin is at 5.0 V (so long as the individual outputs are not experiencing thermal limit conditions).

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage Steady–State Transient Conditions (Note 1)	 $V_{PWR(sus)}$ $V_{PWR(pk)}$	 –1.5 to 26.5 –13 to 60	 V V
Logic Supply Voltage (Note 2)	V_{DD}	–0.3 to 7.0	V
Input Pin Voltage (Note 3)	V_{IN}	–0.3 to 7.0	V
Output Clamp Voltage (Note 4) (5.0 mA ≤ I_{out} ≤ 0.5 A)	$V_{OUT(off)}$	 45 to 65	V
Output Self Limit Current	$I_{OUT(lim)}$	1.0 to 3.0	A
Continuous Per Output Current (Note 5)	$I_{OUT(cont)}$	500	mA
ESD Voltage (Note 6) Human Body Model (Note 7) Machine Model (Note 8)	 V_{ESD1} V_{ESD2}	 2000 200	 V V
Output Clamp Energy (Note 9)	E_{clamp}	50	mJ
Recommended Frequency of SPI Operation	f_{SPI}	3.0	MHz
Storage Temperature	T_{stg}	–55 to 150	°C
Operating Case Temperature	T_C	–40 to 125	°C
Operating Junction Temperature	T_J	–40 to 150	°C
Power Dissipation (T_A = 25°C) (Note 10)	P_D	2.0	W
Lead Soldering Temperature (Note 13)	T_{solder}	260	°C
Thermal Resistance (Junction–to–Ambient) SO–24 Package All Outputs ON (Note 11) Single Output ON (Note 12)	$R_{\theta JA}$	 45 60	°C/W

NOTES:
1. Transient capability with external 100 Ω resistor connected in series with V_{PWR} pin and supply.
2. Exceeding these limits may cause a malfunction or permanent damage to the device.
3. Exceeding these limits on SCLK, SI, CSB, SFPD, or $\overline{\text{Reset}}$ pins may cause permanent damage to the device.
4. With output OFF.
5. Continuous output rating so long as maximum junction temperature is not exceeded. Operation at 125°C ambient temperature will require maximum output current computation using package $R_{\theta JA}$.
6. ESD data available upon request.
7. ESD1 testing is performed in accordance with the Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
8. ESD2 testing is performed in accordance with the Machine Model (C_{Zap} = 100 pF, R_{Zap} = 0 Ω).
9. Maximum ouput clamp energy capability at 150°C junction temperature using single non–repetitive pulse method.
10. Maximum power dissipation at indicated junction temperature with no heat sink used.
11. Thermal resistance from Junction–to–Ambient with all outputs ON and dissipating equal power.
12. Thermal resistance from Junction–to–Ambient with a single output ON.
13. Lead soldering temperature limit is for 10 seconds maximum duration; contact Motorola Sales Office for device immersion soldering time/temperature limits.

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{Bat} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range					V
Quasi–Functional (Note 1)	$V_{PWR(qf)}$	5.5	–	9.0	
Fully Operational	$V_{PWR(fo)}$	9.0	–	26.5	
Supply Current (All Outputs ON, I_{out} = 0.5 A)	$I_{PWR(on)}$	–	1.0	2.0	mA
Sleep State Supply Current at $\overline{Reset}$ ≤ 0.2 V_{DD} and/or V_{DD} < 0.5 V	$I_{PWR(ss)}$	–	1.0	25	µA
Sleep State Output Leakage Current (Per Output, $\overline{Reset}$ = 0)	$I_{OUT(ss)}$	–	1.0	25	µA
Overvoltage Shutdown	V_{OV}	28	32	36	V
Overvoltage Shutdown Hysteresis (Note 2)	$V_{OV(hys)}$	0.2	0.8	1.5	V
Logic Supply Voltage	V_{DD}	4.5	–	5.5	V
Logic Supply Current (Note 3)	I_{DD}				
$\overline{Reset}$ ≥ 0.7 V_{DD}		–	1.0	4.0	mA
$\overline{Reset}$ ≤ 0.5 V		–	–	25	µA
Logic Supply Undervoltage Lockout Threshold (Note 4)	$V_{DD(uvlo)}$	2.5	–	3.5	V
POWER OUTPUT					
Drain–to–Source ON Resistance (I_{out} = 0.5 A, T_J = 25°C)	$R_{DS(on)}$				Ω
V_{PWR} = 5.5 V		–	–	2.0	
V_{PWR} = 9.0 V		–	0.9	1.2	
V_{PWR} = 13 V		–	0.7	1.0	
Drain–to–Source ON Resistance (I_{out} = 0.5 A, T_J = 150°C)	$R_{DS(on)}$				Ω
V_{PWR} = 5.5 V		–	–	3.0	
V_{PWR} = 9.0 V		–	1.2	1.6	
V_{PWR} = 13 V		–	1.0	1.2	
Output Self Limiting Current	$I_{OUT(lim)}$				A
Outputs Programmed ON, V_{out} = 0.6 V_{DD}		1.0	2.0	3.0	
Output Fault Detect Threshold (Note 5)	$V_{OUTth(F)}$				V
Output Programmed OFF		2.5	3.0	3.5	
Output OFF Open Load Detect Current (Note 6)	I_{OCO}				µA
Output Programmed OFF, V_{out} = 0.6 V_{DD}		30	50	100	
Output Clamp Voltage	V_{OK}				V
2.0 mA ≤ I_{out} ≤ 200 mA		45	53	65	
Output Leakage Current (V_{DD} ≤ 2.0 V) (Note 7)	$I_{OUT(lkg)}$	–25	0	25	µA
Over Temperature Shutdown (Outputs OFF) (Note 2)	T_{LIM}	155	180	–	°C
Over Temperature Shutdown Hysteresis (Note 2)	$T_{LIM(hys)}$	–	10	20	°C

NOTES: 1. SPI inputs and outputs operational; Fault status reporting may not be fully operational within this voltage range. Outputs will remain operational somewhat below this V_{PWR} range but $R_{DS(on)}$ will increase, causing power dissipation to increase. Outputs will re–establish their instructed state following a V_{PWR} interruption so long as V_{DD} remains non–interrupted.
2. This parameter is guaranteed by design but is not production tested.
3. Measured with the $\overline{Reset}$ pin held at a logic high state; outputs can be OFF or ON or in any combination thereof.
4. Device incorporates a power–on reset function; For V_{DD} less than the Undervoltage Lockout Threshold voltage, all data registers are reset and all outputs are disabled.
5. Output Fault Detect Threshold with outputs programmed OFF. Output fault detect thresholds are the same for output opens and shorts.
6. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded to be OFF.
7. Output leakage current measured with the output OFF and at 16 V.

STATIC ELECTRICAL CHARACTERISTICS (continued) (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{Bat} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic High Voltage (Note 1)	V_{IH}	0.7	–	1.0	V_{DD}
Input Logic Low Voltage (Note 1)	V_{IL}	0	–	0.2	V_{DD}
Input Logic Voltage Hysteresis (SCLK, $\overline{\text{Reset}}$, and SFPD) (Note 2)	$V_{I(hys)}$	50	100	500	mV
SI Pull–Up Current (SI = 0 V)	I_{SI}	0	10	20	µA
CSB Pull–Up Current (CSB = 0 V)	I_{CSB}	0	10	20	µA
SCLK Pull–Down Current (SCLK = 5.0 V)	I_{SCLK}	0	10	20	µA
$\overline{\text{Reset}}$ Pull–Down Current ($\overline{\text{Reset}}$ = 5.0 V)	I_{RSTB}	5.0	25	50	µA
SFPD Pull–Down Current (SFPD = 5.0 V)	I_{SFPD}	5.0	10	25	µA
SO High State Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD} – 0.4V	V_{DD} – 0.2 V	–	V
SO Low State Output Voltage (I_{OL} = –1.6 mA)	V_{SOL}	–	0.2	0.4	V
SO Tri–State Leakage Current (CSB = 0.7 V_{DD}, 0 V ≤ V_{SO} ≤ V_{DD})	I_{SOT}	–10	0	10	µA
Input Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) (Note 3)	C_{IN}	–	–	12	pF
SO Tri–State Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) (Note 4)	C_{SOT}	–	–	20	pF

NOTES: 1. Upper and lower logic threshold voltage levels apply to SI, CSB, SCLK, $\overline{\text{Reset}}$, and SFPD inputs.
2. Hysteresis is characterized but not production tested.
3. Input capacitance of SI, CSB, SCLK, $\overline{\text{Reset}}$, and SFPD for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design but is not production tested.
4. Tri–state capacitance of SO for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{Bat} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rise Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_r	0.4	5.0	20	µs
Output Fall Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_f	0.4	5.0	20	µs
Output Turn ON Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 2)	$t_{dly(on)}$	1.0	15	50	µs
Output Turn OFF Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 3)	$t_{dly(off)}$	1.0	15	50	µs
Output Short Fault Disable Report Delay (Note 4) SFPD = 0.2 × V_{DD}	$t_{dly(sf)}$	70	150	250	µs
Output OFF Fault Report Delay (Note 5) SFPD = 0.2 × V_{DD}	$t_{dly(off)}$	70	150	250	µs

NOTES: 1. Output Rise and Fall time respectively measured across a 26 Ω resistive load at 10% to 90% and 90% to 10% voltage points.
2. Output Turn ON Delay time measured from 50% rising edge of CSB to 90% of Output OFF voltage (V_{PWR}) with R_L = 26 Ω resistive load.
3. Output Turn OFF Delay time measured from 50% rising edge of CSB to 10% of Output OFF voltage (V_{PWR}) with R_L = 26 Ω resistive load.
4. Propagation time of Short Fault Disable Report measured from 50% rising edge of CSB to 10% Output OFF voltage (V_{PWR}), V_{PWR} = 6.0 V, and SFPD = 0.2 × V_{DD}.
5. Output OFF Fault Report Delay measured from 50% rising edge of CSB to 10% rising edge of Output OFF voltage (V_{PWR}).

DYNAMIC ELECTRICAL CHARACTERISTICS (continued) (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, –40°C ≤ T_C ≤ 125°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{Bat} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING					
Required Low State Duration for $\overline{\text{Reset}}$ (V_{IL} ≤ 0.2 V_{DD}) (Note 1)	$t_{w(RSTB)}$	–	50	167	ns
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	t_{lead}	–	50	167	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)	t_{lag}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time)	$t_{SI(su)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Hold Time)	$t_{SI(hold)}$	–	25	83	ns
SO Rise Time (C_L = 200 pF)	$t_{r(SO)}$	–	25	50	ns
SO Fall Time (C_L = 200 pF)	$t_{f(SO)}$	–	25	50	ns
SI, CSB, SCLK Incoming Signal Rise Time (Note 2)	$t_{r(SI)}$	–	–	50	ns
SI, CSB, SCLK Incoming Signal Fall Time (Note 2)	$t_{f(SI)}$	–	–	50	ns
Time from Falling Edge of CSB to SO Low Impedance (Note 3)	$t_{SO(en)}$	–	–	110	ns
Time from Rising Edge of CSB to SO High Impedance (Note 4)	$t_{SO(dis)}$	–	–	110	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 5) 0.2 V_{DD} ≤ SO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{valid}	–	65	105	ns

NOTES: 1. $\overline{\text{Reset}}$ Low duration measured with outputs enabled and going to OFF or disabled condition.
2. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
3. Time required for output status data to be available for use at SO pin.
4. Time required for output status data to be terminated at SO pin.
5. Time required to obtain valid data out from SO following the rise of SCLK (see Figure 4).

Figure 2. Input Timing Switching Characteristics

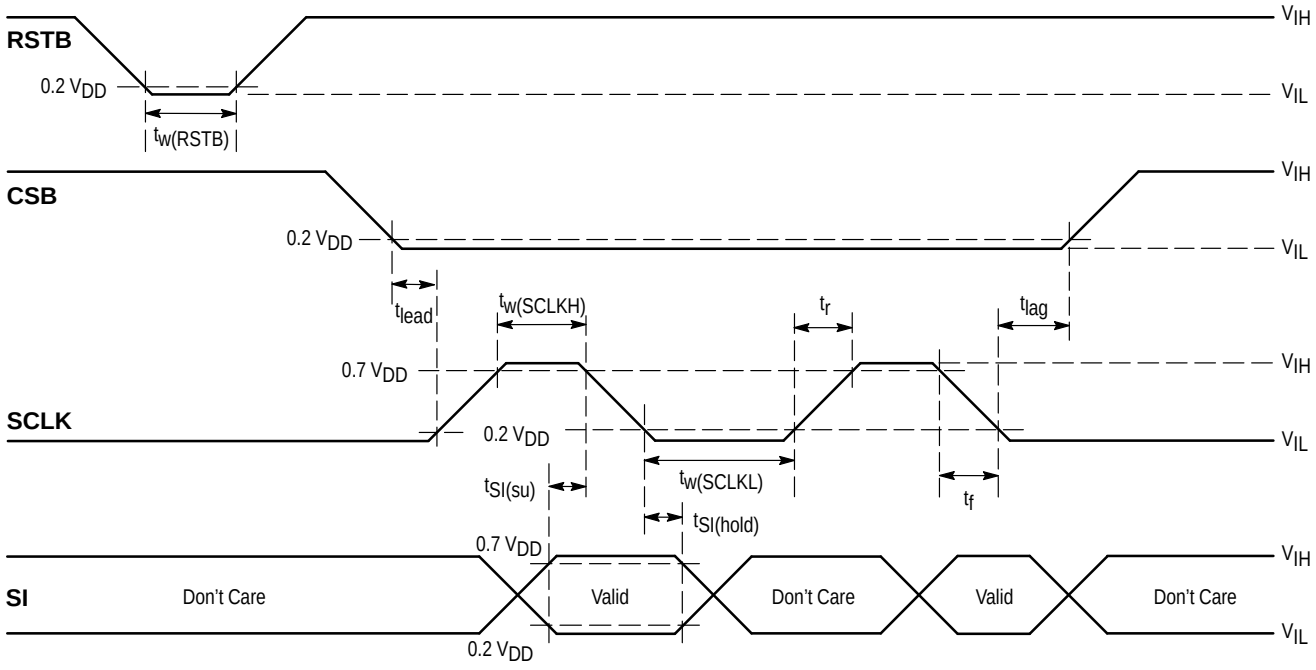
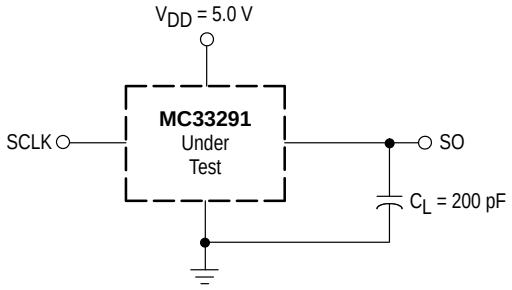
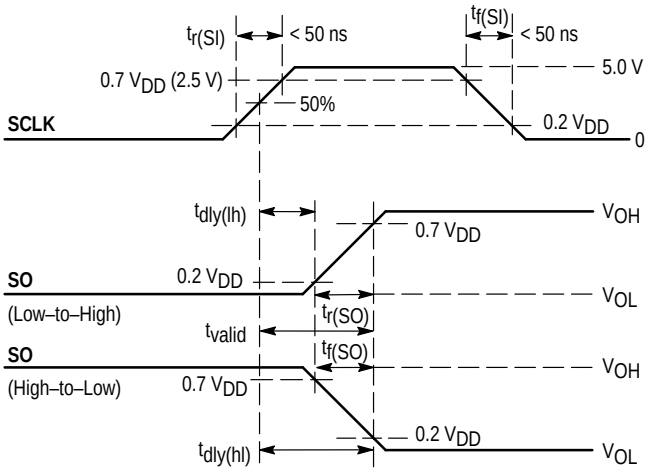


Figure 3. Valid Data Delay Time and Valid Time Test Circuit



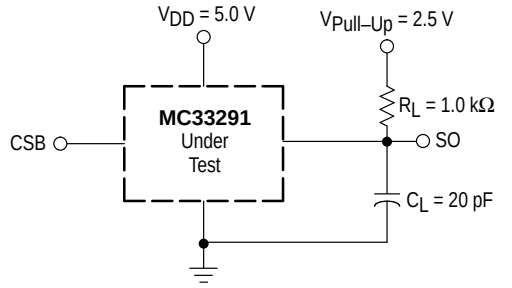
NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 4. Valid Data Delay Time and Valid Time Waveforms



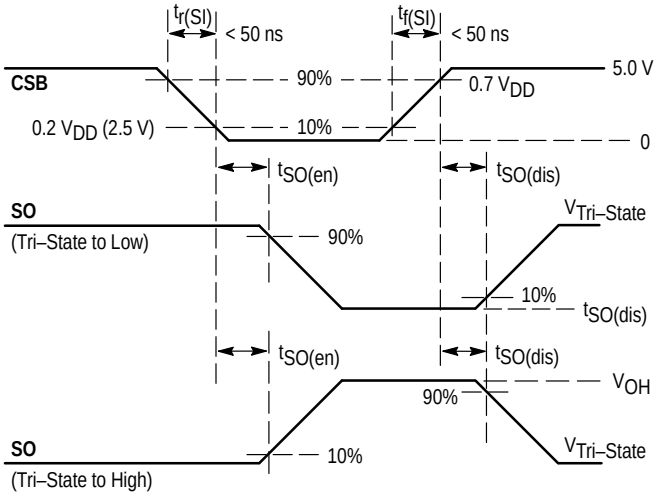
NOTE: SO (Low–to–High) is for an output with internal conditions such that the low–to–high transition of CSB causes the SO output to switch from high to low.

Figure 5. Enable and Disable Time Test Circuit



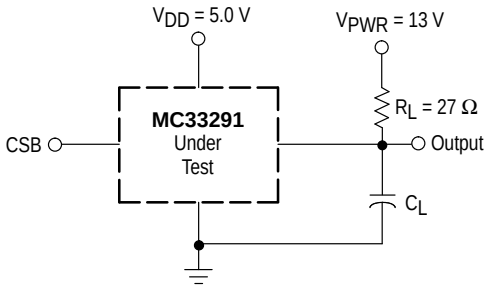
NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 6. Enable and Disable Time Waveforms



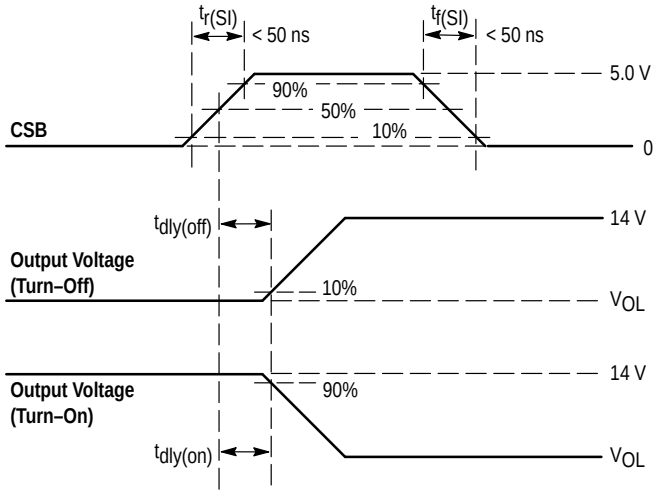
NOTES: 1. SO is in a high or low Tri–state condition whenever CSB is in a logic high state.
2. SO is in either an active low or active high state, depending on whether the corresponding clocked output is faulted or not, when CSB is in a logic low state.

Figure 7. Switching Time Test Circuit



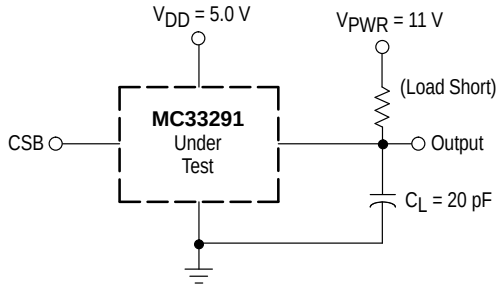
NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 8. Turn–ON/OFF Waveforms



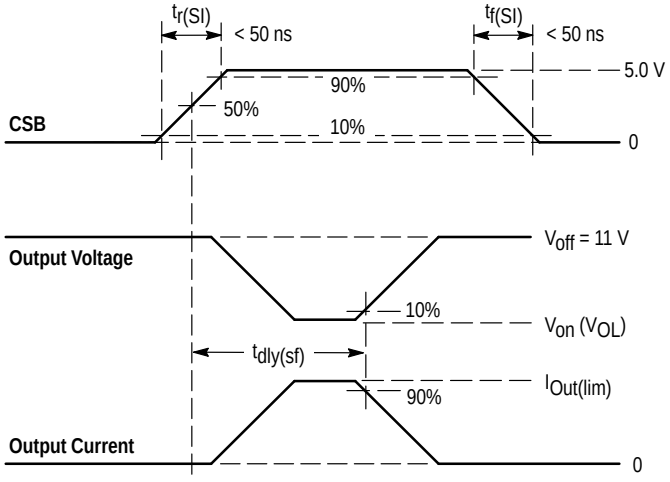
NOTES: 1. $t_{dly(on)}$ and $t_{dly(off)}$ are turn–on and turn–off propagation delay times.
2. Turn–Off is an output programmed from an ON to an OFF state.
3. Turn–On is an output programmed from an OFF to an ON state.

Figure 9. Output Fault Unlatch Disable Delay Test Circuit



NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 10. Output Fault Unlatch Disable Delay Waveforms



NOTES: 1. $t_{pdly(off)}$ is the output fault unlatch disable propagation delay time required to correctly report an output fault after CSB rises. Represents an output commanded ON while having an existing output short (overcurrent) to supply.
2. SFPD pin ≤ 0.2 V

CIRCUIT DESCRIPTION

Introduction

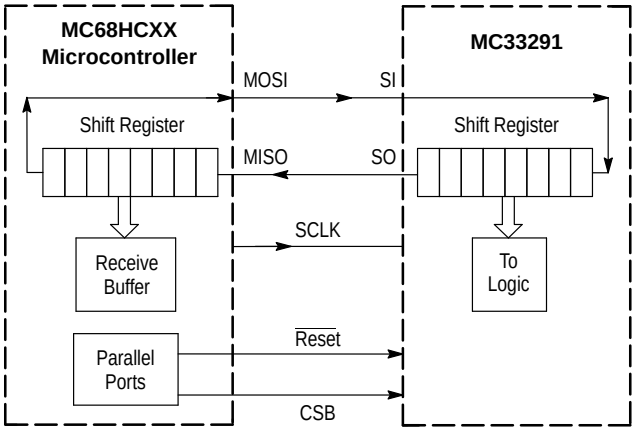
The MC33291 was conceived, specified, designed, and developed for automotive applications. It is an eight output low side power switch having 8–bit serial control. The MC33291 incorporates *SMARTMOS*™ technology having effective 1.5 μ CMOS logic, bipolar/MOS analog circuitry, and independent state of the art double diffused MOS (DMOS) power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified block diagram of the MC33291 is shown in Figure 1.

Where bipolar devices require considerable control current for their operation, structured MOS devices, since they are voltage controlled, require only transient gate charging current affording a significant decrease in power consumption. The CMOS capability of the *SMARTMOS*™ process allows significant amounts of logic to be economically incorporated into the monolithic design. In addition, the bipolar/MOS analog circuits embedded within the updrain power DMOS output transistors monitor and provide fast, independent protection control functions for each individual output. All outputs have internal 45 V at 0.5 A independent output voltage clamps to provide fast inductive turn–off and transient protection.

The MC33291 uses high efficiency updrain power DMOS output transistors exhibiting very low room temperature drain–to–source ON resistance values ($R_{DS(on)} \leq 1.0\ \Omega$ at 13 V V_{PWR}) and dense CMOS control logic. Operational bias currents of less than 2.0 mA (1.0 mA typical) with any combination of outputs ON are the result of using this mixed technology and would not be possible with bipolar structures. To accomplish a comparable functional feature set using a bipolar structure approach would result in a device requiring hundreds of milliamperes of internal bias and control current. This would represent a very large amount of power to be consumed by the device itself and not available for load use.

In operation the MC33291 functions as an eight output serial switch serving as a microcontroller (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. The MC33291 directly interfaces to an MCU and operates at system clock serial frequencies in excess of 3.0 MHz using a Synchronous Peripheral Interface (SPI) for control and diagnostic readout. Figure 11 shows the basic SPI configuration between an MCU and one MC33291.

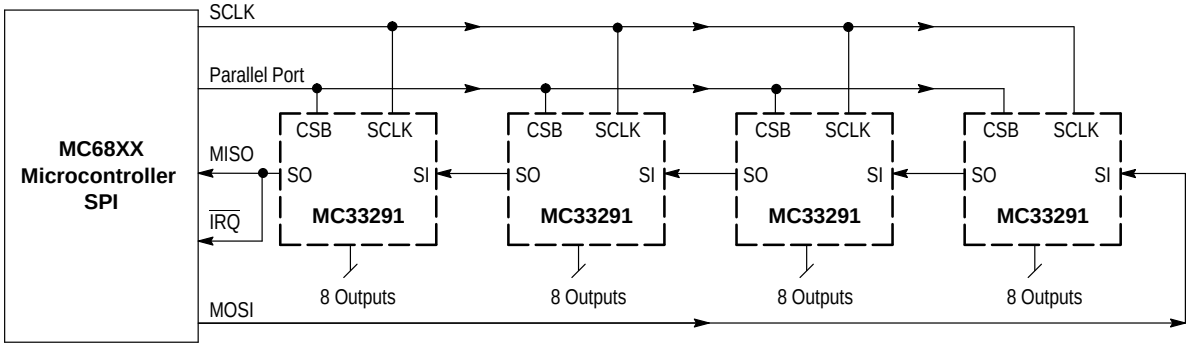
Figure 11. SPI Interface with Microcontroller



The circuit can also be used in a variety of other applications in the computer, telecommunications, and industrial fields. It is parametrically specified over an input “battery”/supply range of 9.0 to 16 V but is designed to operate over a considerably wider range of 5.5 to 26.5 V. The design incorporates the use of Logic Level MOSFETs as output devices. These MOSFETs are sufficiently turned ON with a gate voltage of less than 5.0 V thus eliminating the need for an internal charge pump. Each output is identically sized and *independent* in operation. The efficiency of each output transistor is such that at room temperature with as little as 9.0 V supply (V_{PWR}), the maximum $R_{DS(on)}$ of an output at room temperature is 1.2 Ω (0.9 Ω typical) and increases to only 2.0 Ω as V_{PWR} is decreased to 5.5 V.

All inputs are compatible with 5.0 V CMOS logic levels and incorporate negative or inverted logic. Whenever an input is programmed to a logic low state (<1.0 V) the corresponding low side switched output being controlled will be active low and turned ON. Conversely, whenever an input is programmed to a logic high state (>3.0 V), the output being controlled will be high and turned OFF.

Figure 12. MC33291 SPI System Daisy Chain



One main advantage of the MC33291 is the serial port which when coupled to an MCU, receives ON/OFF commands from the MCU and in return transmits the drain status of the device's output switches. Many devices can be "daisy–chained" together to form a larger system (see Figure 12). Note in this example that only one dedicated MCU parallel port (aside from the required SPI) is needed for chip select to control 32 possible loads.

Multiple MC33291 devices can also be controlled in a parallel input fashion using SPI (see Figure 13). This figure shows a possible 24 loads being controlled by only three dedicated parallel MCU ports used for chip select.

Figure 13. Parallel Input SPI Control

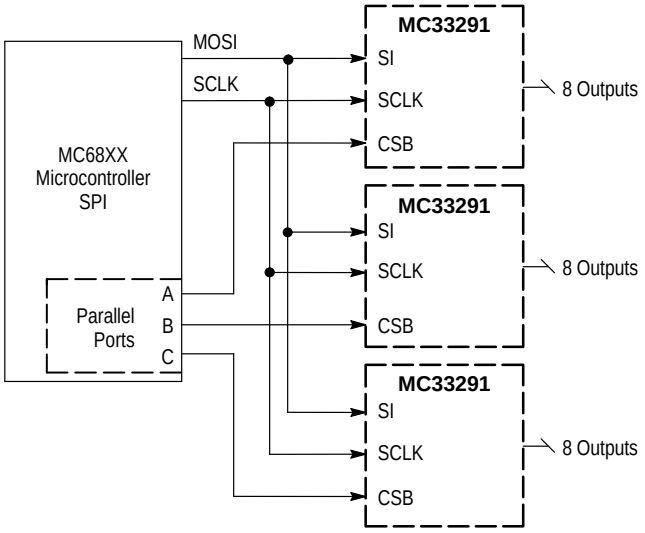


Figure 14 shows a basic method of controlling multiple MC33291 devices using two MCUs. A system can have only one master MCU at any given instant of time and one or more slave MCUs. Master control of the system must pass from one MCU to the other in an orderly manner. The master MCU supplies the system clock signal (top MCU designated the master); the lower MCU being the slave. It is possible to have a system with more than one master, but not at the same time. Only when the master is not communicating can a slave assume the "mastership" and communicate. MCU master control is switched through the use of the slave select (SS) pin of the MCUs. A master will become a slave when it detects a logic low state on its SS pin. Some MCUs have slave select override capability and one must consult the MCU manufacturer for the specific details.

These basic examples make the MC33291 very attractive for applications where a large number of loads need be controlled efficiently. The popular Synchronous Serial Peripheral Interface (SPI) protocol is incorporated, to this end, to communicate efficiently with the MCU.

SPI System Attributes

The SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output (I/O) on the MC33291. It also offers an easy means of expanding the I/O function using few MCU pins. The SPI system of communication consists of the MCU transmitting, and in return, receiving one data–bit of information per system clock cycle.

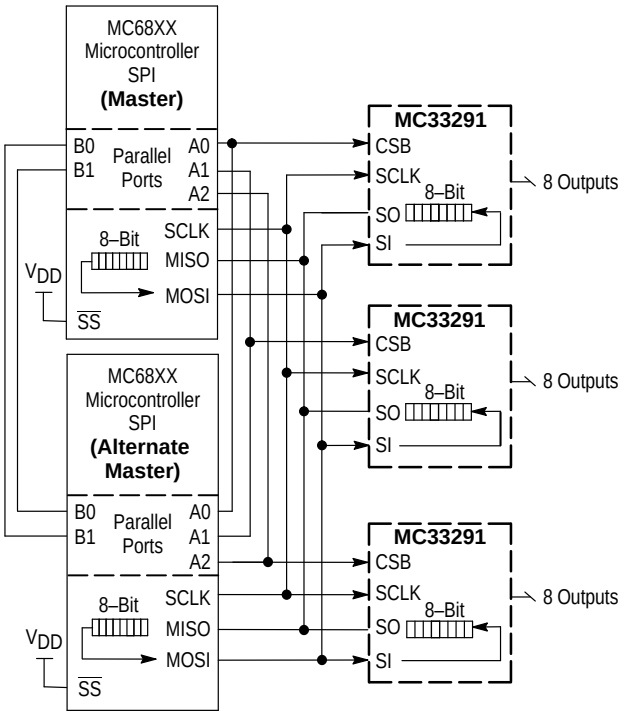
Data–bits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU.

Some features of SPI are:

- Full Duplex, Three–Wire Synchronous Data Transfer
- Each Microcontroller can be a Master or a Slave
- Provides Write Collision Flag Protection
- Provides End of Message Interrupt Flag
- Four I/Os Associated with SPI (MOSI, MISO, SCLK, SS)

The only drawbacks to SPI are that an MCU is required for efficient operational control and, in contrast to parallel input control, is slower at performing pulse width modulating (PWM) functions due to having to write an 8–bit word. The dynamic range and accuracy of PWM functions is a direct result of the clock frequency used.

Figure 14. Multiple MCU SPI Control



PIN FUNCTION DESCRIPTION

CSB Pin

The system MCU selects the MC33291 to be communicated with through the use of the CSB pin. Whenever this pin is in a logic low state, data can be transferred from the MCU to the MC33291 via the SI pin and from the MC33291 to the MCU via the SO pin. Clocked–in data from the MCU is transferred from the MC33291 shift register and latched into the power outputs on the rising edge of the CSB signal. On the falling edge of the CSB signal, drain status information is transferred from the power outputs and loaded into the device's shift register. The CSB pin also controls the output driver of the serial output pin (SO). Whenever the CSB pin goes to a logic low state, the SO pin output driver is enabled allowing information to be transferred from the MC33291 to the MCU. To avoid data corruption or the generation of spurious data, it is essential that the high–to–low transition of the CSB signal occur only when SCLK is in a logic low state.

SCLK Pin

The system clock pin (SCLK) clocks the internal shift registers of the MC33291. The serial input pin (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the SO Line Driver on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CSB) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CSB in logic high state). When CSB is in a logic high state, signals at the SCLK and SI pins are ignored and SO is tri–stated (high impedance). See the Data Transfer Timing diagram of Figure 15.

SI Pin

This pin is for the input of serial instruction data. SI information is read in on the falling edge of SCLK. A logic high state present on this pin when the SCLK signal rises will program a specific output OFF, and in turn, turns OFF the specific output on the rising edge of the CSB signal. Conversely, a logic low state present on the SI pin will program the output ON, and in turn, turns ON the specific output on the rising edge of the CSB signal. To program the eight outputs of the MC33291 ON or OFF, an eight bit serial stream of data is required to be synchronously entered into the SI pin starting with Output 7, followed by Output 6, Output 5, etc., to Output 0. Referring to Figure 15; The D0 bit is the Most Significant Bit (MSB) corresponding to Output 7. For each rise of the SCLK signal, with CSB held in a logic low state, a data–bit instruction (ON or OFF) is synchronously loaded into the shift register per the data–bit SI state. The shift register is full after eight bits of information have been entered. To preserve data integrity, care should be taken to not transition SI as SCLK transitions from a low–to–high logic state.

SO Pin

The serial output (SO) pin is the "tri–stateable" output from the shift register. The SO pin remains in a high impedance state until the CSB pin goes to a logic low state. The SO data reports the drain status, either high or low relative to the previous command word. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is OFF and not faulted, the corresponding SO data–bit is a high state. When an output is ON, and there is no fault, the corresponding data–bit on the SO pin will be a low logic state. The SI/SO shifting of data follows a First–In–First–Out (FIFO) protocol with both input and output words transferring the MSB first. Referring to Figure 15; The D0* bit is the MSB corresponding to Output 7 relative to the previous command word. The SO pin is not affected by the status of the $\overline{\text{Reset}}$ pin.

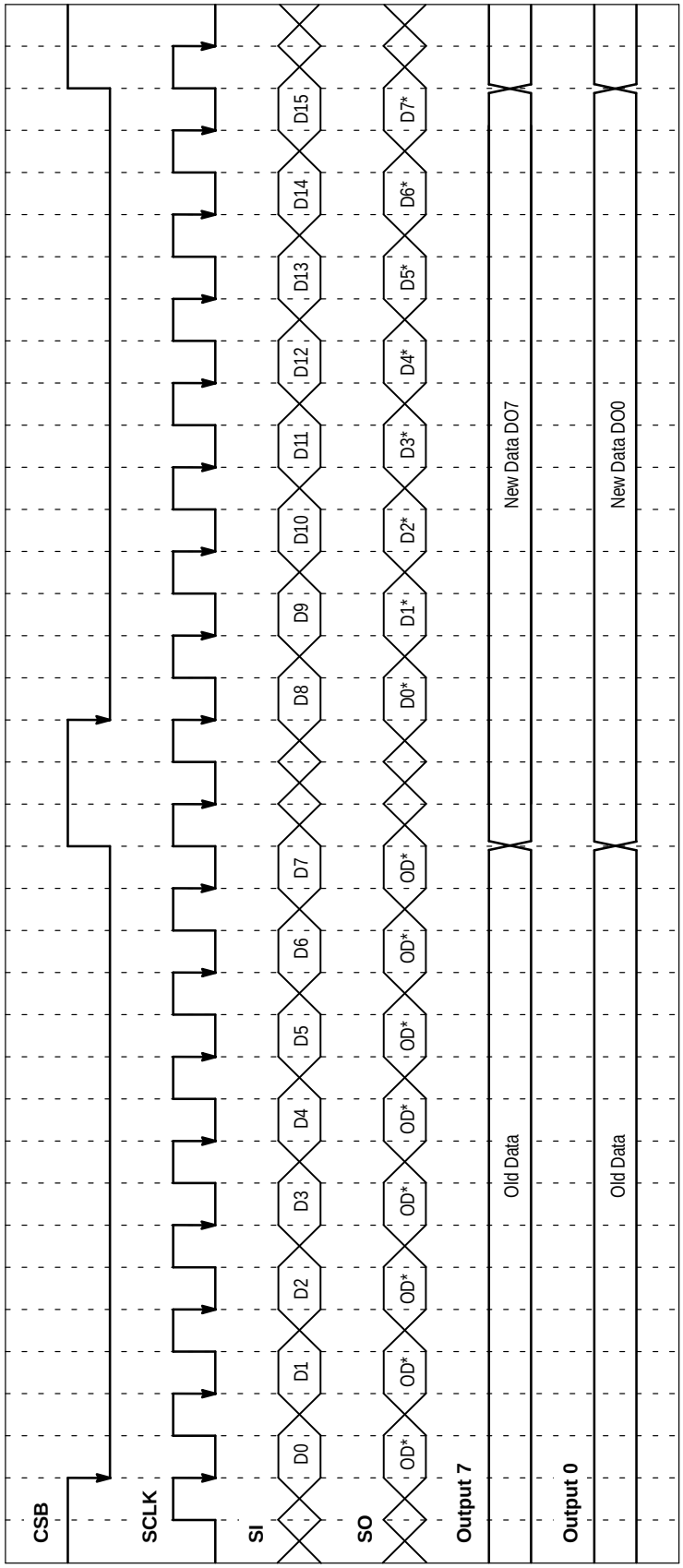
$\overline{\text{Reset}}$ Pin

The MC33291 $\overline{\text{Reset}}$ pin is active low and is used to clear the SPI shift register and in doing so sets all output switches OFF. With the device in a system with an MCU; upon initial system power up, the MCU holds the $\overline{\text{Reset}}$ pin of the device in a logic low state insuring all outputs to be OFF until both the V_{DD} and V_{PWR} pin voltages are adequate for predictable operation. After the MC33291 is reset, the MCU is ready to assert system control with all output switches initially OFF. If the V_{PWR} pin of the MC33291 experiences a low voltage, following normal operation, the MCU should pull the $\overline{\text{Reset}}$ pin low so as to shutdown the outputs and clear the input data register. The $\overline{\text{Reset}}$ pin is active low and has an internal pull–down incorporated to insure operational predictability should the external pull–down of the MCU open circuit. The internal pull–down is only 25 μA to afford safe and easy interfacing to the MCU. The $\overline{\text{Reset}}$ pin of the MC33291 should be pulled to a logic low state for a duration of at least 250 ns to insure reliable reset.

SFPD Pin

The Short Fault Protect Disable (SFPD) pin is used to prevent the outputs from latching–OFF because of an overcurrent condition. This feature allows control of incandescent loads where in–rush currents exceed the device's analog current limits. Essentially the SFPD pin determines whether the MC33291 output(s) will instantly shutdown upon sensing an output short or remain ON in a current limiting mode of operation until the output short is removed or thermal shutdown is reached. If the SFPD pin is tied to V_{DD} = 5.0 V the MC33291 output(s) will remain ON in a current limited mode of operation upon encountering a load short to supply or over current condition. If the SFPD pin is grounded, a short circuit will immediately shut down only the output affected. Other outputs not having a fault condition will operate normally. The short circuit operation is addressed in more detail later.

Figure 15. Data Transfer Timing



NOTES:
1. $\overline{\text{Reset}}$ pin is in a logic high–state during the above operation.
2. D0, D1, D2, ..., and D15 relate to the ordered entry of program data into the MC33291 with D0/D8 bits (MSB) corresponding to Output 7 and D7/D15 corresponding to Output 0.
3. D0*, D1*, D2*, ..., and D7* relate to the ordered data out of the MC33291 with D0* bit (MSB) corresponding to Output 7.
4. OD* corresponds to Old Databits.
5. For brevity, only DO7 and DO0 are shown which respectively correspond to Output 7 and Output 0.

Data Transfer Timing (General)

CSB High–to–Low	SO pin is enabled. Output Status information transferred to Output Shift Register.
CSB Low–to–High	Data from the Shift Register is transferred to the Output Power Switches.
SO	Will change state on the rising edge of the SCLK pin signal.
SI	Will accept data on the falling edge of the SCLK pin signal.

Power Consumption

The MC33291DW has extremely low power consumption in both the operating and standby modes. In the standby or "sleep" mode, with $V_{DD} \leq 2.0$ V, the current consumed by the V_{PWR} pin is less than 25 μA. In the operating mode, the current drawn by the V_{DD} pin is less than 4.0 mA (1.0 mA typical) while the current drawn at the V_{PWR} pin is 2.0 mA maximum (1.0 mA typical). During normal operation, turning outputs ON increases I_{PWR} by only 20 μA per output. Each output experiencing a "soft short" (overcurrent conditions just under the current limit), adds 0.5 mA to the I_{PWR} current.

Paralleling of Outputs

Using MOSFETs as output switches allows the connection of any combination of outputs together. $R_{DS(on)}$ of MOSFETs have an inherent positive temperature coefficient providing balanced current sharing between outputs without destructive operation (bipolar outputs could not be paralleled in this fashion as thermal run–away would likely occur). The device can even be operated with all outputs tied together. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(on)}$ while the Output OFF Open Load Detect Currents and the Output Current Limits increase correspondingly (by a factor of eight if all outputs are paralleled). Less than 125 mΩ $R_{DS(on)}$ at 25°C with current limiting of 8 to 24 A will result if all outputs are paralleled together. There will be no change in the Overvoltage detect or the OFF Output Threshold Voltage Range. The advantage of paralleling outputs within the same MC33291 affords the existence of minimal $R_{DS(on)}$ and output clamp voltage variation between outputs. Typically, the variation of $R_{DS(on)}$ between outputs of the same device is less than 0.5%. The variation in clamp voltages (which could affect dynamic current sharing) is less than 5%. Paralleling outputs from two or more different devices is possible but not recommended. This is because there is no guarantee that the $R_{DS(on)}$ and clamp voltage of the two devices will match. System level thermal design analysis and verification should be conducted whenever paralleling outputs; particularly where different devices are involved.

FAULT LOGIC OPERATION

General

The MCU can perform a parity check of the fault logic operation by comparing the command 8–bit word to the status 8–bit word. Assume that after system reset, the MCU first sends an 8–bit command word (Command Word 1) to the MC33291. Each output that is to be turned ON will have its corresponding data–bit low. Refer to the Data Transfer Timing diagram of Figure 15. As Command Word 1 is being written into the shift register of the MC33291, a status word is being simultaneously written out and received by the MCU. However, the word being received by the MCU is the status of the *previous* command word written to the MC33291 (Status Word 0). If the same command word of the MCU is written a second time (Command Word 2 = Command Word 1), the word *received* by the MCU, Status Word 2, is the status of Command Word 1. The timing diagram shown in Figure 15 depicts this operation. Status Word 2 is then compared with Command Word 1. The MCU will Exclusive OR Status Word 2 with Command Word 1 to determine if the two status words are identical. If the two status words are identical, no faults exist. If the two status words differ, there exists a fault and further status word analysis is necessary to determine the cause. The timing between the two write words must be greater than 100 μs so as to allow adequate time to sense and report the proper drain status. The system databus integrity may be tested by writing two like words to the MC33291 within a few microseconds of each other.

Initial System Setup Timing

The MCU can monitor two kinds of faults:
(1) Communication errors on the data bus and
(2) Actual faults of the output loads.

After initial system start up or reset, the MCU will write one word to the MC33291. If the word is repeated within a few microseconds (say 5) of the first word, the word received by the MCU, at the end of the repeated word, serves as a confirmation of data bus integrity (1). At startup, the MC33291 will take 70 to 250 μs before a repeat of the first word can give the actual status of the outputs. Therefore, the first word should be repeated at least 250 μs later to verify the status of the outputs.

The SO pin of the MC33291 will indicate any one of four faults. The four possible faults are Over Temperature, Output OFF Open Fault, Short Fault (overcurrent), and V_{PWR} Overvoltage Fault. All of these faults, with the exception of the Overvoltage Fault, are output specific. Over Temperature Detect, Output OFF Open Detect, and Output Short Detect are dedicated to each output separately such that the outputs are independent in operation. A V_{PWR} Overvoltage Detect is of a "Global" nature causing all outputs to be turned OFF.

Over Temperature Fault

Over Temperature Detect and shutdown circuits are specifically incorporated for each individual output. The shutdown that follows an Over Temperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155 to 185°C. When an output shuts down due to an Over Temperature Fault, no other outputs are affected. The MCU recognizes the fault since the output was commanded to be ON and the status word indicates that it is OFF. A maximum hysteresis of 20°C ensures an adequate time delay between output turn OFF and recovery. This avoids a very rapid turn ON and turn OFF of the device around the Over Temperature threshold. When the temperature falls below the recovery level for the Over Temperature Fault, the device will turn ON only if the Command Word during the *next* write cycle indicates the output should be turned ON.

Overvoltage Fault

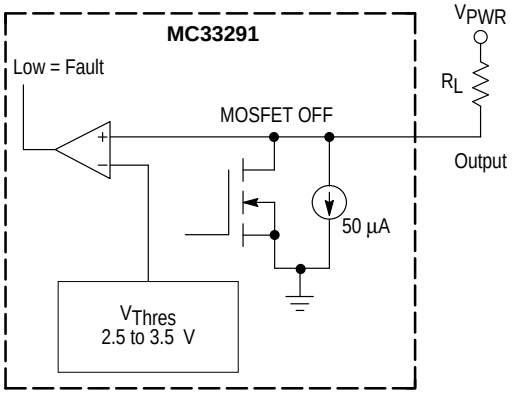
An Overvoltage condition on the V_{PWR} pin will cause the MC33291 to shutdown all outputs until the overvoltage condition is removed and the device is re–programmed by the SPI. The Overvoltage threshold on the V_{PWR} pin is specified as 28 to 36 V with 1.0 V typical hysteresis. Following the overvoltage condition, the *next* write cycle sends the SO pin the hexadecimal word $FF (all ones) indicating all outputs are turned OFF. In this way, potentially

dangerous timing problems are avoided and the MCU reset routine ensures an orderly startup of the loads. The MC33291 does not detect an overvoltage on the V_{DD} pin. Other external circuitry, such as the Motorola MC33161 Universal Voltage Monitor, is necessary to accomplish this function.

Output OFF Open Load Fault

An Output OFF Open Load Fault is the detection and reporting of an "open" load when the corresponding output is disabled (input bit programmed to a logic high state). To understand the operation of the Open Load Fault detect circuit, see Figure 16. The Output OFF Open Load Fault is detected by comparing the drain voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Figure 16. Output OFF Open Load Detect



An Output OFF Open Load Fault is indicated when the output voltage is less than the Output Threshold Voltage (V_{Thres}) of 2.5 to 3.5 V. Since the MC33291 outputs function as switches, during normal operation, each MOSFET output should either be completely turned ON or OFF. By design the threshold voltage was selected to be between the ON and OFF voltage of the MOSFET. During normal operation, the ON state V_{DS} voltage of the MOSFET is less than the minimum threshold voltage and the OFF state V_{DS} voltage is greater than the maximum threshold voltage. This design approach affords using the same threshold comparator for Output Open Load Detect in the OFF state and Short Circuit (or overcurrent) Detect in the ON state. See Figure 17 for an understanding of the Short Circuit Detect circuit. An OFF state output voltage of less than 2.5 V *will* be detected as an Output OFF Open Load Fault (output open) while voltages greater than 3.5 V will *not* be detected as a fault.

The MC33291 has an internal pull–down current source of 50 µA, as shown in Figure 16, between the MOSFET drain and ground. This prevents the output from floating up to V_{PWR} if there is an open load or internal wirebond failure. The internal comparator compares the drain voltage with a reference voltage, V_{Thres}. If the output voltage is less than this reference voltage, the MC33291 will declare the condition to be an open load fault.

During output switching, especially with capacitive loads, a *false* Output OFF Open Load Fault may be triggered. To prevent this *false* fault from being reported an internal fault filter of 70 to 250 µs is incorporated. The duration for which a false fault may be reported is a function of the load impedance (R_L, C_L, L_L), $R_{DS(on)}$, and C_{out} of the MOSFET as well as the supply voltage, V_{PWR}. The rising edge of CSB triggers a built–in fault delay timer which must time out (70 to 250 µs) before the fault comparator is enabled to detect a faulted threshold. The circuit automatically returns to normal operation once the condition causing the Open Load Fault is removed.

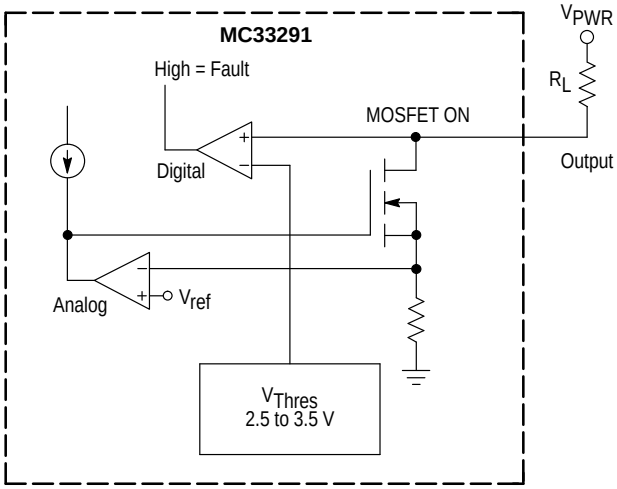
Shorted Load Fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit.

There are three safety circuits progressively in operation during load short conditions which afford system protection; 1) The device's output current is monitored in an analog fashion using a SENSEFET™ approach and current limited, 2) The device's output current is sensed by monitoring the MOSFET drain voltage, and 3) The device's output thermal limit is sensed and when attained causes only the specific faulted output to be latched OFF, allowing all remaining outputs to operate normally. All three protection mechanisms are incorporated in each output affording robust independent output operation.

The analog current limit circuit is always active and monitors the output drain current. An overcurrent condition causes the gate control circuitry to reduce the gate–to–source voltage imposed on the output MOSFET which re–establishes the load current in compliance with current limit (1.0 to 3.0 A) range. The time required for the current limit circuitry to act is less than 20 µs. Therefore, currents higher than 1.0 to 3.0 A will never be seen for more than 20 µs (a typical duration is 10 µs). If the current of an output attempts to exceed the predetermined limit of 1.0 to 3.0 A (2.0 A nominal), the V_{DS} voltage will exceed the V_{Thres} voltage and the overcurrent comparator will be tripped as shown in Figure 17.

Figure 17. Short Circuit Detect and Analog Current Limiting Circuit



The status of SFPD will determine whether the MC33291 will shut down immediately or continue to operate in an analog current limited mode until either the short circuit (overcurrent) condition is removed or thermal shutdown is reached.

Grounding the SFPD pin will enable the short fault protection shutdown circuitry. Consider a load short (output short to supply) occurring on an output before, during, and

after output turn ON. When the CSB signal rises to the high logic state, the corresponding output is turned ON and a delay timer activated. The duration of the delay timer is 70 to 250 μs. If the short circuit takes place before the output is turned ON, the delay experienced is the entire 70 μs to 250 μs followed by shutdown. If the short occurs during the delay time, the shutdown still occurs after the delay time has elapsed. If the short circuit occurs after the delay time, shutdown is immediate (within 20 μs after sensing). The purpose of the delay timer is to prevent *false* faults from being reported when switching capacitive loads.

If the SFPD pin is at 5.0 V (or $V_{DD)}$, an output will not be disabled when an overcurrent is detected. The specific output will, within 5.0 to 10 μs of encountering the short circuit, go into an analog current limited mode. This feature is especially useful when switching incandescent lamp loads, where high in–rush currents experienced during startup last for 10 to 20 milliseconds.

Each output of the MC33291 has its own overcurrent shutdown circuitry. Over temperature faults and the overvoltage faults are not affected by the SFPD pin's state.

Both load current sensing and output voltage sensing are incorporated for Short Fault detection with actual detection occurring slightly *after* the onset of current limit. The current limit circuitry incorporates a "SENSEFET™" approach to measure the total drain current. This calls for the current through a small number of cells in the power MOSFET to be measured and the result multiplied by a constant to give the total current. Wherein output shutdown circuitry measures the drain–to–source voltage and shuts down the output if its threshold (V_{Thres}) is exceeded.

Short Fault detection is accomplished by sensing the output voltage and comparing it to V_{Thres}. The lowest V_{Thres} requires a voltage of 2.5 V to be sensed. For an enabled output, with $V_{DD} = 5.0 \pm 0.5$ V, an output voltage in excess of 3.5 V *will* be detected as a "short" (overcurrent condition) while voltages less than 2.5 V will *not* be detected as "shorts."

Over Current Recovery

If the SFPD pin is in a high logic state, the circuit returns to normal operation automatically after the short circuit is removed (unless thermal shutdown has occurred).

If the SFPD pin is grounded and overcurrent shutdown occurs, removal of the short circuit will result in the output remaining OFF until the next write cycle. If the short circuit is *not* removed, the output will turn ON for the delay time (70 to 250 μs) and then turn OFF for every write cycle commanding a turn ON.

SFPD Pin Voltage Selection

Since the voltage condition of the SFPD pin controls the activation of the short fault protection (i.e. shutdown) mode equally for all eight outputs, the load having the longest duration of in–rush current determines what voltage (state) the SFPD pin should be at. Usually if at least one load is, say an incandescent lamp, the in–rush current on that input will be milliseconds in duration. Therefore, setting SFPD at 5.0 V will prevent shutdown of the output due to the in–rush current. The system relies only on the Over Temperature Shutdown to protect the outputs and the loads. The MC33291 was designed to switch GE194 incandescent lamps (or equivalents) with the SFPD pin in a grounded state. Considerably larger lamps can be switched with the SFPD pin held in a high logic state.

Sometimes both a delay period greater than 70 to 250 μs (current limiting of the output) followed by an immediate over current shutdown is necessary. This can be accomplished by programming the SFPD pin to 5.0 V for the extended delay period to afford the outputs to remain ON in a current limited mode and then grounding it to accomplish the immediate shutdown after some period of time. Additional external circuitry is required to implement this type of function. An MCU parallel output port can be devoted to controlling the SFPD voltage during and after the delay period, is often a much better method. In either case, care should be taken to execute the SFPD start–up routine every time start–up or reset occurs.

Undervoltage Shutdown

An undervoltage V_{DD} condition will result in the global shutdown of all outputs. The undervoltage threshold is between 2.5 V and 3.5 V. When V_{DD} goes below the threshold, all outputs are turned OFF and the SO data register is reset to indicate the same.

An undervoltage condition at the V_{PWR} pin will *not* cause output shutdown and reset. When V_{PWR} is between 5.5 V and 9.0 V, the outputs will operate per the command word. However, the status as reported by the serial output (SO) pin may not be accurate below 9.0 V V_{PWR}. Proper operation at V_{PWR} voltages below 5.5 V can not be guaranteed.

Deciphering Fault Type

The MC33291 SO pin can be used to understand what kind of system fault has occurred. With eight outputs having open load, over current, over temperature, and over voltage faults; a total of 25 different faults are possible. The SO status word received by the MCU will be compared with the word sent to the MC33291 during the previous write cycle. For a specific output, if the SO bit compares with the corresponding SI bit of the previous word; the output is operating normal with no fault. Only when the SO bit and previous word SI bit differ is there a fault indicated. If the two words are *not* the same, then the MCU should be programmed to determine which output or outputs are faulted.

If for a specific output, the initial SI command bit were logic high, the output would be programmed to be "off"; if upon the next command word being entered, a logic low came back on SO, for that specific output's corresponding bit, an "output–off open–load" fault would be indicated. The resulting SO bit, for that specific output, would be different from that entered during the previous word for that SI bit, indicating the fault. The eight output–off open–load faults are therefore most easily detected.

If for a specific output, the initial SI command bit were a logic low, calling for the output to be programmed "on"; upon the next word command being entered, the corresponding bit came back with a logic high on SO, an output over current fault would be indicated. An over current fault is always reported by the SO output and is independent of the logic state existing on the SFPD pin. It should be pointed out that when the SFPD pin is in a logic high state, an over current condition will be reported on the SO pin but output current limiting will be in effect and the output will be permitted to operate so long as the over current condition does not drive output into an over temperature fault. An over temperature fault will shutdown the specific output effected for the duration of the over temperature condition.

Over current and over temperature faults are often related. Turning the effected output switches OFF and waiting for some time to allow the output to cool down should make these types of faults go away. “Soft” over current faults can sometimes be determined over hard short faults and over temperature faults by observing the time required for the device to recover. In general though, over current and over temperature faults can not be differentiated in normal application usage.

One advantage of the synchronous serial output is that multiple faults can be detected with only one pin (SO) being used for fault status reporting.

If V_{PWR} experiences an overvoltage condition, all outputs will immediately be turned OFF and remain latched OFF. A new command word is required to turn the outputs back ON following an overvoltage condition.

1st Cmd Word		2nd Cmd Word		Status
SI	SO (Note 1)	SI (Note 2)	SO	(Note 3)
H	X	H	H	ok/normal/output “off”
L	X	L	L	ok/normal/output “on”
H	X	H	L	fault/output–off open
L	X	L	H	fault/output over current or thermal shutdown or overvoltage shutdown

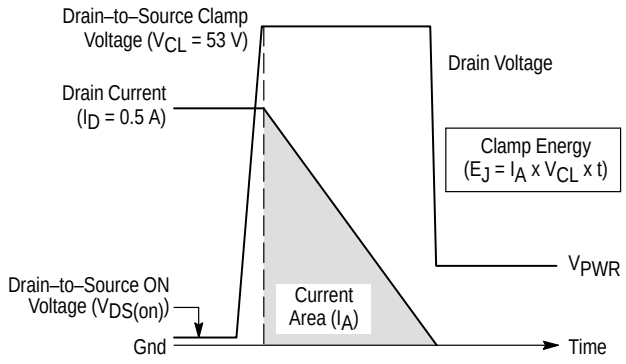
NOTES: 1. During the first command word, the SO output status word is to be ignored (don’t care).
2. During the second command word, the SO output status word is independent of the second command word SI input data; SO results are only valid for the SI data entered during the first (previous) command word.
3. Output faults due to over current, over temperature, or over voltage can be determined but require additional interrigation in order to differentiate the actual cause.

Output Voltage Clamping

Each output of the MC33291 incorporates an internal voltage clamp to provide fast turn–off and transient protection of the output. Each clamp independently limits the drain to source voltage to 53 V at drain currents of 0.5 A and keeps the output transistors from avalanching by causing the transient energy to be dissipated in the linear mode (see Figure 18). The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) times the duration the clamp is active (t).

Characterization of the output clamps, using a single pulse non–repetitive method at 0.5 A, indicate the maximum energy to be 50 mJ at 150°C junction temperature per output.

Figure 18. Output Voltage Clamping



THERMAL CHARACTERIZATION

Thermal Performance

Traditionally, the steady state thermal performance of packaged semiconductor devices has been characterized by only a single junction–to–ambient thermal resistance constant, commonly referred to as θ_{JA}. This is particularly inadequate for multiple output devices where several power dissipating junctions reside within the same integrated circuit (IC), as in the MC33291. In many cases this fact is ignored and all output junctions are lumped together, thereby neglecting the importance of their thermal interaction. This method of characterization overlooks some fundamental thermal physics, specifically that condition where all outputs in the IC are always powered in a fixed relative proportion, the thermal path to ambient cannot be represented by one θ_{JA} constant.

A more sensible approach to the problem of characterizing the thermal performance of multiple output devices is to acknowledge the multiplicity of heat sources (generators) which exist within the IC. The matrix equation shown in Figure 19 was developed for the MC33291 mounted on a Semiconductor Equipment and Materials International (SEMI) standard FR4 thermal characterization board measuring 76.2 by 114.3 mm and containing a minimal amount of metal traces. The equation is accurate for steady state natural convection thermal conditions. The printed circuit board was mounted horizontally in an Electronic Industries Association/Joint Electronic Design Engineering Council (EIA/JEDEC) natural convection test chamber measuring 0.0283 mm^3. The components Q_0 through Q_7 represent the corresponding power dissipation of the individual outputs in Watts. The components T_{J0} through T_{J7} represent the resulting steady state junction temperature of the various outputs in °C. The component “b” is a multiplier which allows the linear matrix equation to account for both radiation and natural convection non–linearities. The equation has been found to predict junction temperatures to within 2°C of experimental data.

Figure 19. Steady State Thermal Matrix Equation

$$b \cdot \begin{bmatrix} 74.3 & 72.7 & 68.7 & 68.4 & 68.6 & 68.2 & 69.3 & 70.0 \\ 73.1 & 74.8 & 69.1 & 68.3 & 68.1 & 68.2 & 69.0 & 68.6 \\ 70.1 & 70.3 & 73.0 & 70.7 & 69.6 & 68.4 & 68.1 & 67.8 \\ 70.1 & 70.1 & 70.9 & 72.1 & 70.8 & 69.2 & 68.5 & 67.9 \\ 70.1 & 69.8 & 69.2 & 70.4 & 72.9 & 71.1 & 69.2 & 68.4 \\ 69.8 & 69.5 & 68.4 & 69.0 & 71.2 & 73.1 & 69.5 & 68.4 \\ 70.8 & 69.9 & 67.8 & 67.8 & 68.7 & 68.8 & 73.3 & 70.7 \\ 72.5 & 71.0 & 68.3 & 68.1 & 68.6 & 68.6 & 71.2 & 71.8 \end{bmatrix} \cdot \begin{bmatrix} Q_0 \\ Q_1 \\ Q_2 \\ Q_3 \\ Q_4 \\ Q_5 \\ Q_6 \\ Q_7 \end{bmatrix} + T_a = \begin{bmatrix} Tj_0 \\ Tj_1 \\ Tj_2 \\ Tj_3 \\ Tj_4 \\ Tj_5 \\ Tj_6 \\ Tj_7 \end{bmatrix} \text{ where } b = \left(\frac{\sum_{i=1}^{7} Q_i}{0.45} \right)^{-13.0389}$$

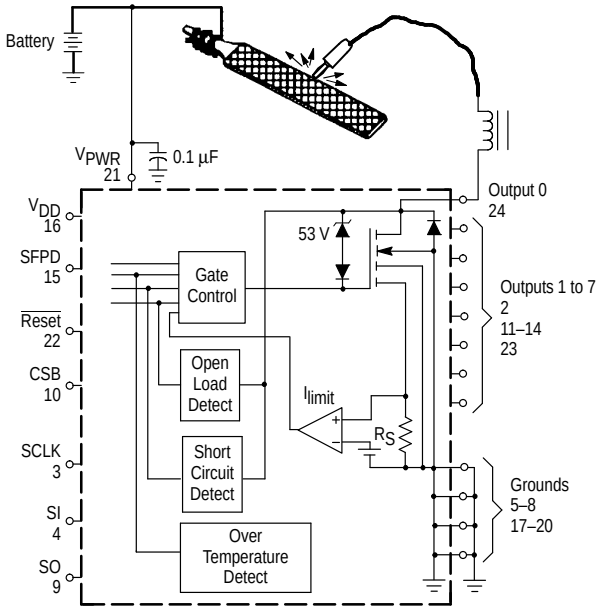
Latch–Up Immunity

Device latch–up caused by substrate injection has been characterized. Latch–up immunity has both a dc and a transient immunity component. DC latch–up immunity results indicate the device to be capable of withstanding in excess of four amps of reverse current out of any of the output transistors while the control logic continues to function normally. The logic control current (I_{DD}) was found to increase by only 0.6 mA with four amps of current being pulled out of an output. Additionally, the I_{PWR} current was found to increase by only 0.15 mA under the same condition. These increases are a result of minority carriers being injected into substrate and subsequently collected.

The following procedure has been developed to test for transient latch–up immunity and has been applied to this automotive circuit design. Results of transient testing indicate the device to operate properly at output currents greater than 1.5 A. The procedure tests for the device's immunity to intermittent load–to–battery current connection with the device controlling an inductive load. Using the appropriately termed "the file test," the battery is connected to a shop file while the lead to the inductive load is dragged across the files surface causing intermittent load opens producing lots of arcs, sparks, and smoke, plus severe transients (see Figure 20). It is during these severe transients that latch–up most likely could occur. The battery voltage used for this test was 18 V and the inductive load was 2.0 mH. These values were found to produce severe transient stresses of the device outputs. All outputs must maintain operation and input control during transient generation to pass "the file test."

The device's input control currents were found to remain stable and were not affected by dc or transient latch–up immunity testing in most all cases.

Figure 20. Transient Latch–Up Immunity File Test



APPLICATIONS INFORMATION

SIOP Communication

Two common communication protocols used in Motorola's microcontrollers are the Serial Peripheral Interface (SPI) and Synchronous Input Output Port (SIOP). SIOP is a subset of the more flexible SPI and the simpler of the two protocols. SIOP is used on many of the MC68HC05 family of microcontrollers. Restrictions of the SIOP protocol include: 1) the SCLK frequency is fixed at one–fourth the internal clock rate and 2) the polarity of the SCLK signal is fixed.

By way of example, the MC68HC05P9 utilizes SIOP protocol and is not directly compatible with the serial input requirements of the MC33291. Specifically, the MC33291 accepts data on the falling edge of SCLK whereas its rising edge triggers data transfer in the SIOP protocol. SCLK is high during SIOP transmissions, which is the opposite of what the MC33291 requires.

Though designed specifically for SPI communication protocol, the MC33291 can easily be adapted to communicate with SIOP protocol through the use of software. The amount of code required to implement SPI in software is relatively small, so the only major drawback is a slower transfer of data. The software routine shown in Table 1 completes a transfer in about 100 μs.

Cost

The bottom line relates to cost. The MC33291 is a very cost effective octal output serial switch for applications typically encountered in the automotive and industrial market segments. To accomplish only the most basic serial switch function the MC33291 offers, using a discrete semiconductor approach, would require the use of at least eight logic level power MOSFETs for the outputs and two shift registers for the I/O plus other miscellaneous "glue" components. Additional circuitry would have to be incorporated to accomplish the protection features offered by the MC33291. Other noteworthy advantages the MC33291 offers are conservation of power and board space, requirement of fewer application components, and enhanced application reliability. The MC33291 is available at a fraction of the cost required for discrete component implementation and represents true value.

The bottom line is; the MC33291 represents a cost effective device having advanced performance and features and worthy of consideration. Hope you find the device satisfactory for your application.

Table 1. Program to Exercise the MC33291 Using SPI (Having Only SIOP) Protocol

SET LABELS FOR OUTPUT REGISTERS

PORTA	EQU	$0000	;SPI Port ;DO (Data Out), SCLK, CS, $\overline{\text{Reset}}$, X, FLTOUT, DI (Data In)
PORTB	EQU	$0001	;Normally the SIOP Port. SIOP will be disabled.
PORTC	EQU	$0002	;A–D Converter Port
PORTD	EQU	$0003	;Timer Capture Port
DDRA	EQU	$0004	;Data Direction Register for SPI Port
DDRB	EQU	$0005	;Data Direction Register for SCLK, SDI, SDO, 11111
DDRC	EQU	$0006	;Data Direction Register for A–D Converter Port
DDRD	EQU	$0007	;Data Direction Register for PORTD, Timer Capture

DTOUT	EQU	$0080	;Register for the SPI output data. This register will be used for a Serial–to–Parallel transformation
DATAIN	EQU	$0081	;Input Register for SPI. Also used for a Serial–to–Parallel transformation
VALUE	EQU	$0082	;Register to store the SPI output word for fault testing
DATA1	EQU	$0083	;Miscellaneous data register

SCR	EQU	$000A	;Label for SIOP control register, 0 SPE 0 MSTR 0 0 0 0
SSR	EQU	$000B	;Label for SIOP status register, SPIF DCOL 0 0 0 0 0 0, Read Only Register
SDR	EQU	$000C	;Label for SIOP data register

	ORG	$0100	;Program starts at first byte of User ROM
INIT	RSP		;Reset Stack Pointer to $FF

Table 1. Program to Exercise the MC33291 Using SPI (Having Only SIOP) Protocol (continued)

INITIALIZE THE DATA REGISTERS AND THEIR DATA DIRECTION BIT REGISTERS

	LDA	#$FE	;Configure Port A as the SPI Port
	STA	DDRA	;All but Bit 0 will be outputs

	LDA	#$FF	
	STA	DDRB	;Configure Register B as an output. SIOP is not used for the MC33291 but is available for another peripheral.
	STA	DDRC	;Configure Register C as an output
	STA	DDRD	;Configure Register D as an output

	LDA	#%00010000	;Initialize the SIOP Control Register
	STA	SCR	;Disable SIOP by clearing Bit 6

SELECT THE DESIRED OUTPUTS

TOP	LDA STA	#$55 VALUE	;Select outputs of MC33291 to be turned ON. This instruction is left inside the loop to include changes while running the program. A set bit will cause the associated MC33291 output to be OFF. The value register is uncorrupted by the serial–to–parallel conversion.
	BSET	4,PORTA	;Reset the MC33291
	BCLR	4,PORTA	;Also establishes a + or – trigger source
	BSET	4,PORTA	;The MC33291 is reset with a logic low

	BCLR	5,PORTA	;Enable MC33291 by pulling CSB (chip select bar) low. Within the MC33291 the Fault Status is transferred to the MC33291 Serial Register at a falling edge of CSB

	LDA	VALUE	;Select outputs to be turned ON
	STA	DTOUT	;Save Output Word (Value) to check for fault

SPI TRANSFER LOOP

	LDX	#$07	;Set the number of Read/Shift cycles

LOOP	ASL	DATAIN	;Shift a Zero into LSB of DATAIN and ASL other bits
	ASL	DTOUT	;Test value currently in MSB of DTOUT
	BCS	DOONE	;
	BCLR	7,PORTA	;MSB was Zero, so clear DATA OUT bit
	JMP	GOON	
DOONE	BSET	7,PORTA	;MSB was One, so set the DATA OUT bit
GOON	BSET	6,PORTA	;Set the SCLK. Serial Output pin of the MC33291 changes state on the rising edge of the SCLK. Read the next bit coming from the MC33291.

	BRCLR	0,PORTA, WZZER0	;Read the bit and branch if Zero. LSB of DATAIN is already cleared due to the ASL above.
	BSET	0,DATAIN	;Bit was One, Set the next bit in DATAIN

WZZER0	BCLR	6,PORTA	;Clear SCLK. Falling edge causes the MC33291 to read the next bit from the MCU.
	DECX		
	BPL	LOOP	;Continue to loop eight times until the SPI transfer is complete

	BSET	5,PORTA	;Transfer control signal to output transistors

Table 1. Program to Exercise the MC33291 Using SPI (Having Only SIOP) Protocol (continued)

ESTABLISH A BRIEF DELAY

	LDA	#16	
PAUSE	DECA		;3 Clock cycles
	BNE	PAUSE	;3 Clock cycles
	BCLR	5,PORTA	;Transfer output status to Serial Register
	JSR	FLTCHK	;Jump to Fault Check subroutine

	JSR	DLY	;Delay 1/T msec

	BSET	5,PORTA	;Deselect the MC33291
	BRA	TOP	;Return to top of loop

SUBROUTINE TO CHECK FOR FAULTS

FLTCHK	BCLR	1,PORTA	;CLR the Fault pin
	LDA	DATAIN	
	CMP	VALUE	;Check for Faults
	BEQ	NOFLT	;If there is no Fault, continue
	BSET	1,PORTA	;Activate Fault LED
NOFLT	RTS		

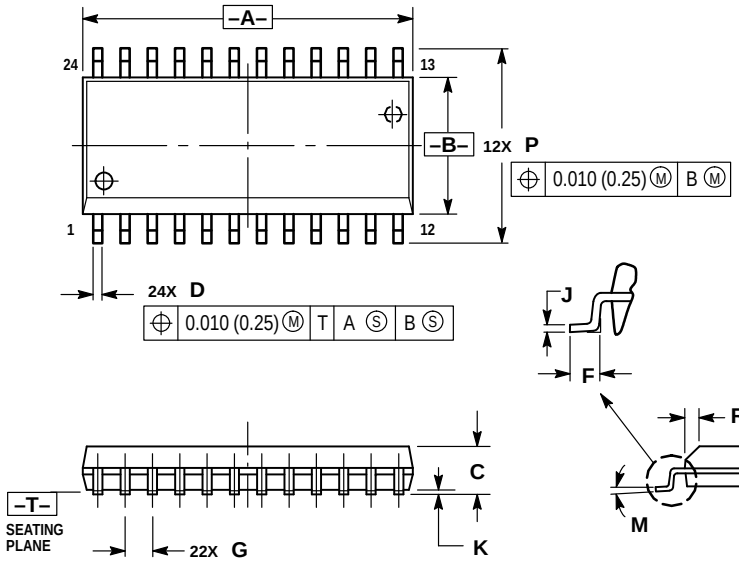
DELAY SUBROUTINE

DLY	STA	DATA1	;Save Accumulator in RAM
	LDA	#$04	;Do outer loop 4 times, roughly 4 ms.
OUTLP	CLRX		;X used as Inner Loop Count
INNRLP	DECX		;0–FF, FF–FE, … 1–0 256 loops
	BNE	INNRLP	;6CYC* 256* 1 µs/CYC = 1.53 ms
	DECA		;4–3, 3–2, 2–1, 1–0
	BNE	OUTLP	;1545CYC* 4*1 µs/CYC = 6.18 ms
	LDA	DATA1	;Recover Accumulator value
	RTS		;Return from subroutine

	ORG	$1FF	
	FDB	INIT	

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04
SOP (16+4+4)L
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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