MOTOROLA

MC74F160A
MC74F162A

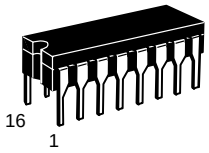
SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

The MC74F160A and MC74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74F162A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

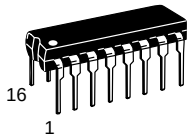
- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

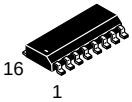
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

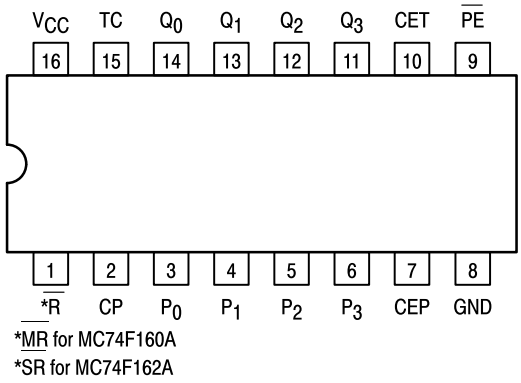


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXAJ	Ceramic
MC74FXXXAN	Plastic
MC74FXXXAD	SOIC

CONNECTION DIAGRAM



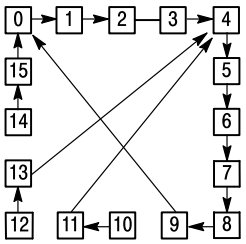
*MR for MC74F160A
*SR for MC74F162A

FUNCTION TABLE

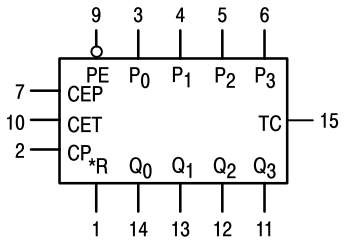
SR	PE	CET	CEP	ACTION ON THE RISING CLOCK EDGE (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P_n Q_n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

STATE DIAGRAM



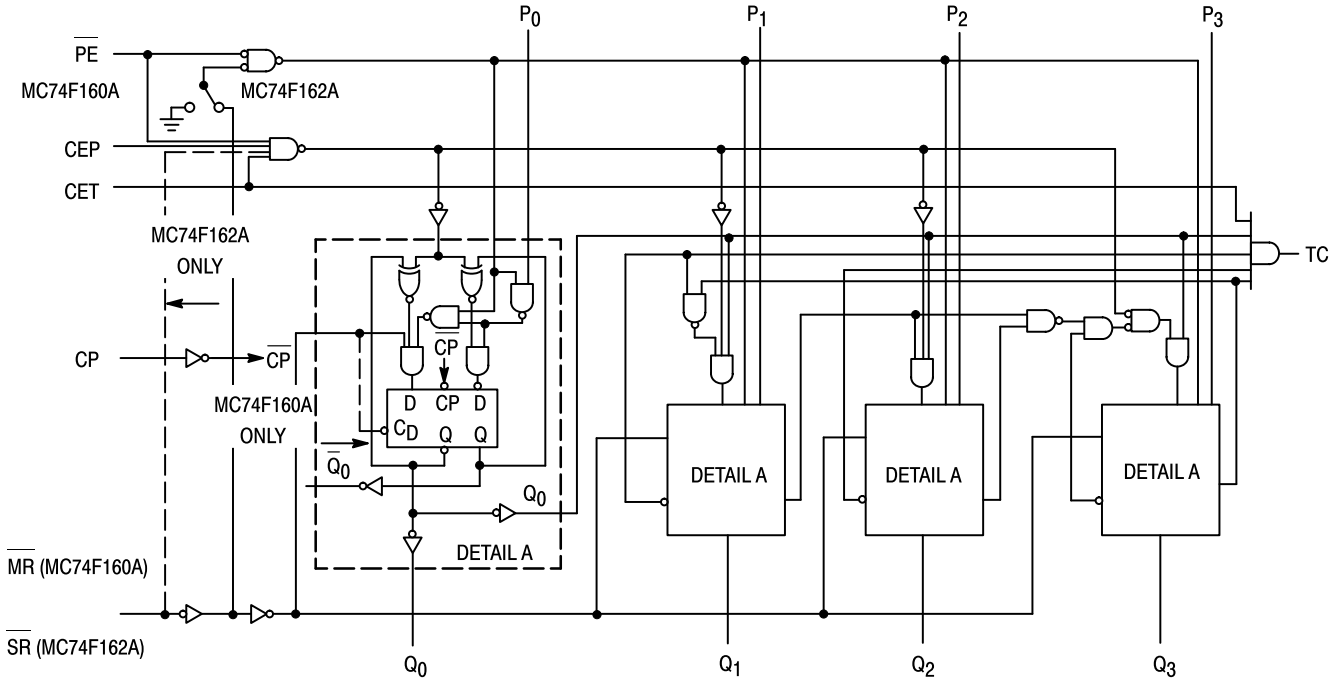
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

*MR for MC74F160A
*SR for MC74F162A

LOGIC DIAGRAM



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74F160A and MC74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus, all changes of the Q outputs (except due to Master Reset of the MC74F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC74F160A), synchronous reset (MC74F162A), parallel load, count-up and hold. Five control inputs — Master Reset (MR, MC74F160A), Synchronous Reset (SR, MC74F162A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Function Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (MC74F160A) or $\overline{SR}$ (MC74F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74F160A and MC74F162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP, and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			–1.0	mA
I_{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	V_{CC} = MIN, I_{IN} = – 18 mA	
V_{OH}	Output HIGH Voltage	74	2.5	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	VCC = MAX, V_{IN} = 2.7 V	
					0.1	mA	VCC = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET, SR				–0.6 –1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		–60		– 150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			37	55	mA	V_{CC} = MAX	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters, or registers. In the MC74F160A and MC74F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations:

Count Enable = $\overline{CEP} \bullet CET \bullet \overline{PE}$

$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

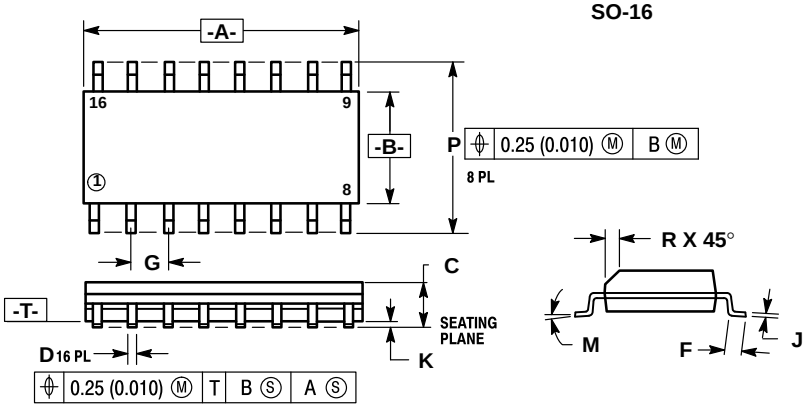
AC CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	100		90		MHz
t_{PLH}	Propagation Delay, Count	3.5	7.5	3.5	8.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	10	3.5	11	
t_{PLH}	Propagation Delay	3.5	8.5	3.5	9.5	
t_{PHL}	CP to Q_n ($\overline{PE}$ Input LOW)	4.0	8.5	4.0	9.5	
t_{PLH}	Propagation Delay	5.0	14	5.0	15	ns
t_{PHL}	CP to TC	4.5	14	4.5	15	
t_{PLH}	Propagation Delay	2.5	7.5	2.5	8.5	ns
t_{PHL}	CET to TC	2.5	7.5	2.5	8.5	
t_{PHL}	Propagation Delay MR to Q_n (MC74F160A)	5.5	12	5.5	13	ns
t_{PHL}	Propagation Delay MR to TC (MC74F160A)	4.5	10.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		74F T_A = 0°C to 70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	5.0		5.0		ns
$t_s(L)$	P_n to CP	5.0		5.0		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		
$t_h(L)$	P_n to CP	2.0		2.0		
$t_s(H)$	Setup Time, HIGH or LOW	11		11.5		ns
$t_s(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	8.5		9.5		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		
$t_h(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	0		0		
$t_s(H)$	Setup Time, HIGH or LOW	11		11.5		ns
$t_s(L)$	CEP or CET to CP	5.0		5.0		
$t_h(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	CEP or CET to CP	0		0		
$t_w(H)$	Clock Pulse Width (Load)	5.0		5.0		ns
$t_w(L)$	HIGH or LOW	5.0		5.0		
$t_w(H)$	Clock Pulse Width (Count)	4.0		4.0		ns
$t_w(L)$	HIGH or LOW	6.0		7.0		
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW (MC74F160A)	5.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP (MC74F160A)	6.0		6.0		

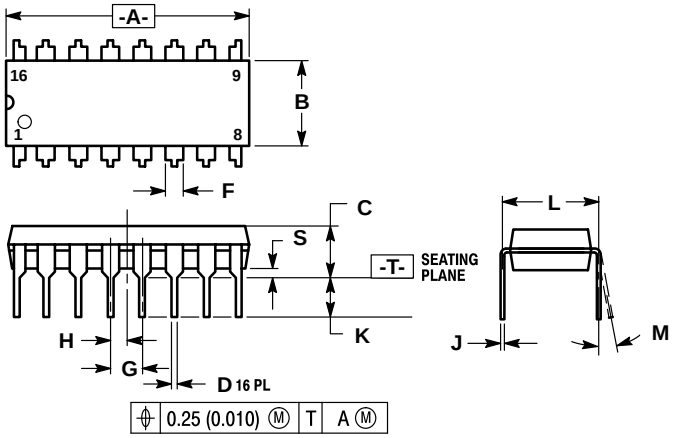
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

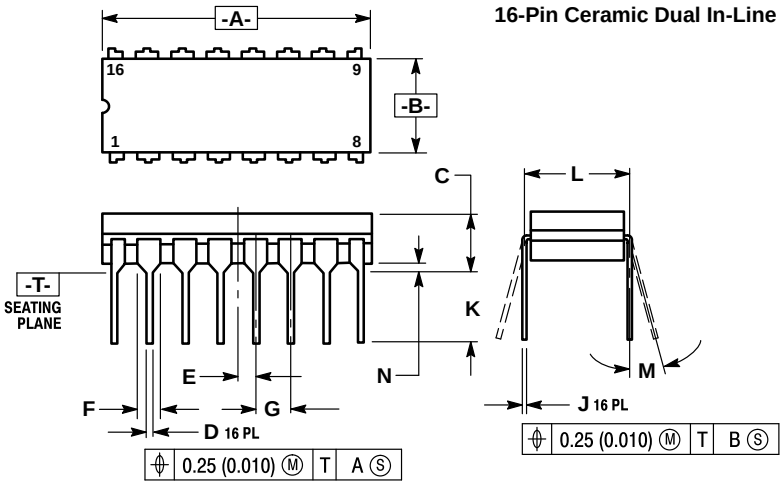
Case 648-08 N Suffix
16-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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