

Advance Information

Low-Voltage CMOS Octal Latching Transceiver

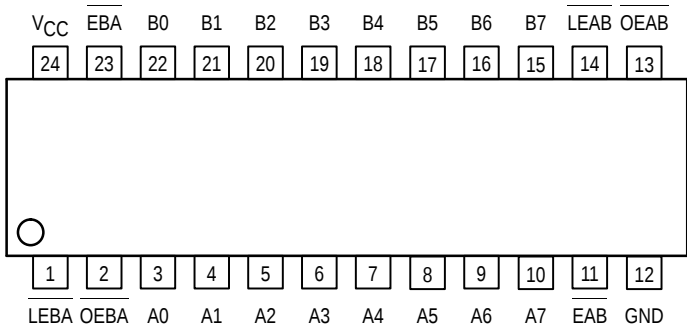
With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX543 is a high performance, non-inverting octal latching transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX543 inputs to be safely driven from 5V devices. The MC74LCX543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the EAB LOW, the A-to-B Output Enable (OEAB) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal will latch the A latches, and the outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the EBA, LEBA, and OEBA inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

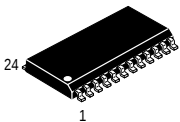
Pinout: 24-Lead Package (Top View)



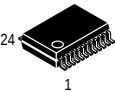
MC74LCX543

LCX

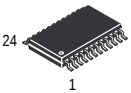
LOW-VOLTAGE CMOS
OCTAL LATCHING
TRANSCIVER



DW SUFFIX
PLASTIC SOIC
CASE 751E-04



SD SUFFIX
PLASTIC SSOP
CASE 940D-03



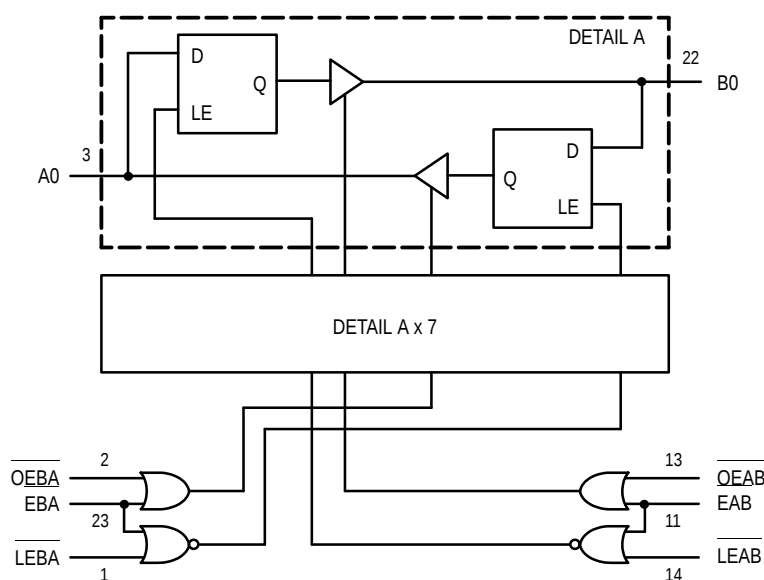
DT SUFFIX
PLASTIC TSSOP
CASE 948H-01

PIN NAMES

Pins	Function
OExx	Output Enable Inputs
Exx	Enable Inputs
LExx	Latch Enable Inputs
A0-A7	3-State Inputs/Outputs
B0-B7	3-State Inputs/Outputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEAB	OEBA	EAB	EBA	LEAB	LEBA	An	Bn	
H	H					Input	Input	
		X	X	X	X	X	X	Disable Outputs
		L	L	L	L	X	X	Transparent Data; Outputs Disabled
				H	H	l h	l h	Latch and Outputs Disabled
L	H					Input	Output	
		H	X*	L	X	l h	Z Z	Load and B Outputs Disabled
				H	X	X	Z	Hold; B Outputs Disabled
		L	X*	L	X	L H	L H	Transparent A to B
				H	X	l h	L H	Latch and Display B Outputs
H	L					Output	Input	
		X*	H	X	L	Z Z	l h	Load and A Outputs Disabled
				X	H	Z	X	Hold; A Outputs Disabled
		X*	L	X	L	L H	L H	Transparent B to A
				X	H	L H	l h	Latch and Display A Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; X = Don't Care; * = The latches are not internally gated with the Output Enables. Therefore, data at the A or B ports may enter the latches at any time, provided that the LExx and Exx pins are set accordingly. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
		$+50$	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to $+150$		$^{\circ}C$

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.0	3.3	3.6	V
	Operating Data Retention Only	1.5	3.3	3.6	
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3-State)	0		V_{CC}	V
		0		5.5	
I_{OH}	HIGH Level Output Current, $V_{CC} = 3.0V - 3.6V$			-24	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 3.0V - 3.6V$			24	mA
I_{OH}	HIGH Level Output Current, $V_{CC} = 2.7V - 3.0V$			-12	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 2.7V - 3.0V$			12	mA
T_A	Operating Free-Air Temperature	-40		$+85$	$^{\circ}C$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0V$	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7V$; $I_{OH} = -12mA$	2.2		
		$V_{CC} = 3.0V$; $I_{OH} = -18mA$	2.4		
		$V_{CC} = 3.0V$; $I_{OH} = -24mA$	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		$V_{CC} = 2.7V$; $I_{OL} = 12mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 16mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 24mA$		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
I _I	Input Leakage Current	2.7V ≤ V _{CC} ≤ 3.6V; 0V ≤ V _I ≤ 5.5V		±5.0	μA
I _{OZ}	3-State Output Current	2.7 ≤ V _{CC} ≤ 3.6V; 0V ≤ V _O ≤ 5.5V; V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0V; V _I or V _O = 5.5V		10	μA
I _{CC}	Quiescent Supply Current	2.7 ≤ V _{CC} ≤ 3.6V; V _I = GND or V _{CC}		10	μA
		2.7 ≤ V _{CC} ≤ 3.6V; 3.6 ≤ V _I or V _O ≤ 5.5V		±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 ≤ V _{CC} ≤ 3.6V; V _{IH} = V _{CC} - 0.6V		500	μA

AC CHARACTERISTICS (Note 3.; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T _A = −40°C to +85°C				
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay An to Bn or Bn to An	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	ns
t _{PLH} t _{PHL}	<u>Propagation Delay</u> LEBA to An or LEAB to Bn	4	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t _{pZH} t _{pZL}	<u>Output Enable Time</u> OEBA to An or OEAB to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t _{PHZ} t _{PLZ}	<u>Output Disable Time</u> OEBA to An or OEAB to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t _{pZH} t _{pZL}	<u>Output Enable Time</u> EBA to An or EAB to Bn	2	1.5 1.5	9.0 9.0	1.5 1.5	10.0 10.0	ns
t _{PHZ} t _{PLZ}	<u>Output Disable Time</u> EBA to An or EAB to Bn	2	1.5 1.5	7.0 7.0	1.5 1.5	7.5 7.5	ns
t _s	Setup Time, HIGH to LOW Data to LExx	4	2.5		2.5		ns
t _h	Hold Time, HIGH to LOW Data to LExx	4	1.5		1.5		ns
t _s	Setup Time, HIGH to LOW Data to Exx	4	2.5		2.5		ns
t _h	Hold Time, HIGH to LOW Data to Exx	4	1.5		1.5		ns
t _w	Latch Enable or Enable Pulse Width, LOW	4	3.3		3.3		ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 4.)			1.0 1.0			ns

3. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

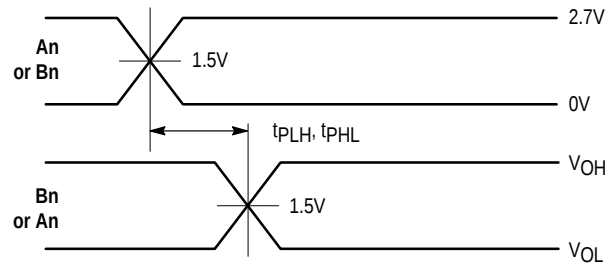
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 5.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 5.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V

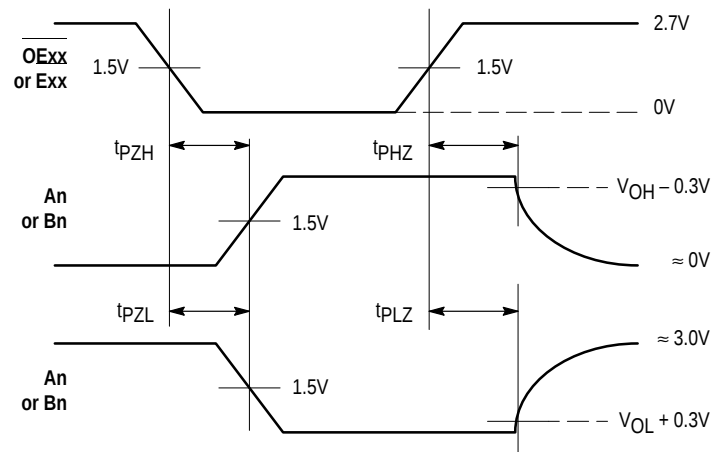
5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF



WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS

 $t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$


WAVEFORM 2 – OExx/Exx to A or B OUTPUT ENABLE AND DISABLE TIMES

 $t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$

Figure 1. AC Waveforms

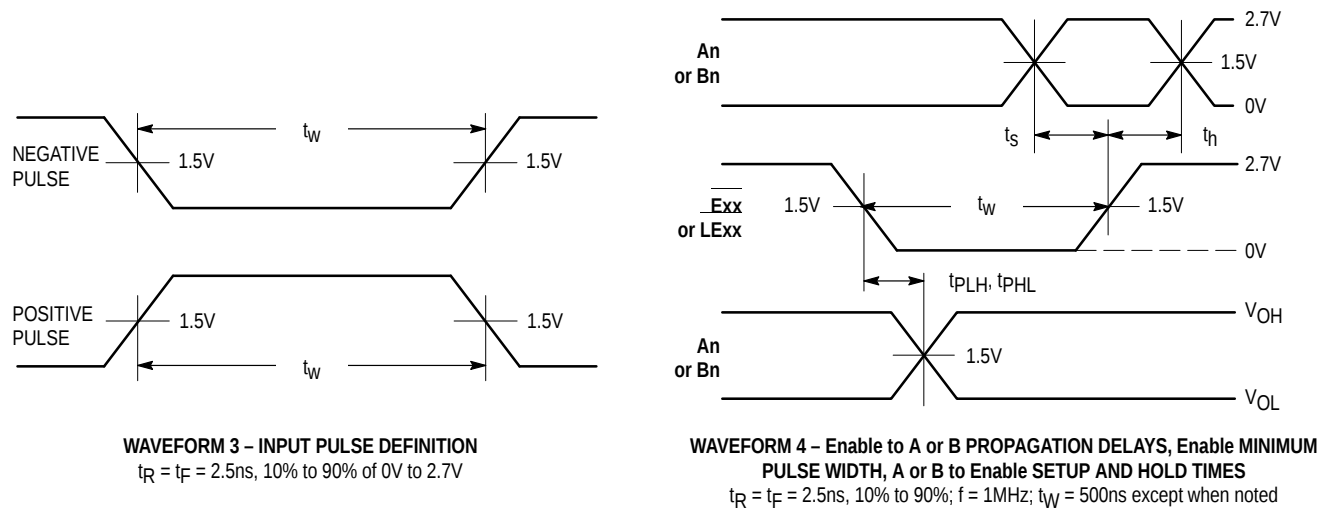


Figure 2. AC Waveforms (continued)

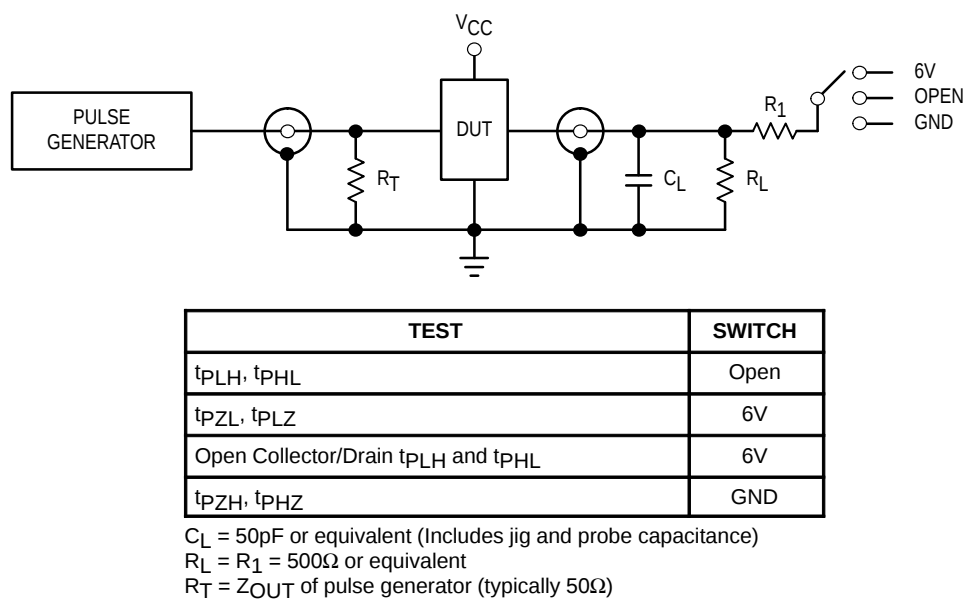
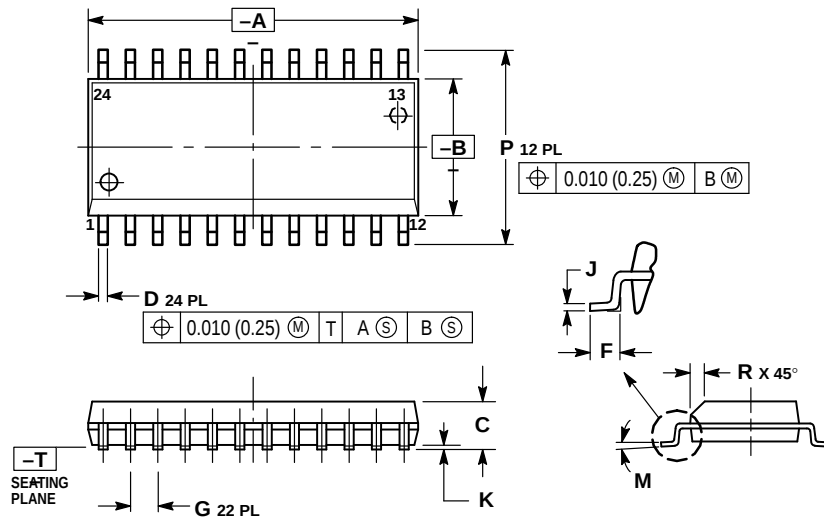


Figure 3. Test Circuit

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E-04
ISSUE E

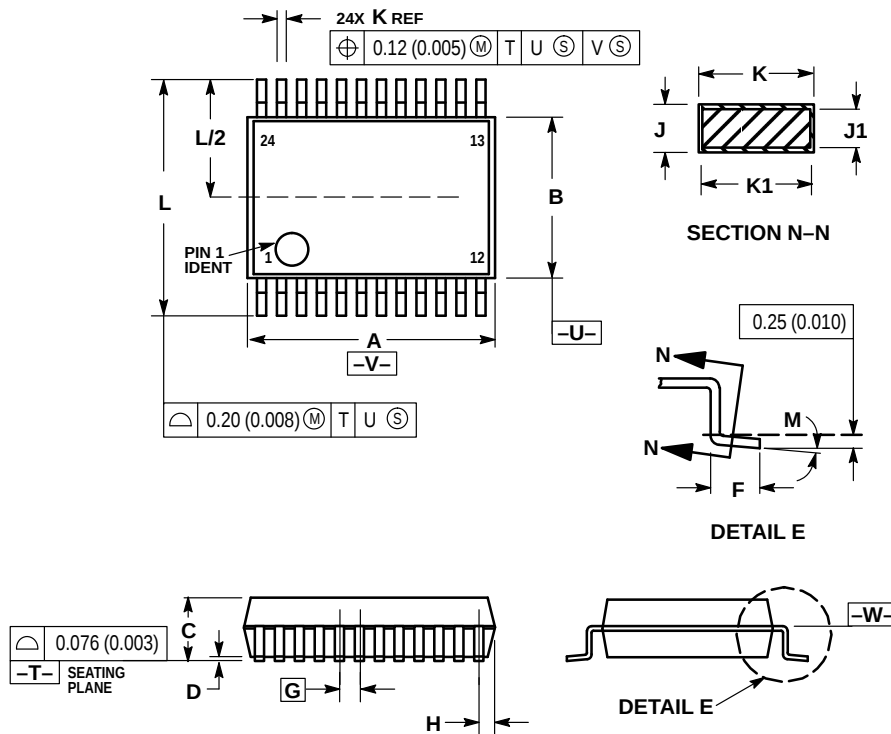


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D-03
ISSUE B



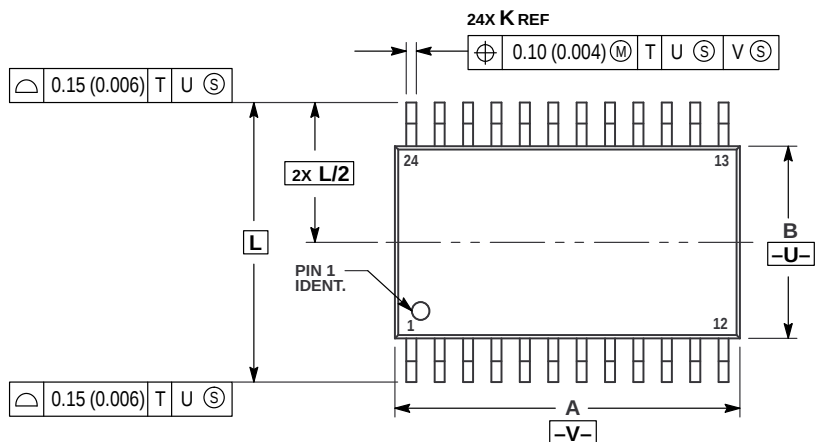
NOTES:

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
8. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
9. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
10. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

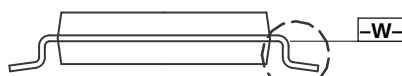
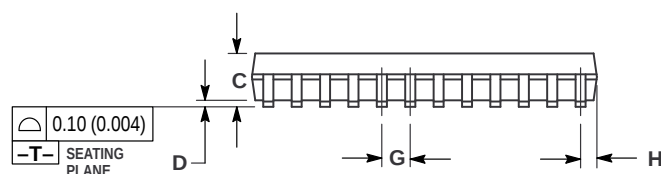
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H-01
ISSUE O



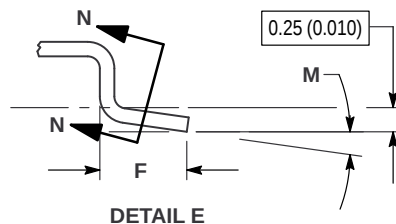
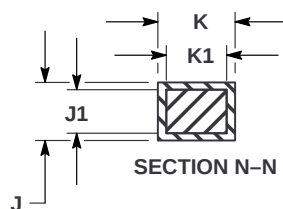
NOTES:

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- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



DETAIL E



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MOTOROLA
