

PH3230S

N-channel TrenchMOS™ logic level FET

Rev. 01 — 12 February 2003

Preliminary data

1. Description

The latest generation N-channel enhancement mode field-effect power transistor in a SOT669 (LFPACK) package.

Product availability:

PH3230S in SOT669 (LFPACK).

2. Features

- Logic level compatible
- Low drive current
- High density mounting
- Very low on-state resistance.

3. Applications

- DC-to-DC converter
- Computer motherboards
- Switched mode power supplies.

4. Pinning information

Table 1: Pinning - SOT669 (LFPACK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	Top view MBL286	MBB076
4	gate (g)		
mb	drain (d)		



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$	-	107	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	62.5	W
T_j	junction temperature		-	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	2.7	3.2	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	5.0	6.5	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

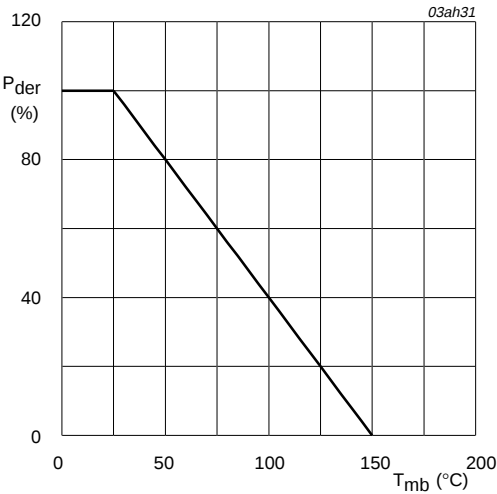
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25\text{ to }150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; Figure 2 and 3	-	107	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ μs}$; Figure 3	-	428	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

Source-drain diode

I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ μs}$	-	107	A
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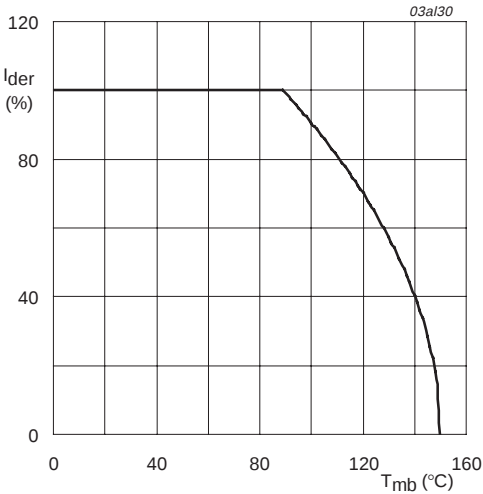
Avalanche ruggedness

$I_{DS(AL)R}$	repetitive drain-source avalanche current	$T_j = 25\text{ °C}$	-	5	A
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	$T_j = 25\text{ °C}$; $R_{GS} \geq 50\text{ Ω}$; $I_{DS(AL)R} = 5\text{ A}$; $V_{DD} = 15\text{ V}$; duty < 0.1%	-	2.5	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

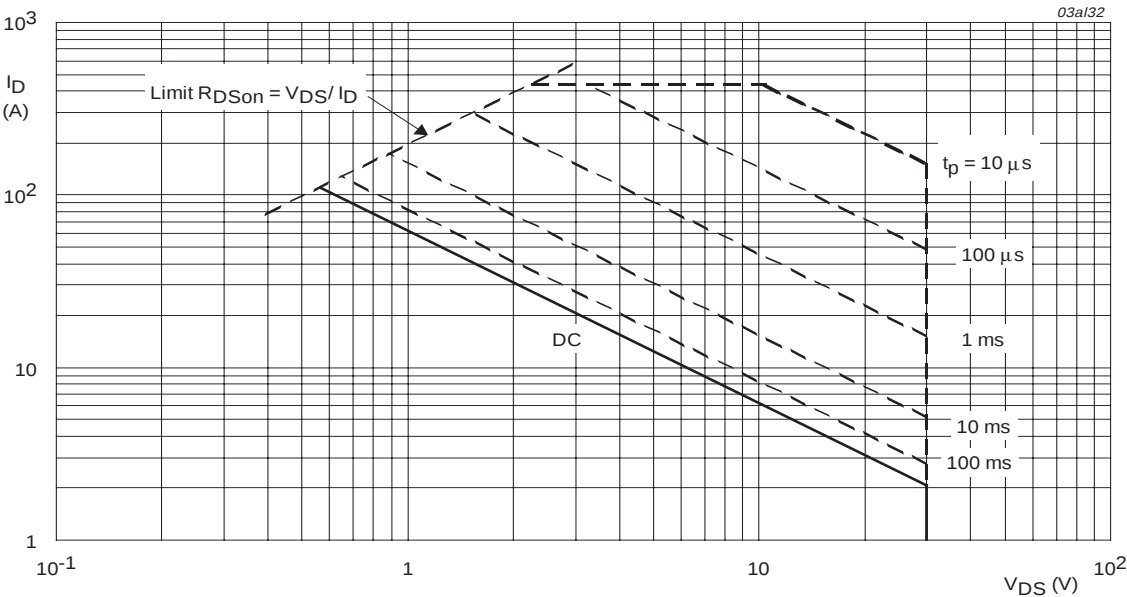
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse.

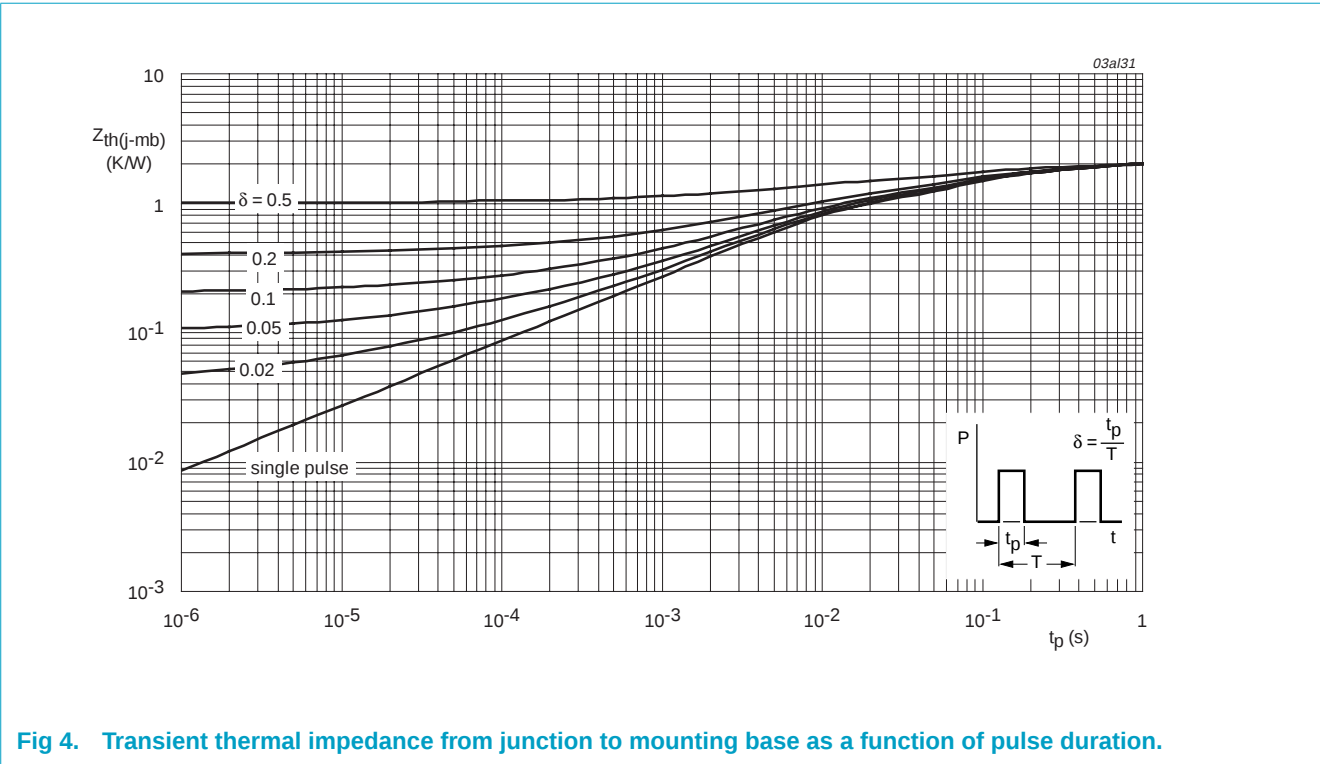
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

7.1 Transient thermal impedance



8. Characteristics

Table 5: Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 mA; V _{GS} = 0 V	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9	1	2	3	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V	-	-	1	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; Figure 7 and 8	-	2.7	3.2	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; Figure 8	-	5.0	6.5	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 25 A; Figure 11	39	55	-	S
Q _{g(tot)}	total gate charge	I _D = 50 A; V _{DD} = 10 V; V _{GS} = 5 V; Figure 14	-	42	-	nC
Q _{gs}	gate-source charge		-	21	-	nC
Q _{gd}	gate-drain (Miller) charge		-	13	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; Figure 12	-	4100	-	pF
C _{oss}	output capacitance		-	1150	-	pF
C _{rss}	reverse transfer capacitance		-	750	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 10 V; I _D = 25 A; V _{GS} = 10 V; R _G = 4.7 Ω	-	14	-	ns
t _r	rise time		-	145	-	ns
t _{d(off)}	turn-off delay time		-	85	-	ns
t _f	fall time		-	50	-	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 50 A; V _{GS} = 0 V; Figure 13	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 50 A; dI _S /dt = −50 A/μs; V _{GS} = 0 V	-	46	-	ns

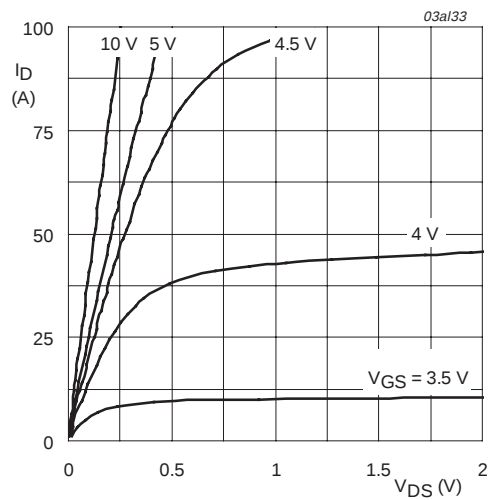


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.

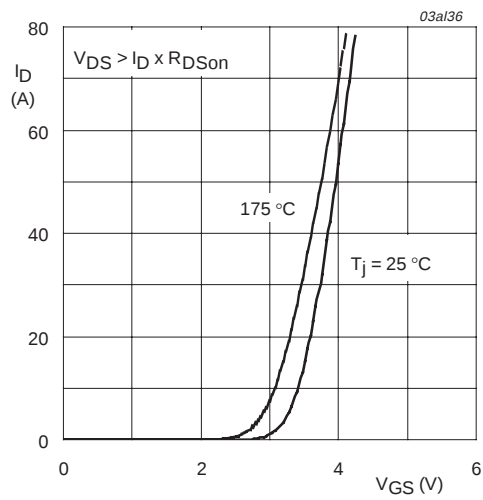


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.

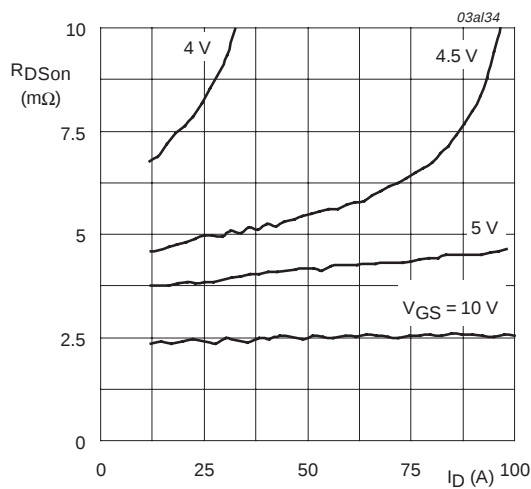


Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

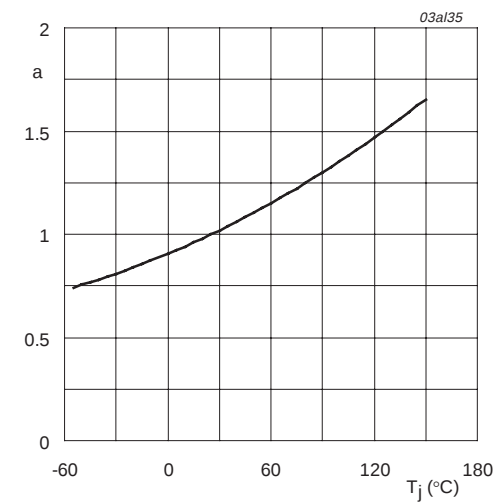
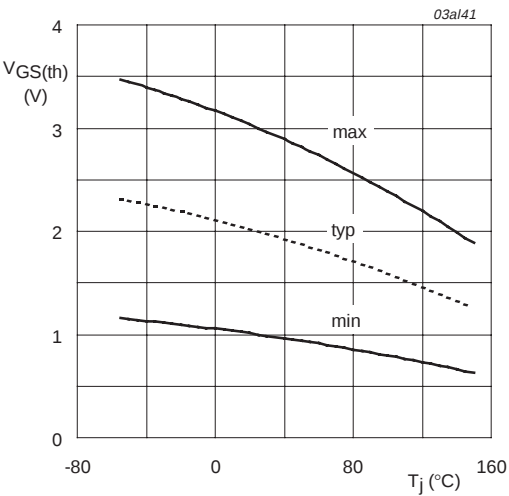
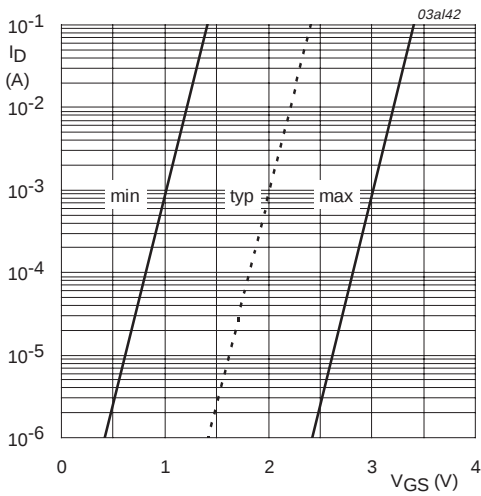


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



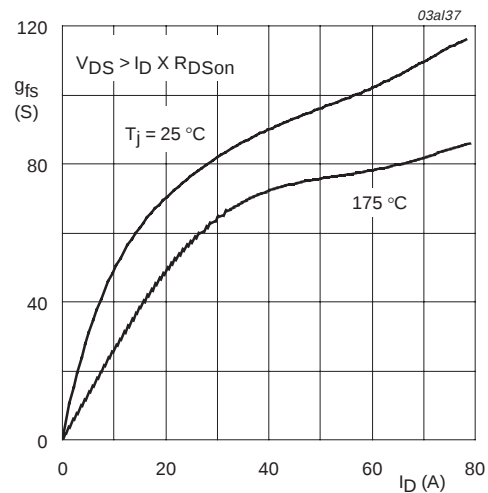
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



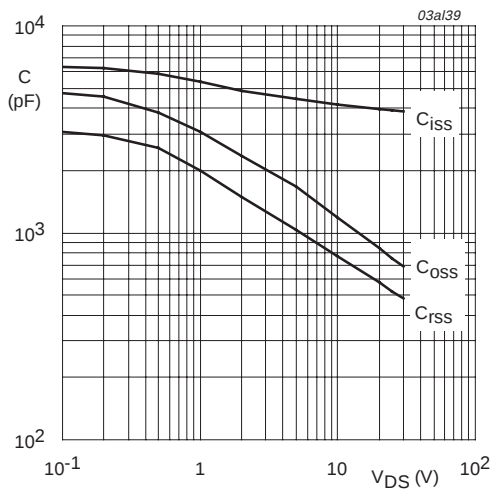
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



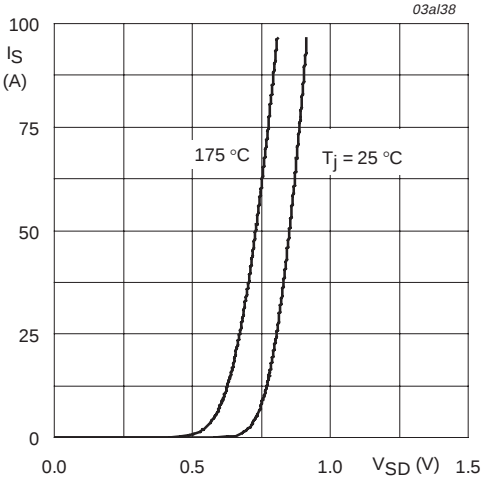
$T_j = 25 \text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DS(on)}$

Fig 11. Forward transconductance as a function of drain current; typical values.



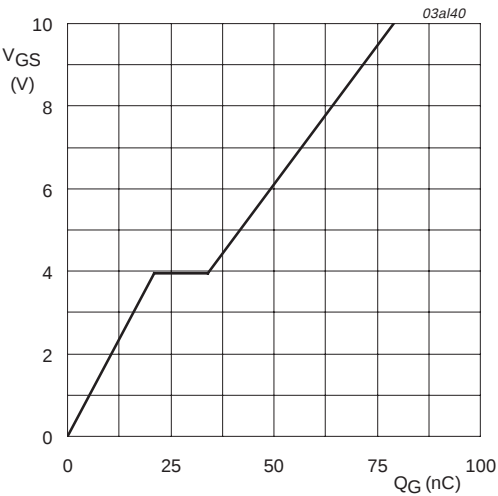
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_J = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



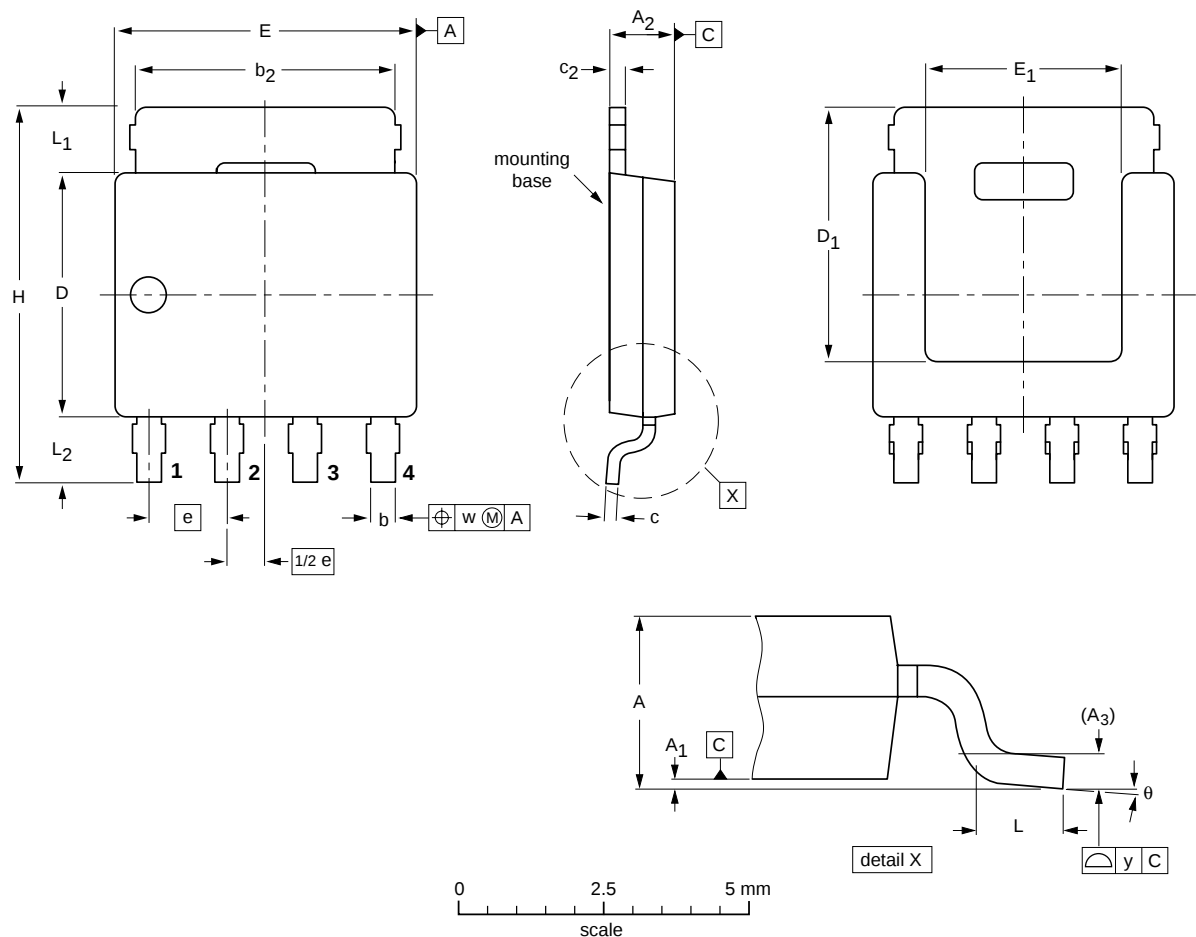
$T_J = 25^\circ\text{C}$; $I_D = 50\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version LFAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ max	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				02-07-10 03-02-05

Fig 15. SOT669 (LFAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20030212	-	Preliminary data (9397 750 11078)

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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