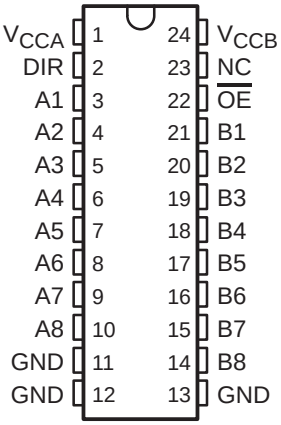
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port, V_{CCA}, is dedicated to accept a 5-V supply level, and the configurable B port, which is designed to track V_{CCB}, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

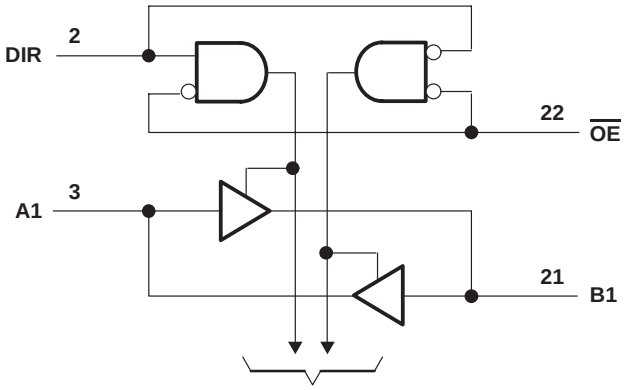
The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC4245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}		–0.5 V to 6 V
Input voltage range, V_I (see Note 1):	I/O ports (A port)	–0.5 V to V_{CCA} + 0.5 V
	I/O ports (B port)	–0.5 V to V_{CCB} + 0.5 V
	Except I/O ports	–0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 1):	A port	–0.5 V to V_{CCA} + 0.5 V
	B port	–0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)		–50 mA
Output clamp current, I_{OK} (V_O < 0)		–50 mA
Continuous output current, I_O		±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage				4.5	5	5.5	V
V_{CCB}	Supply voltage				2.7	3.3	5.5	V
V_{IHA}	High-level input voltage	$V_{OB} \le 0.1$ V, $V_{OB} \ge V_{CCB} - 0.1$ V	4.5 V	2.7 V	2			V
				3.6 V	2			
			5.5 V	5.5 V	2			
V_{IHB}	High-level input voltage	$V_{OA} \le 0.1$ V, $V_{OA} \ge V_{CCA} - 0.1$ V	4.5 V	2.7 V	2			V
				3.6 V	2			
			5.5 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	$V_{OB} \le 0.1$ V, $V_{OB} \ge V_{CCB} - 0.1$ V	4.5 V	2.7 V			0.8	V
				3.6 V			0.8	
			5.5 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	$V_{OA} \le 0.1$ V, $V_{OA} \ge V_{CCA} - 0.1$ V	4.5 V	2.7 V			0.8	V
				3.6 V			0.8	
			5.5 V	5.5 V			1.65	
V_{IA}	Input voltage				0		V_{CCA}	V
V_{IB}	Input voltage				0		V_{CCB}	V
V_{OA}	Output voltage				0		V_{CCA}	V
V_{OB}	Output voltage				0		V_{CCB}	V
I_{OHA}	High-level output current		4.5 V	3 V			–24	mA
I_{OHB}	High-level output current		4.5 V	2.7 V to 4.5 V			–24	mA
I_{OLA}	Low-level output current		4.5 V	3 V			24	mA
I_{OLB}	Low-level output current		4.5 V	2.7 V to 4.5 V			24	mA
T_A	Operating free-air temperature				–40		85	°C

NOTE 3: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 μA	4.5 V	3 V	4.4	4.49		V
		I_{OH} = –24 mA	4.5 V	3 V	3.76	4.25		
V_{OHB}		I_{OH} = –100 μA	4.5 V	3 V	2.9	2.99		V
		I_{OH} = –12 mA	4.5 V	2.7 V	2.2	2.5		
				3 V	2.46	2.85		
		I_{OH} = –24 mA	4.5 V	2.7 V	2.1	2.3		
				3 V	2.25	2.65		
				4.5 V	3.76	4.25		
V_{OLA}		I_{OL} = 100 μA	4.5 V	3 V			0.1	V
		I_{OL} = 24 mA	4.5 V	3 V		0.21	0.44	
V_{OLB}		I_{OL} = 100 μA	4.5 V	3 V			0.1	V
		I_{OL} = 12 mA	4.5 V	2.7 V		0.11	0.44	
		I_{OL} = 24 mA	4.5 V	2.7 V		0.22	0.5	
				3 V		0.21	0.44	
				4.5 V		0.18	0.44	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	5.5 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I_{OZ}†	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}	5.5 V	3.6 V		±0.5	±5	μA
I_{CCA}	B to A	$A_n = V_{CC}$ or GND	5.5 V	Open		8	80	μA
		$I_{O(A\ port)}$ = 0, $B_n = V_{CCB}$ or GND	5.5 V	3.6 V		8	80	
				5.5 V		8	80	
I_{CCB}	A to B	$A_n = V_{CCA}$ or GND, $I_{O\ (B\ port)}$ = 0	5.5 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI_{CCA}‡	A port	$\overline{V_I} = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	5.5 V	5.5 V		1.35	1.5	mA
	$\overline{OE}$	$V_I = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA} or GND	5.5 V	5.5 V		1	1.5	
	DIR	$\overline{V_I} = V_{CCA}$ – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at V_{CCA} or GND	5.5 V	3.6 V		1	1.5	
ΔI_{CCB}‡	B port	$\overline{V_I} = V_{CCB}$ – 0.6 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	5.5 V	3.6 V		0.35	0.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open	Open		5		pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND	5 V	3.3 V		11		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the associated V_{CC}.

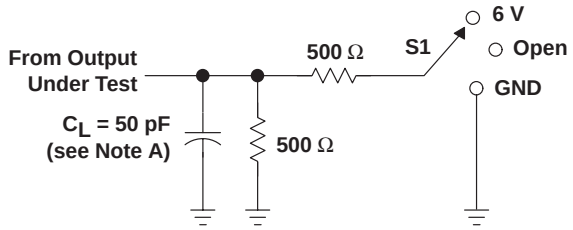
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V TO 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	7.1	1	7	ns
t_{PLH}			1	6	1	7	
t_{PHL}	B	A	1	6.8	1	6.2	ns
t_{PLH}			1	6.1	1	5.3	
t_{PZL}	$\overline{OE}$	A	1	9	1	9	ns
t_{PZH}			1	8.3	1	8	
t_{PZL}	$\overline{OE}$	B	1	8.2	1	10	ns
t_{PZH}			1	8.1	1	10.2	
t_{PLZ}	$\overline{OE}$	A	1	4.7	1	5.2	ns
t_{PHZ}			1	4.9	1	5.2	
t_{PLZ}	$\overline{OE}$	B	1	5.4	1	5.4	ns
t_{PHZ}			1	6.3	1	7.4	

operating characteristics, V_{CCA} = 5 V, V_{CCB} = 3.3 V, T_A = 25°C

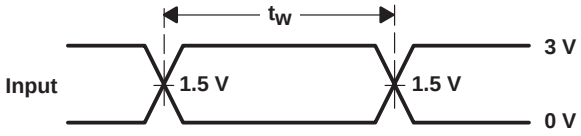
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0,	f = 10 MHz	20	pF
		Outputs disabled			6.5	

PARAMETER MEASUREMENT INFORMATION FOR A TO B
V_{CCA} = 4.5 V TO 5.5 V AND V_{CCB} = 2.7 V TO 3.6 V

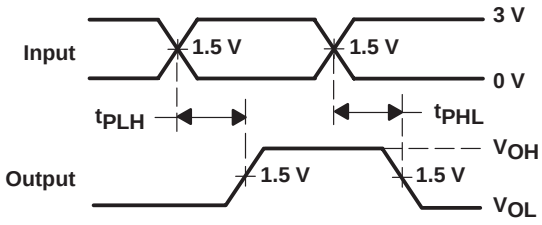


LOAD CIRCUIT

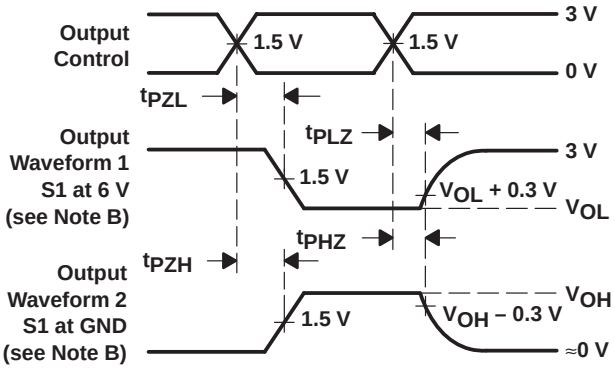
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

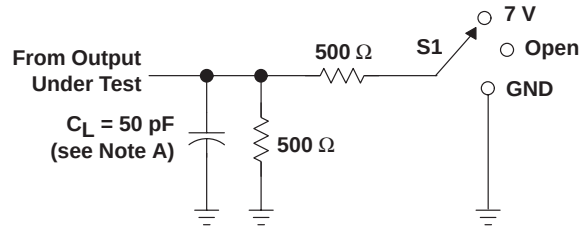


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

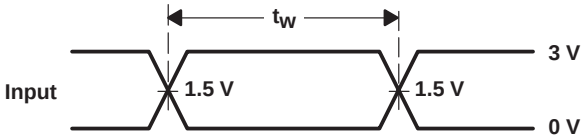
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A TO B
V_{CCA} = 4.5 V TO 5.5 V AND V_{CCB} = 3.6 V TO 5.5 V

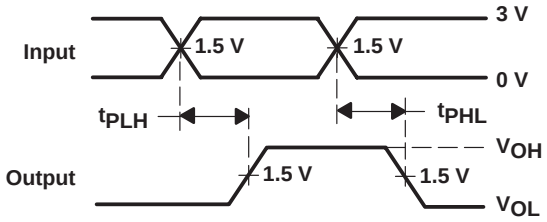


LOAD CIRCUIT

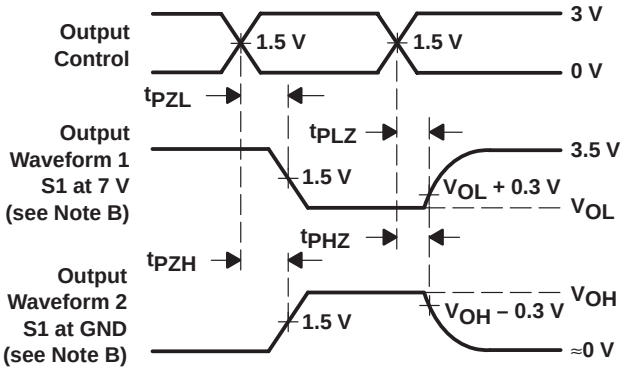
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



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ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
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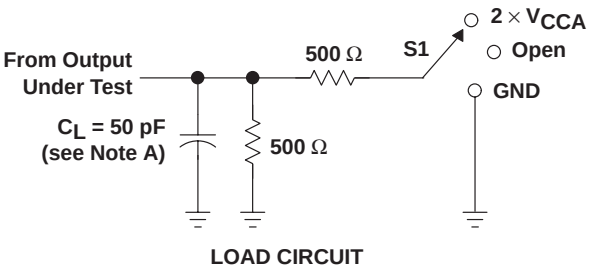
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

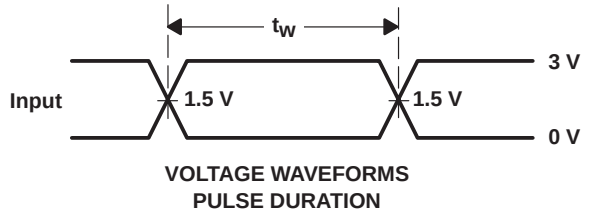
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B TO A
V_{CCA} = 4.5 V TO 5.5 V AND V_{CCB} = 2.7 V TO 3.6 V

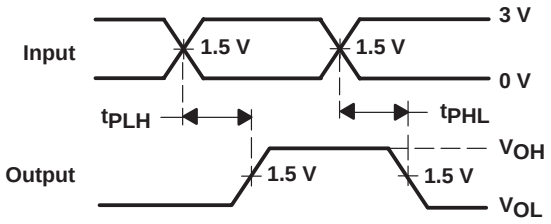


LOAD CIRCUIT

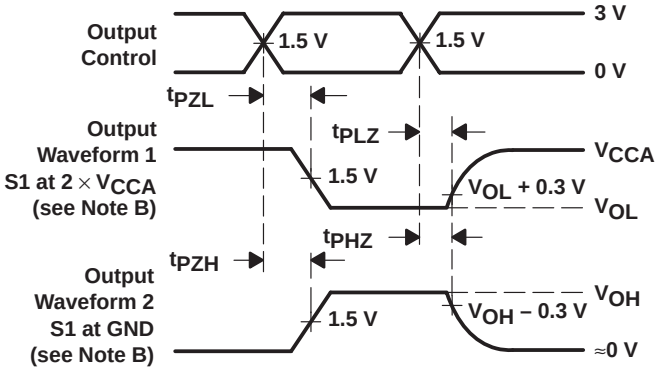
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCA}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



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ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
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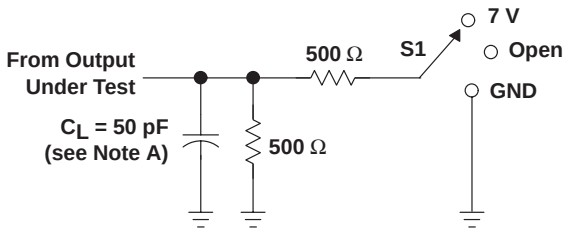
D. The outputs are measured one at a time with one transition per measurement.

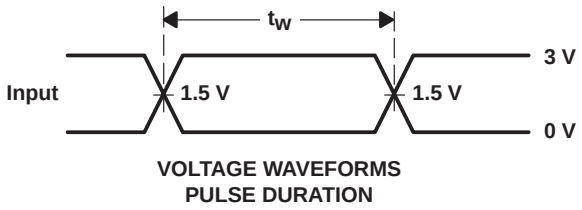
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B TO A
V_{CCA} = 4.5 V TO 5.5 V AND V_{CCB} = 3.6 V TO 5.5 V

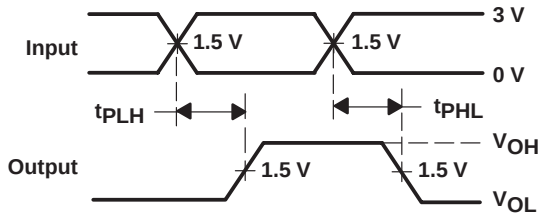


LOAD CIRCUIT

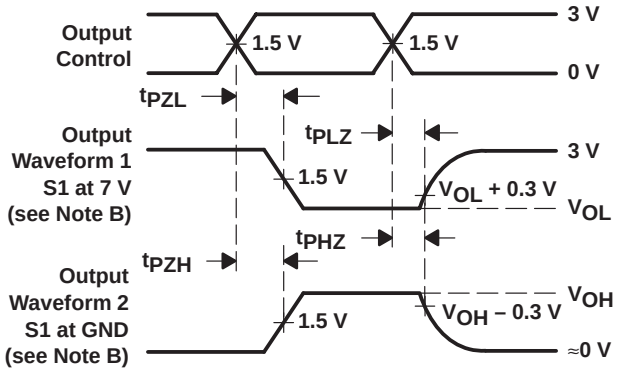
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
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C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

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