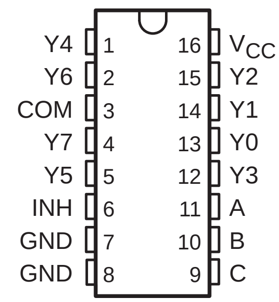
- ***EPIC*** **™ (Enhanced-Performance Implanted CMOS) Process**
- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, and Standard Plastic (N) and Ceramic (J) DIPs**

SN54LV4051A . . . J OR W PACKAGE
SN74LV4051A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



description

These 8-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV4051A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

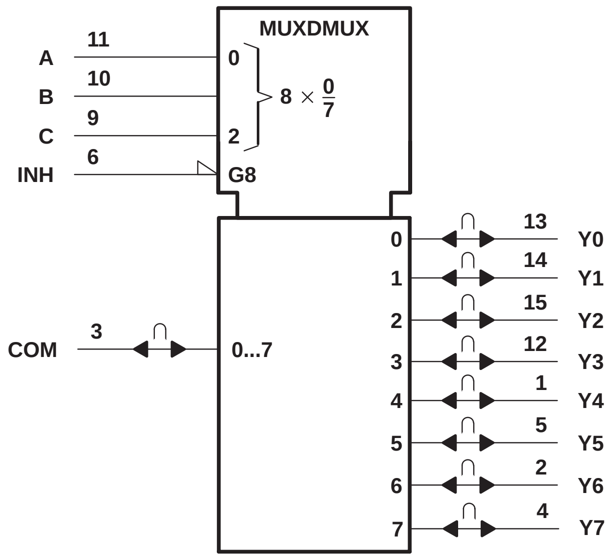
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The SN54LV4051A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV4051A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

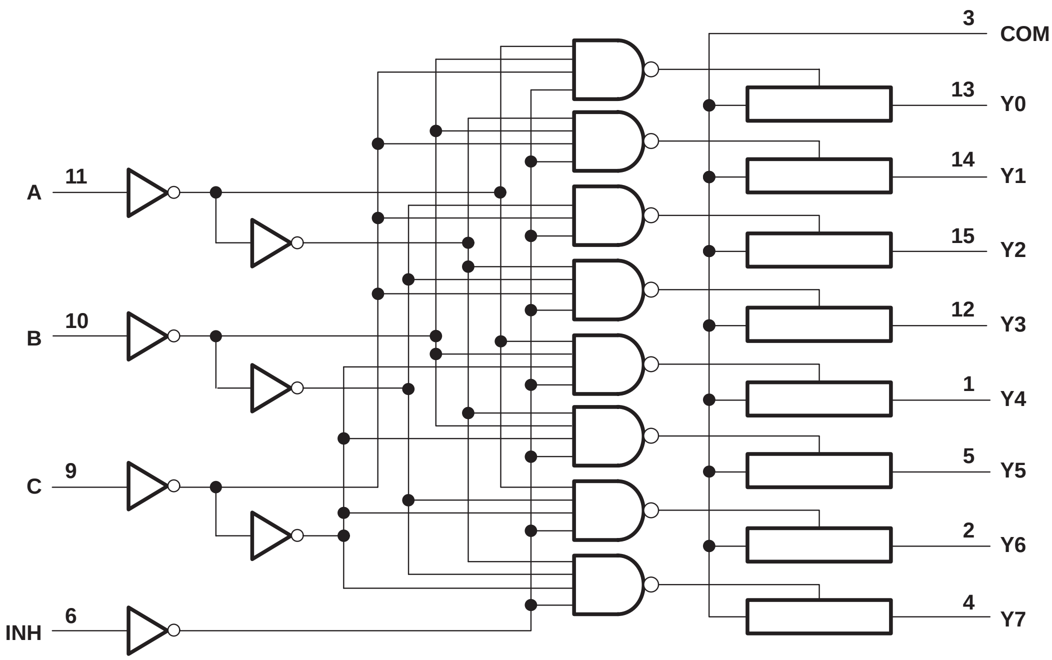
INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . –0.5 V to 7.0 V
Input voltage range, V_I (see Note 1) . . . –0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2) . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . –20 mA
I/O diode current, I_{IOK} (V_{IO} < 0 or V_{IO} > V_{CC}) . . . ±50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC}) . . . ±25 mA
Continuous current through V_{CC} or GND . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . 73°C/W
DB package . . . 82°C/W
DGV package . . . 120°C/W
N package . . . 67°C/W
NS package . . . 64°C/W
PW package . . . 108°C/W
Storage temperature range, T_{stg} . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV4051A		SN74LV4051A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
R_{on}	On-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 1)	2.3 V		38	180		225		225	Ω
			3 V		30	150		190		190	
			4.5 V		22	75		100		100	
$R_{on(p)}$	Peak on-state resistance	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	2.3 V		113	500		600		600	Ω
			3 V		54	180		225		225	
			4.5 V		31	100		125		125	
ΔR_{on}	Difference in on-state resistance between switches	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	2.3 V		2.1	30		40		40	Ω
			3 V		1.4	20		30		30	
			4.5 V		1.3	15		20		20	
I_I	Control input current	V_I = V_{CC} or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{soff}	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} (see Figure 2)	5.5V			±0.1		±1		±1	µA
I_{son}	On-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5 V					20		20	µA
C_{IC}	Control input capacitance	f = 10 MHz	3.3 V		2						pF
C_{IS}	Common terminal capacitance		3.3 V		23.4						pF
C_{OS}	Switch terminal capacitance		3.3 V		5.7						pF
C_T	Feedthrough capacitance		3.3 V		0.5						pF

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.9	10		16		16	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		6.6	18		23		23	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.4	18		23		23	ns
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 5)		3.8	12		18		18	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		7.8	28		35		35	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		11.5	28		35		35	ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.2	6		10		10	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.7	12		15		15	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		5.7	12		15		15	ns
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		2.5	9		12		12	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		5.5	20		25		25	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.8	20		25		25	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		0.6	4		7		7	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		3.5	8		10		10	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.4	8		10		10	ns
t_{PLH}, t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		1.5	6		8		8	ns
t_{PZH}, t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		4	14		18		18	ns
t_{PHZ}, t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.2	14		18		18	ns

analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

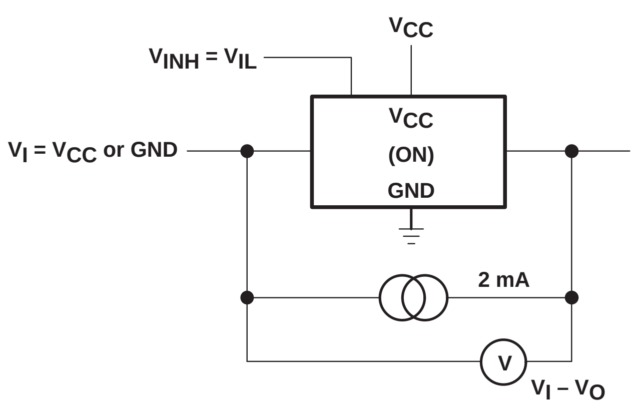
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	$C_L = 50$ pF, $R_L = 600\ \Omega$, $f_{in} = 1$ MHz (sine wave) (see Note 5 and Figure 6)		2.3 V		20		MHz
					3 V		25		
					4.5 V		35		
Crosstalk (control input to signal output)	INH	COM or Yn	$C_L = 50$ pF, $R_L = 600\ \Omega$, $f_{in} = 1$ MHz (square wave) (see Figure 7)		2.3 V		20		mV
					3 V		35		
					4.5 V		60		
Feed-through attenuation (switch off)	COM or Yn	Yn or COM	$C_L = 50$ pF, $R_L = 600\ \Omega$, $f_{in} = 1$ MHz (see Note 6 and Figure 8)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Sine-wave distortion	COM or Yn	Yn or COM	$C_L = 50$ pF, $R_L = 10\ k\Omega$, $f_{in} = 1$ kHz (sine wave) (see Figure 9)	$V_I = 2\ V_{p-p}$	2.3 V		0.1		
				$V_I = 2.5\ V_{p-p}$	3 V		0.1		
				$V_I = 4\ V_{p-p}$	4.5 V		0.1		

NOTES: 5. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads –3 dB.
6. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, $V_{CC} = 3.3$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50$ pF, f = 10 MHz	5.9	pF

PARAMETER MEASUREMENT INFORMATION



$$R_{ON} = \frac{V_I - V_O}{2 \times 10^{-3}}\ \Omega$$

Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION

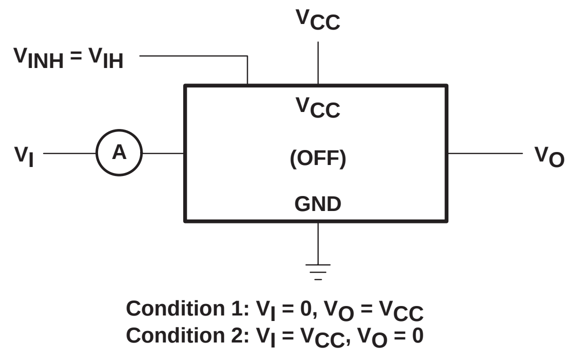


Figure 2. Off-State Switch Leakage-Current Test Circuit

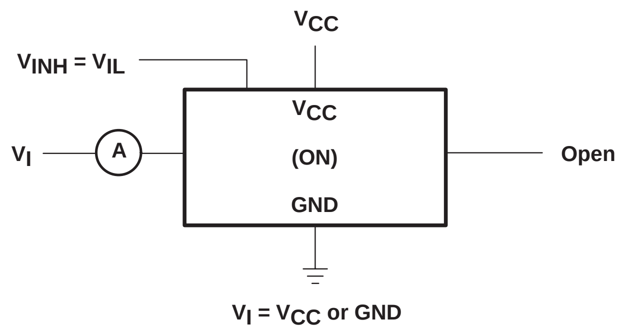


Figure 3. On-State Switch Leakage-Current Test Circuit

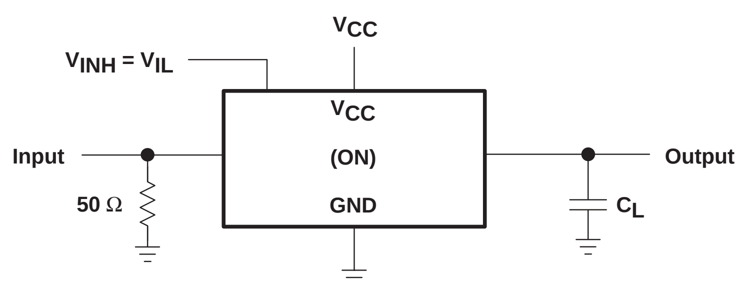
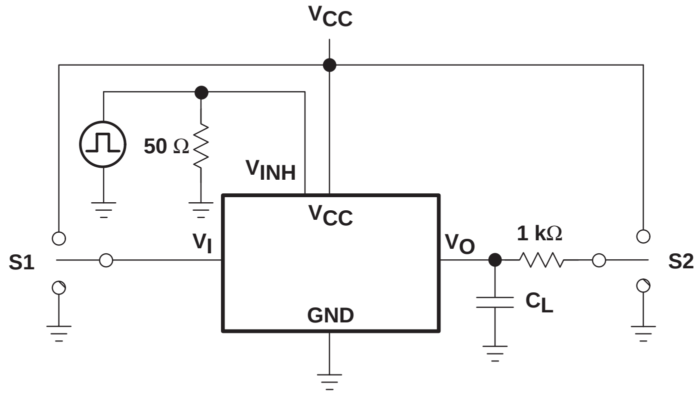


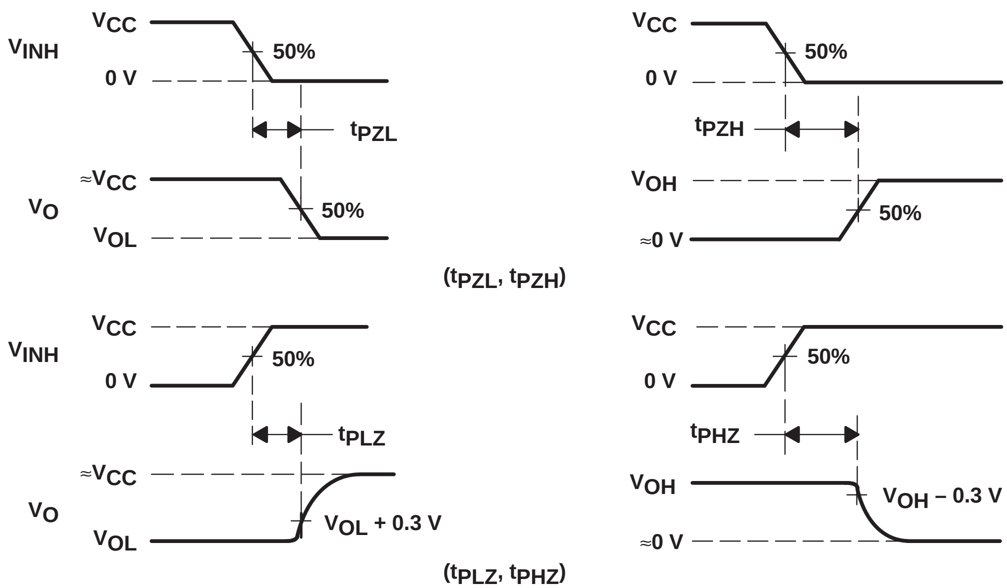
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



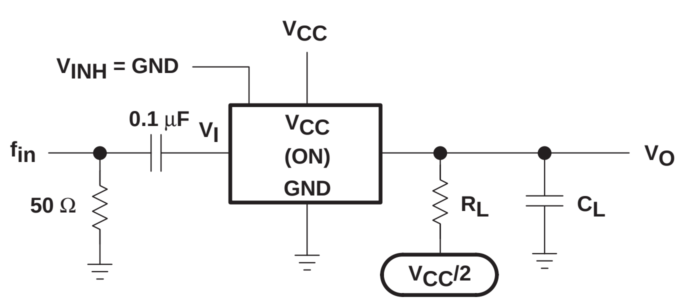
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

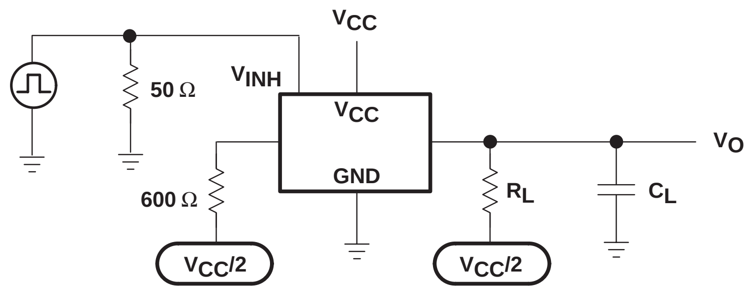


Figure 7. Crosstalk (Control Input, Switch Output)

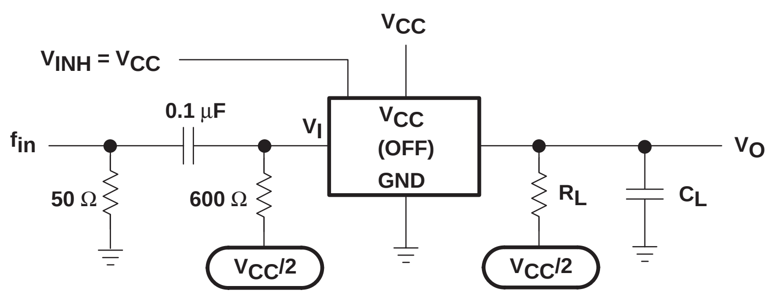


Figure 8. Feedthrough Attenuation (Switch Off)

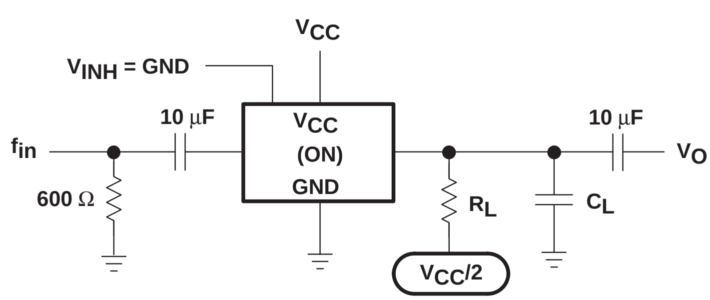


Figure 9. Sine-Wave Distortion