TEXAS INSTRUMENTS

PCI2050
Evaluation Module

User's Guide

2000

PCIBus Solutions

SCPU006

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Preface

Read This First

About This Manual

This manual is designed to assist the user of the PCI2050 evaluation module (EVM). It provides descriptions of parts, features, and operating requirements of the EVM that are necessary or useful to obtain maximum benefit from EVM use.

How to Use This Manual

This document contains the following chapters:

Chapter 1, *Introduction*, provides a brief description of the EVM, and a bill of materials for the EVM kit.

Chapter 2, *Software Requirements*, details the minimum software requirements for any PC system on which the PCI2050 EVM is to be run.

Chapter 3, *Configuration*, explains secondary bus masters and interrupt routing as related to the edge connectors on the board.

Chapter 4, *Board Configuration*, describes the location and purpose of board components such as pins, jumpers, connectors, and LEDs.

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

PCI2050 PCI-to-PCI Bridge Data Manual, TI Literature Number – SCPS053

PCI2050 Implementation Guide, TI Literature Number – SCPU009

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Chapter 1

Introduction

This chapter provides a brief overview of the PCI2050 evaluation module, along with a bill of materials for the EVM kit.

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1.1 Introduction

This document is intended to assist the user of the PCI2050 evaluation module (EVM), EVM2050A. Included within this document are instructions detailing the proper setup and configuration necessary to operate the PCI2050 EVM. The PCI2050 EVM is a universal add-in card and can be used in either 3.3-V or 5-V signaling environments.

1.2 Evaluation Kit Bill of Materials

The PCI2050 EVM consists of the following items:

Item	Nomenclature	Quantity
EVM2050A	PCI to PCI Adapter Card Assembly	1
3.5” Diskette	PCIBus and PCIBus95 Utility Programs	1

Chapter 2

Software Requirements

This chapter provides the minimum software requirements for any PC system on which the PCI2050 EVM is to be used.

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2.1 Software Requirements

The EVM2050A evaluation board will work in any system that meets the following requirements:

1) BIOS which supports the *PCI Bridge Specification 1.0*.

2) Operating system that supports the *PCI Bridge Specification 1.0*.

In the majority of today's computer systems, bridge support is built into the BIOS. Many operating systems, like Windows™ 95/98 and Windows NT™, have support for bridges.

Chapter 3

Configuration

This chapter explains secondary bus masters and interrupt routing as related to edge connectors on the board.

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3.1 Configuration

The PCI2050 supports nine secondary bus masters. Due to board space, only three masters are supported with the EVM2050A board. The three supported masters can be plugged into three edge connectors labeled P1, P2, and P3. These edge connectors are configured as listed in Table 3–1.

Table 3–1. Edge Connector Device ID

Edge Connector	Resistor Installed	Slot ID
P1	R19	0
	R20 (default)	4 (default)
	R21	8
P2	R22 (default)	1 (default)
	R23	5
	R24	9
P3	R25 (default)	2 (default)
	R26	6
	R27	A

The interrupts for each connector on the secondary bus are routed according to the PCI Local Bus Specification 2.2, subsection 2.2.6. Table 3–2 depicts how the interrupts are routed on the EVM2050A evaluation board.

Table 3–2. Edge Connector Interrupt Routing

Edge Connector	Interrupt	Routed on INTX on PI
P1	$\overline{\text{INTA}}$	$\overline{\text{INTA}}$
	$\overline{\text{INTB}}$	$\overline{\text{INTB}}$
	$\overline{\text{INTC}}$	$\overline{\text{INTC}}$
	$\overline{\text{INTD}}$	$\overline{\text{INTD}}$
P2	$\overline{\text{INTA}}$	$\overline{\text{INTB}}$
	$\overline{\text{INTB}}$	$\overline{\text{INTC}}$
	$\overline{\text{INTC}}$	$\overline{\text{INTD}}$
	$\overline{\text{INTD}}$	$\overline{\text{INTA}}$
P3	$\overline{\text{INTA}}$	$\overline{\text{INTC}}$
	$\overline{\text{INTB}}$	$\overline{\text{INTD}}$
	$\overline{\text{INTC}}$	$\overline{\text{INTA}}$
	$\overline{\text{INTD}}$	$\overline{\text{INTB}}$

Chapter 4

Board Configuration

This chapter describes the location and purpose of board components such as pins, jumpers, connectors, and LEDs.

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4.1 Board Jumpers

Built into the evaluation board is the ability to monitor and test all the capabilities of the PCI2050. There are many jumpers located on the evaluation board (J1 through J9) which allow an engineer to perform tests ranging from measuring power to changing the arbitration of the PCI2050. All of these jumpers are defined in Table 4–1.

Table 4–1. Jumper Definitions

Jumper	Description
J1	This four-pin jumper header is used either to test or to set the signal level of the four general-purpose I/O terminals on the PCI2050.
J2 and J3	Jumpers J2 and J3 are used to control the mode-select inputs to the PCI2050.
J4	This five-pin jumper header is used to access the JTAG interface on the PCI2050.
J5	Arbitration support. By cutting the trace across this jumper and installing R5, an external arbiter can be used.
J6	S_VCCP for the PCI2050. This jumper can be used to measure the power consumed through the S_VCCP.
J7	P_VCCP for the PCI2050. This jumper can be used to measure the power consumed through the P_VCCP.
J8	Core VCC for the PCI2050. This jumper can be used to measure the power consumed by the PCI2050 core logic.
J9	S_VIO select. This jumper is used to select between 3.3-V and 5-V signaling environments on the secondary bus.

4.2 PCI2050 Mode Select Pins

The PCI2050 has three modes of operation based on the value of the mode select pins MS0/MS1. Table 4–2 shows the jumper settings for the different modes of operation.

Table 4–2. Mode Select Jumper Settings

J3	J2	Mode
2–3	2–3	TI hot-swap
2–3	1–2	TI power management
1–2	X	Intel 21150 mode

4.2.1 CompactPCI™ Hot-Swap

When hot-swap mode is selected, the GPIO3 test point can be used to control $\overline{\text{HS\_SWITCH}}$.

4.3 LED Indicators

4.3.1 D1 $\overline{\text{ENUM}}$

When the PCI2050 is configured in CompactPCI mode, this LED indicator lights when the $\overline{\text{ENUM}}$ signal is driven low.

4.3.2 D2 HSLED

When the PCI2050 is configured in CompactPCI mode, this LED indicator lights when the HSLED signal is driven low.

4.3.3 D3 C1_PRES

D3 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P1.

4.3.4 D4 C2_PRES

D4 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P2.

4.3.5 D5 C3_PRES

D5 lights when a PCI board that has the $\overline{\text{PRSNT2}}$ pin tied to ground is inserted in connector P3.

4.3.6 D6 EVM3V

D6 lights to indicate that 3.3 V is available on the secondary bus.

4.3.7 D7 PCU3V

D7 lights to indicate that the PCI2050 has power applied to the core logic.

4.4 Power Measurements

In order to measure the current drawn by the core logic or one of the VIO rails of the PCI2050, it is necessary to isolate the power supplied to these terminals from the rest of the system. This can be done by cutting the traces that connect the power terminals to the system. Jumpers J6, J7, and J8 have default traces that are provided for this purpose. After the traces are cut, an external power supply can be used along with a current meter to measure the current used by the selected power rail. The power rail can then be reconnected to the system by placing a jumper where the trace was cut.

4.5 Undetected Cards

The PCI2050 EVM board uses the $\overline{\text{PRSNT2}}$ terminal to determine if a card is inserted in a socket, and to enable the clock to that socket. If the $\overline{\text{PRSNT2}}$ terminal is not connected to GND before reset is deasserted, then the clock to that socket is disabled and the card will not be configured. The present LEDs C1_PRES, C2_PRES, and C3_PRES indicate whether the $\overline{\text{PRSNT2}}$ terminal on a board is connected to ground. If the present LED for a slot is off, the clock to that socket is not enabled. If a card cannot be seen by the system when it is inserted in the PCI2050 EVM board and the present LED for that socket is on, the user should check the secondary clock control register at PCI offset 68h to determine if the clock to the socket is enabled. A bit set to 0 indicates that the corresponding clock is turned on. Table 4–3 shows the relationship of the bits in the secondary clock control register and the clock to each socket. If the clock is not enabled, a blue wire can be placed on the PCI2050 EVM board from the $\overline{\text{PRSNT2}}$ terminal on the socket to ground, forcing the clock to turn on. $\overline{\text{PRSNT2}}$ is terminal B11 on the PCI socket.

Table 4–3. Socket Clock Control Bits

Socket Number	Secondary Clock Control Register Bits
P1	0, 1
P2	2, 3
P3	4, 5

4.6 Mictor Connector Definition

Connectors MC1 and MC2 can be used to connect a logic analyzer to the secondary PCI bus. See Table 4–4 for a listing of the signals for each logic analyzer POD.

Table 4–4. HP Logic Analyzer POD Definition

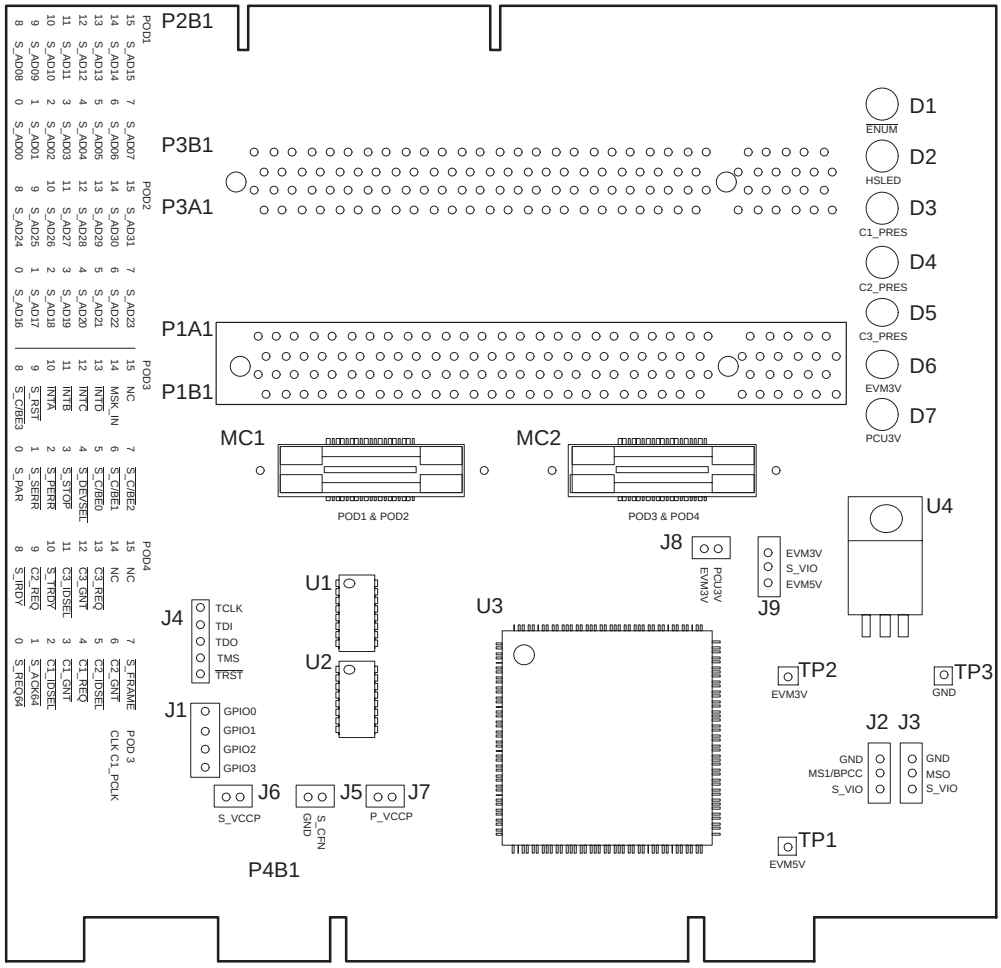
Pin Number	POD 1	POD 2	POD 3	POD 4
0	S_AD0	S_AD16	S_PAR	$\overline{\text{S\_REQ64}}$
1	S_AD1	S_AD17	$\overline{\text{S\_SERR}}$	$\overline{\text{S\_ACK64}}$
2	S_AD2	S_AD18	$\overline{\text{S\_PERR}}$	C1_INDSEL
3	S_AD3	S_AD19	$\overline{\text{S\_STOP}}$	$\overline{\text{C1\_GNT}}$
4	S_AD4	S_AD20	$\overline{\text{S\_DEVSEL}}$	$\overline{\text{C1\_REQ}}$
5	S_AD5	S_AD21	$\overline{\text{S\_C/BE0}}$	C2_IDSEL
6	S_AD6	S_AD22	$\overline{\text{S\_C/BE1}}$	$\overline{\text{C2\_GNT}}$
7	S_AD7	S_AD23	$\overline{\text{S\_C/BE2}}$	$\overline{\text{S\_FRAME}}$
8	S_AD8	S_AD24	$\overline{\text{S\_C/BE3}}$	$\overline{\text{S\_IRDY}}$
9	S_AD9	S_AD25	$\overline{\text{S\_RST}}$	$\overline{\text{C2\_REQ}}$
10	S_AD10	S_AD26	$\overline{\text{INTA}}$	$\overline{\text{S\_TRDY}}$
11	S_AD11	S_AD27	$\overline{\text{INTB}}$	C3_IDSEL
12	S_AD12	S_AD28	$\overline{\text{INTC}}$	$\overline{\text{C3\_GNT}}$
13	S_AD13	S_AD29	$\overline{\text{INTD}}$	$\overline{\text{C3\_REQ}}$
14	S_AD14	S_AD30	NC	NC
15	S_AD15	S_AD31	NC	NC

Note: The secondary bus clock is connected to the POD 3 clock line. This clock must be enabled in the clock control register.

4.7 Board Description

The board layout is shown in Figure 4–1. The schematic diagram of the board is in Figure 4–2. Table 4–5, Bill of Materials, is a list of the parts used to assemble the board.

Figure 4–1. Part and Jumper Locations



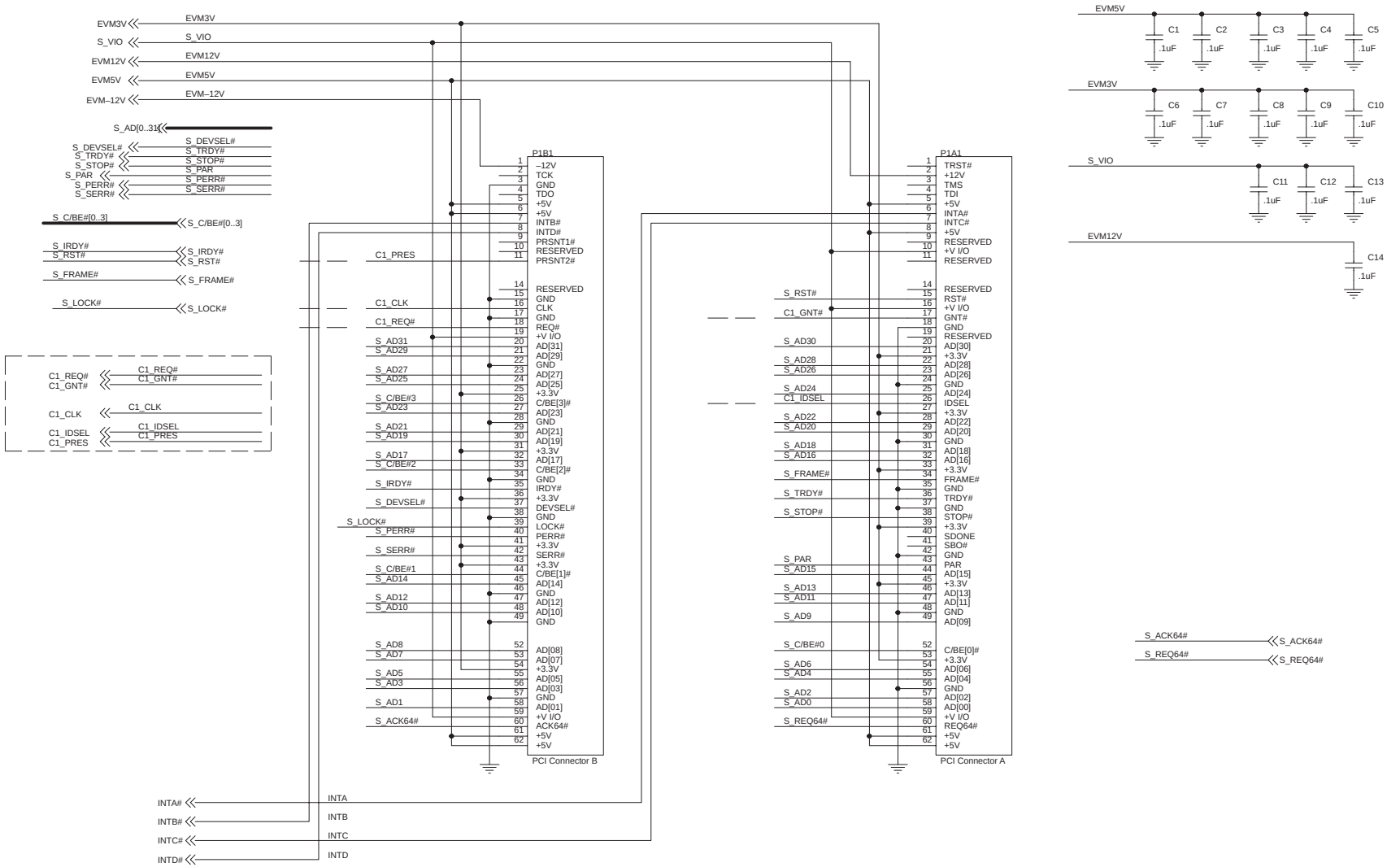


Figure 4–2. Schematic Diagram (Sheet 1 of 8)

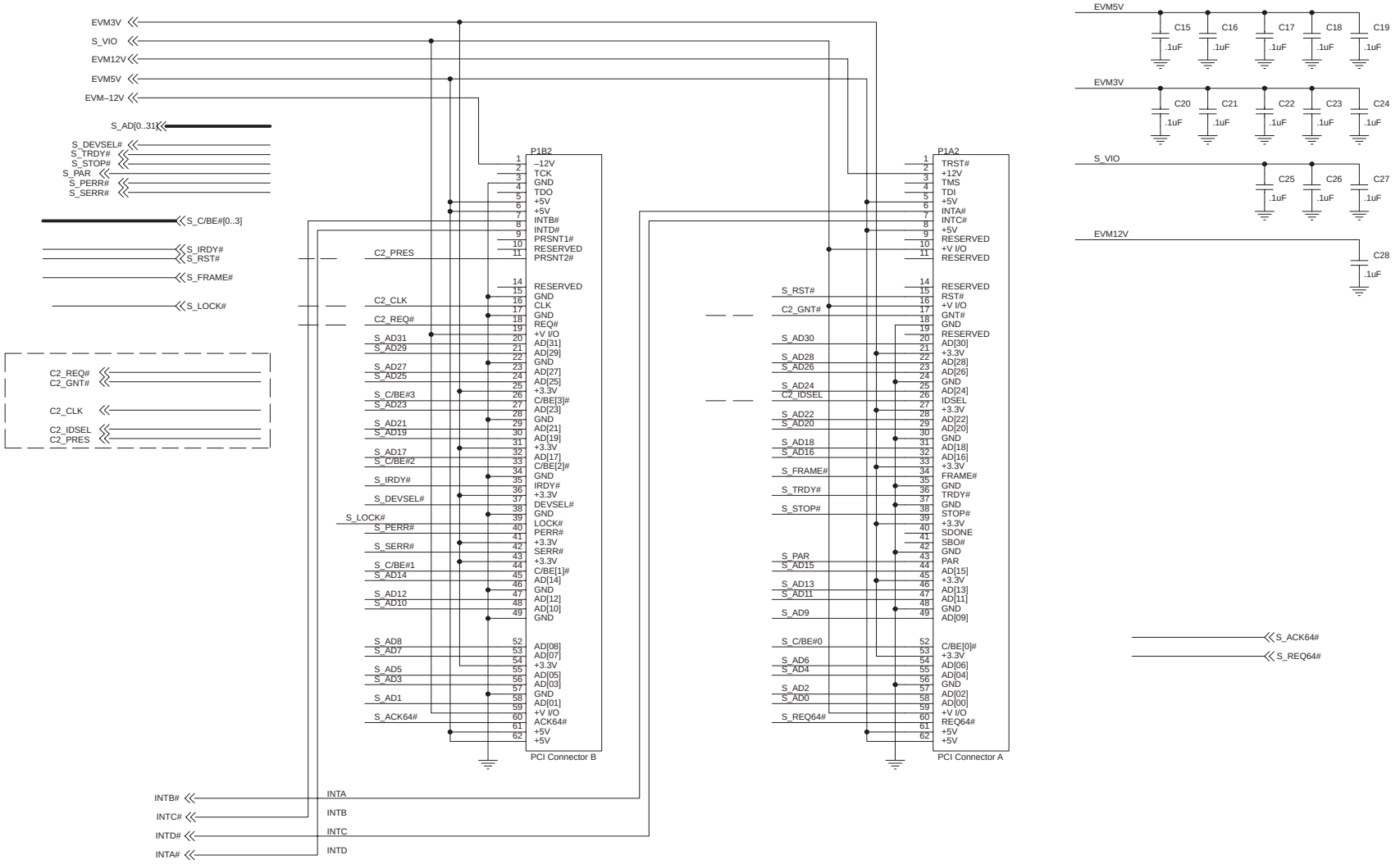


Figure 4–2. Schematic Diagram (Sheet 2 of 8)

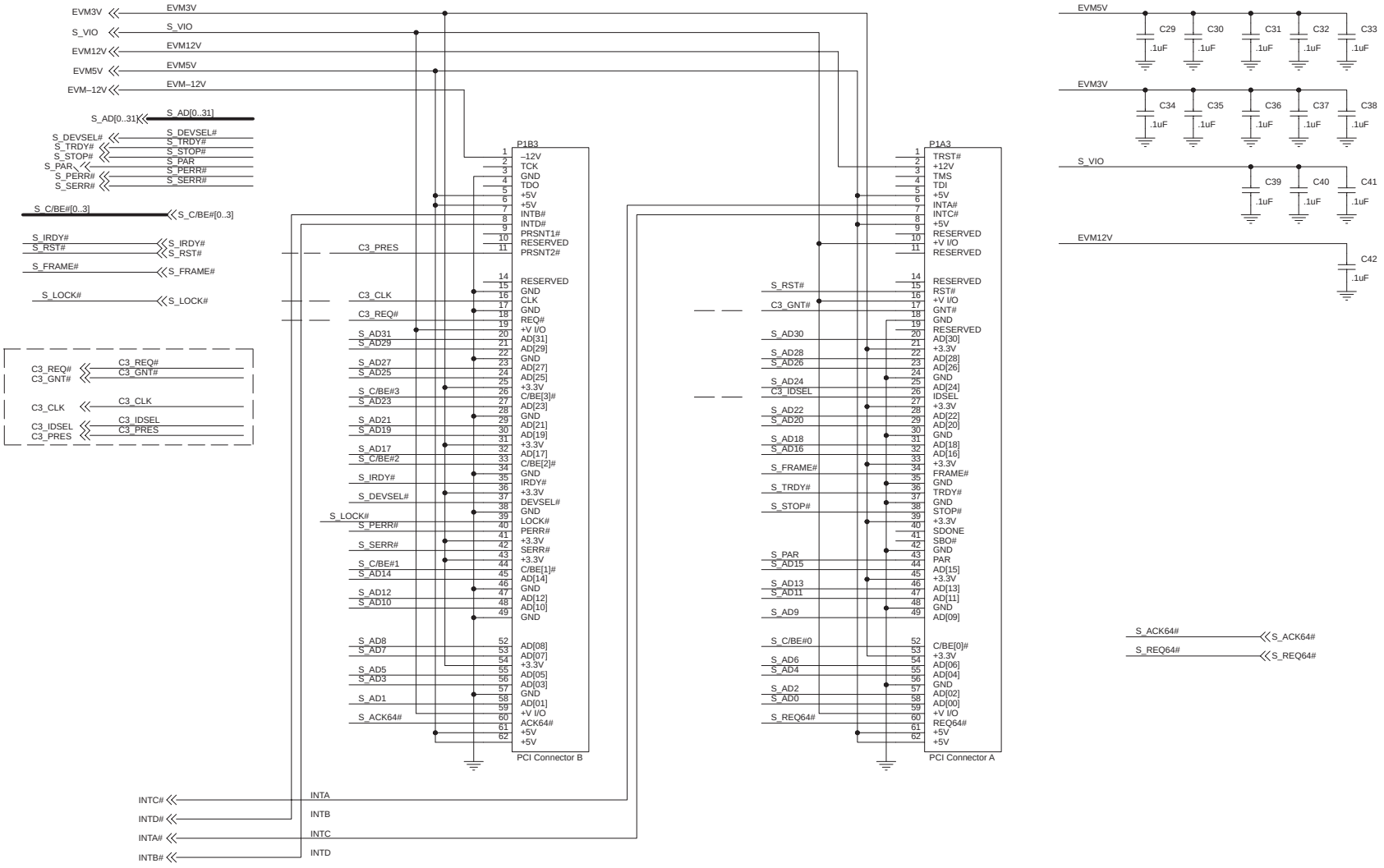


Figure 4–2. Schematic Diagram (Sheet 3 of 8)

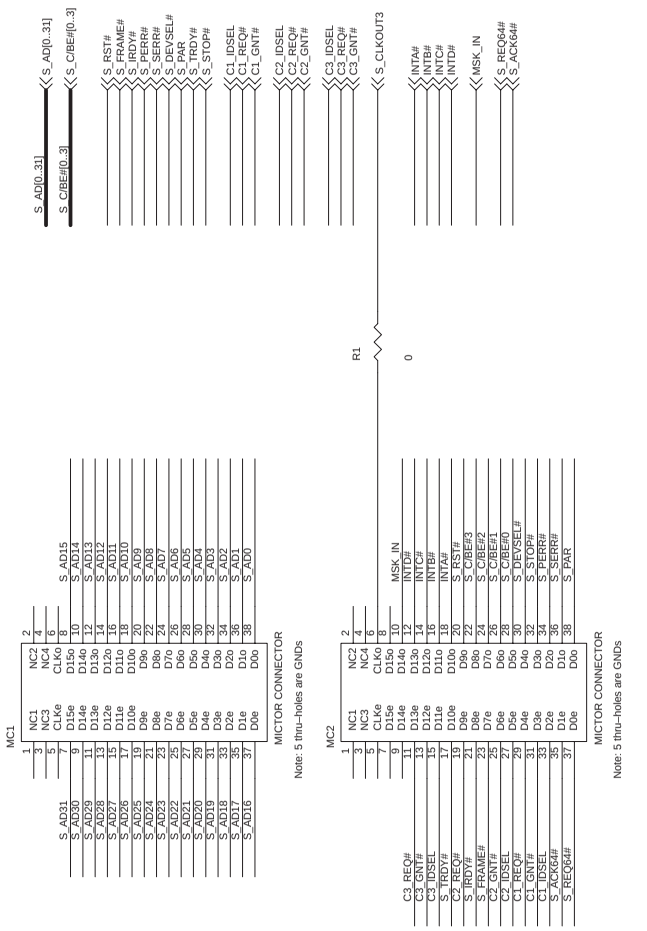


Figure 4–2. Schematic Diagram (Sheet 4 of 8)

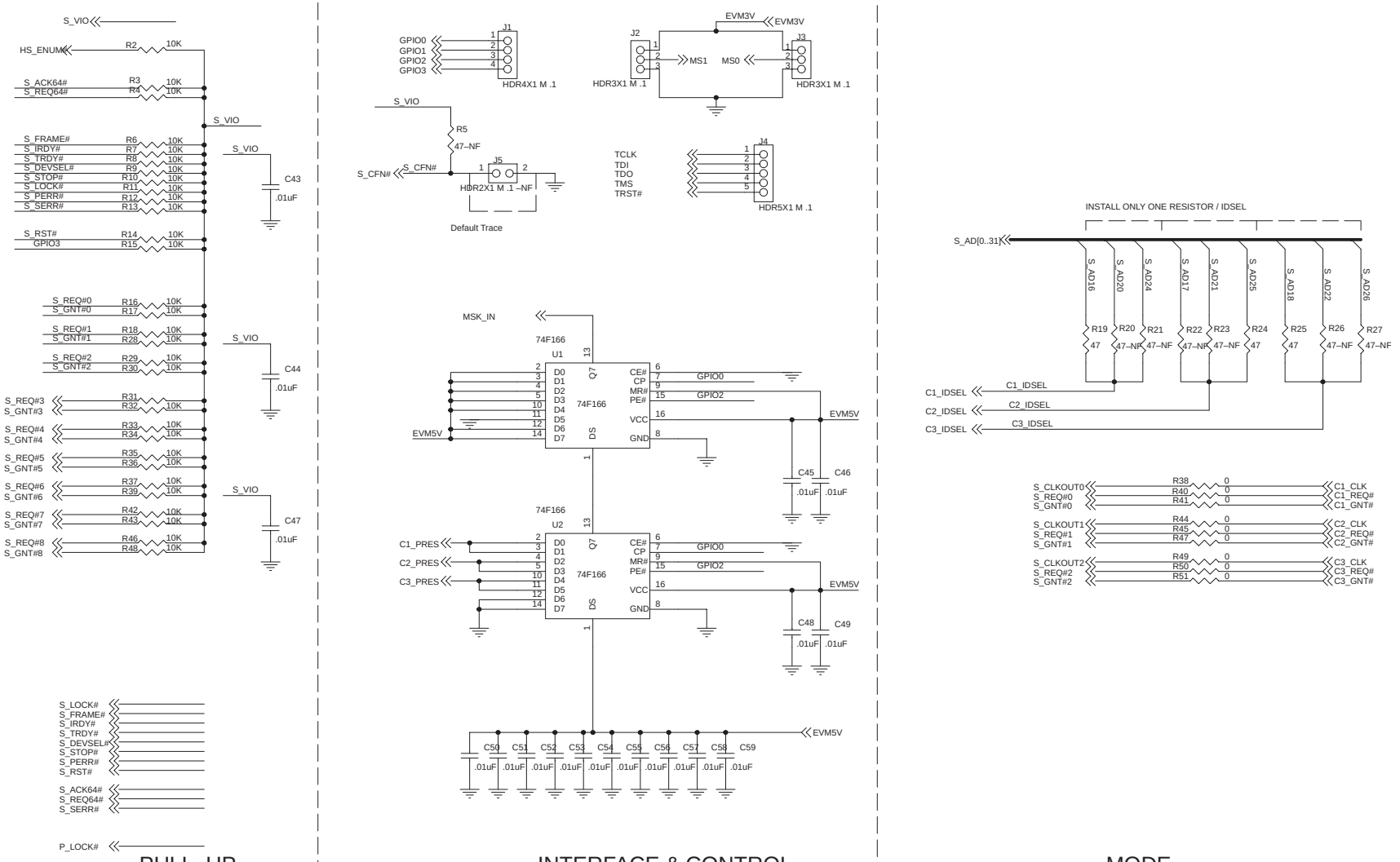


Figure 4–2. Schematic Diagram (Sheet 5 of 8)

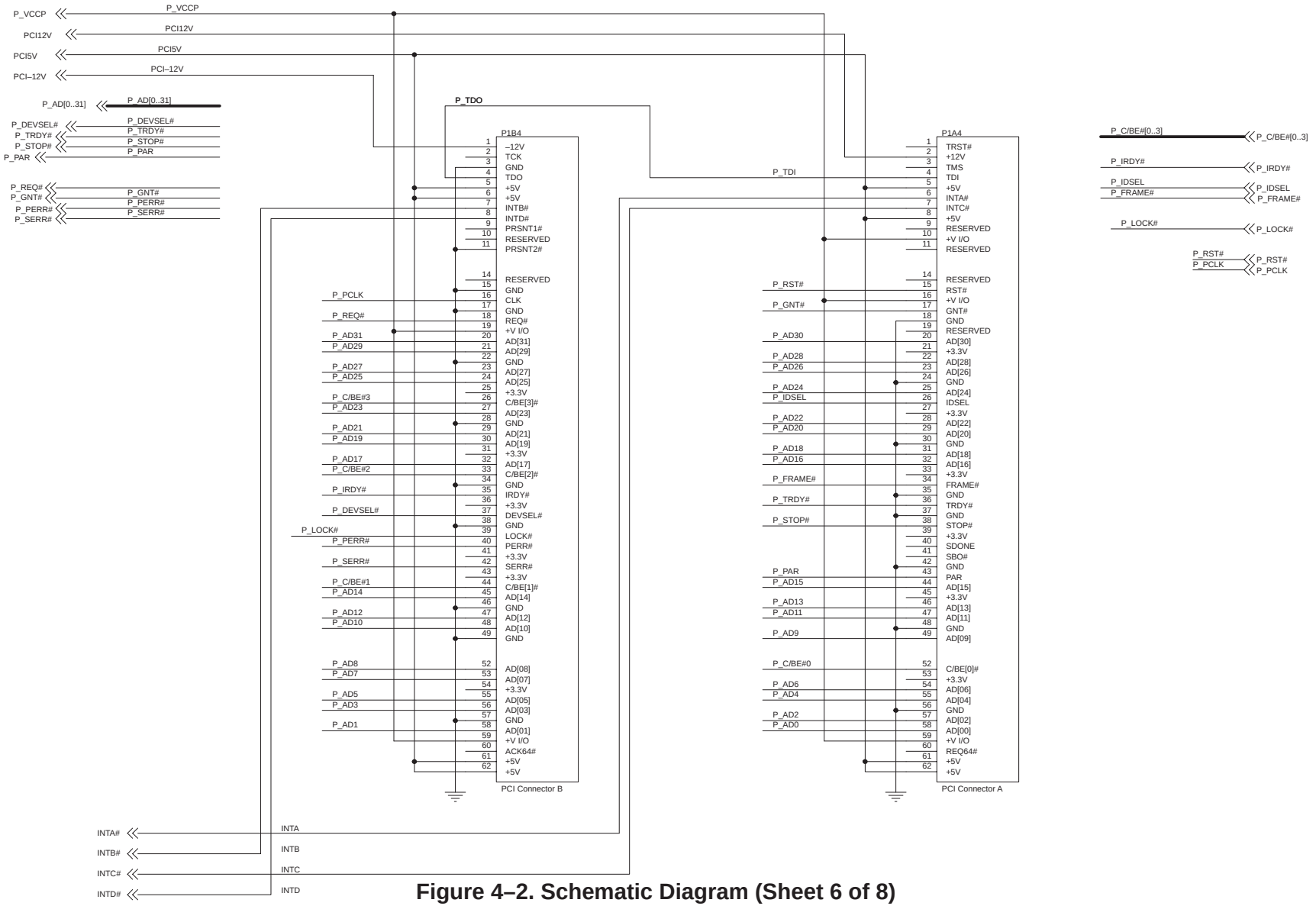


Figure 4–2. Schematic Diagram (Sheet 6 of 8)

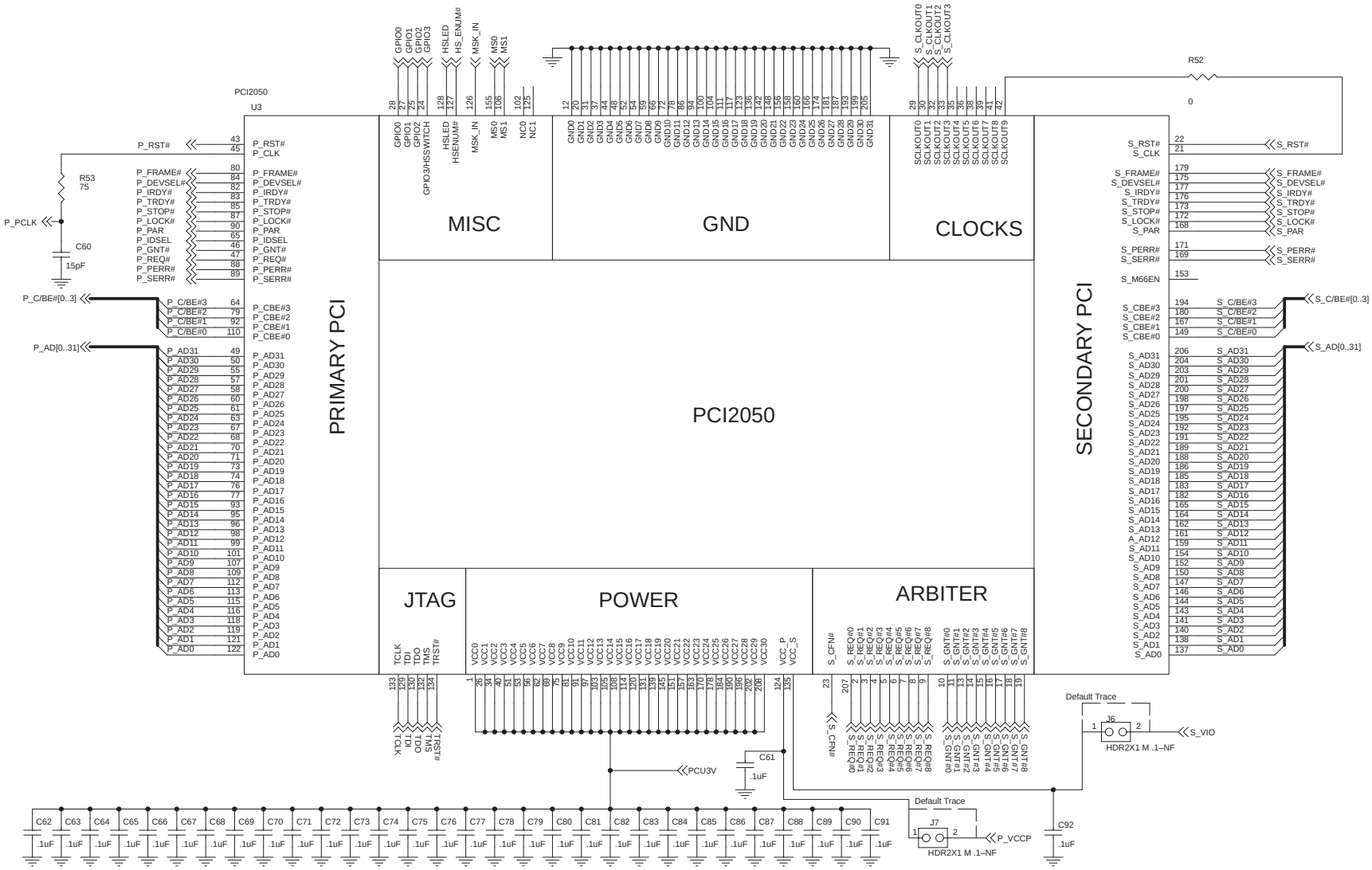


Figure 4–2. Schematic Diagram (Sheet 7 of 8)

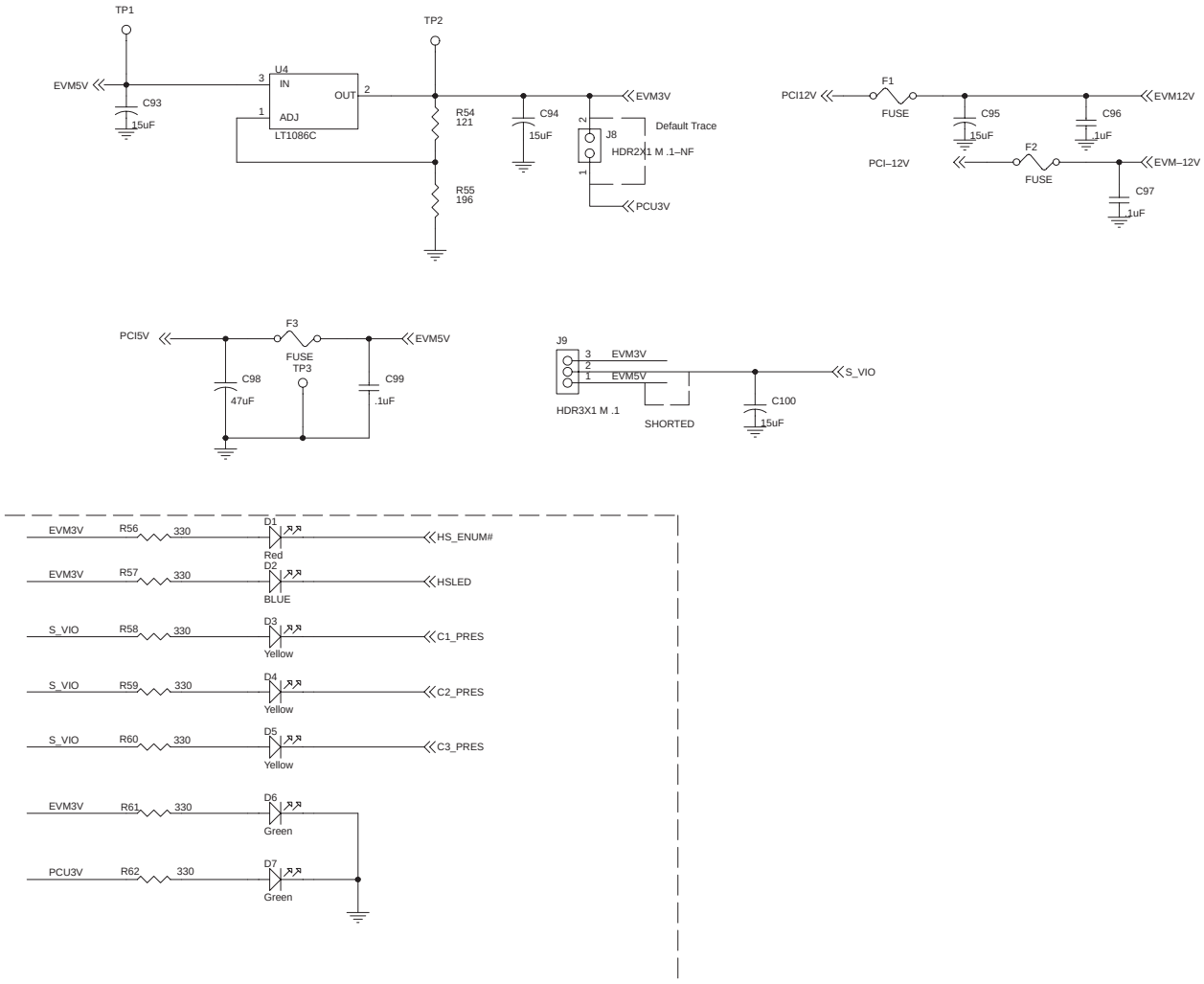


Figure 4–2. Schematic Diagram (Sheet 8 of 8)

Table 4–5. PCI2050 EVM Bill of Materials

Item	Qty	Reference	Part	Pkg	MFG	Part No.
1	77	C1–C42, C61–C92, C96, C97, C99	0.1 μF	805	Phillips	08052R104K9BB0
2	17	C43–C59	0.01 μF	805	MMC	CE103K2NR
3	1	C60	15 pF	805	MMC	CE150J2NO
4	4	C93,C94, C95, C100	15 μF	6032	NIC	NTC-T156K20TRC
5	1	C98	47 μF	6032	NIC	NTC-T476K6.3TRC
6	1	D1	Red	See Diagram	Lumex	
7	1	D2	Red	See Diagram	Lumex	
8	3	D3, D4, D5	Yellow	See Diagram	Lumex	
9	2	D6,D7	Green	See Diagram	Lumex	
10	3	F1, F2, F3	FUSE	TH	LittleFuse	251.75
11	1	J1	HDR4X1 M 0.1 nF		AMP	103321-4
12	3	J2,J3,J9	HDR3X1 M 0.1 nF		AMP	103321-3
13	4	J5–J8	HDR2X1 M 0.1 nF		AMP	103321-2
14	1	J4	HDR5X1 M 0.1 nF		AMP	103321-5
15	2	MC2, MC1	Mictor Connector		AMP	2-767004-2
16	2	P1A1/P1B1, P1A3/P1B3	PCI Connector	N/A	AMP	145154-8
17	1	P1A2/P1B2	PCI Connector	N/A	Capstone	CEE2X60SMV-3Z14W
18	31	R2–R4, R6–R18, R28–R37, R39, R41, R42, R45, R47	10K	805	KOA	RM73B2A103J
19	7	R5, R19, R21, R22, R23, R26, R27	47 nF	805	KOA	RM73B2A470J
20	10	R1, R38, R40, R43, R44, R46, R48, R49, R50, R51	0	805	KOA	RM73Z2A000
21	3	R20, R24, R25	47	805	KOA	RM73B2A470J
22	1	R52	75	805	KOA	RM73B2A750J
23	1	R53	121	TH	NIC	NMR25F1210B
24	1	R54	196	TH	NIC	NMR25F1960B
25	7	R55–R61	330	805	KOA	RM73B2A331J
26	3	TP1, TP2, TP3	TEST POINT		AMP	

Table 4–5. PCI2050 EVM Bill of Materials (Continued)

Item	Qty	Reference	Part	Pkg	MFG	Part No.
27	2	U1, U2	74F166	See Drawing	Philips Semiconductor	74F166
28	1	U3	PCI2050	See Drawing	Texas Instruments	PCI2050
29	1	U4	LT1086C	TO-220	DigiKey	LT1086C