TEXAS INSTRUMENTS

PCI2250

PCI-to-PCI Bridge

Implementation Guide

2000

MSDS PCI

SCPU008

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1 Introduction

This document is provided to assist platform developers who are using the PCI2250 PCI-to-PCI bridge controller.

Chapter 2 is a list of the features of the PCI2250.

Chapter 3 is a listing of the device terminals, with the corresponding signal names for each terminal.

Chapter 4 is the electrical guidelines. This section explains pullup resistors and voltage level capacitors required for proper implementation of the PCI2250. The PCI specification requires all signals to be driven to a known level. This is accomplished with pullup resistors or by the PCI device. Some small capacitors are recommended on the power connections of the PCI2250. This is standard practice in board design to provide a stable supply voltage when large loads are placed on the system.

Chapter 5 describes a number of functional considerations in implementing a PCI2050 solution, including proper use of an external arbiter with the PCI2250, how PCI interrupts and IDSEL mappings interrelate, how to implement clock run, lock, and cPCI hot-swap with the PCI2250, and implementing PCI power management.

2 PCI2250 Feature Set

The PCI2250 provides the following features.

- Supports *PCI Local Bus Specification Revision 2.2* and *PCI-PCI Bridge Specification 1.1*
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Supports two 32-bit, 33-MHz PCI buses
- Provides internal arbitration for up to four external secondary bus masters with programmable control
- Provides five secondary PCI bus clock outputs
- Supports sustained pass-through bandwidth of 132 MBps
- Packaged in high technology 176-terminal TQFP or 160-terminal PQFP
- Supports for PCI clock run on both buses
- External arbiter option
- Support for bus locking
- Support for CompactPCI™ hot-swap
- Independent read and write buffers for each direction
- Secondary positive, negative, and subtractive decode
- Two extension windows
- Provides VGA/palette, memory, I/O, and subtractive decoding options

3 Terminal Assignments

Table 3–1. 176-Terminal LQFP Signal Names Sorted by Terminal Number

NO.	SIGNAL NAME	NO.	SIGNAL NAME	NO.	SIGNAL NAME	NO.	SIGNAL NAME
1	GND	45	GND	89	GND	133	GND
2	NC	46	NC	90	NC	134	NC
3	S_PAR	47	S_REQ3	91	P_C/BE3	135	P_C/BE0
4	NC	48	NC	92	NC	136	NC
5	S_SERR	49	S_GNT0	93	P_IDSEL	137	P_AD7
6	S_PERR	50	S_GNT1	94	P_AD23	138	P_AD6
7	S_MFUNC	51	S_GNT2	95	P_AD22	139	VCC
8	S_STOP	52	VCC	96	GND	140	P_AD5
9	S_DEVSEL	53	S_GNT3	97	P_AD21	141	P_AD4
10	VCC	54	S_RST	98	P_AD20	142	GND
11	S_TRDY	55	S_CFN	99	P_AD19	143	P_AD3
12	S_IRDY	56	GND	100	VCC	144	P_AD2
13	S_FRAME	57	S_CLK	101	P_AD18	145	VCC
14	GND	58	S_VCCP	102	P_AD17	146	P_AD1
15	S_C/BE2	59	S_CLKOUT0	103	P_AD16	147	P_AD0
16	S_AD16	60	GND	104	GND	148	S_AD0
17	VCC	61	S_CLKOUT1	105	P_C/BE2	149	GND
18	S_AD17	62	VCC	106	P_FRAME	150	S_AD1
19	S_AD18	63	S_CLKOUT2	107	P_IRDY	151	S_AD2
20	S_AD19	64	GND	108	VCC	152	S_AD3
21	GND	65	S_CLKOUT3	109	P_TRDY	153	VCC
22	S_AD20	66	VCC	110	P_DEVSEL	154	S_AD4
23	S_AD21	67	S_CLKOUT4	111	P_STOP	155	S_AD5
24	S_AD22	68	NO/HSLED	112	P_MFUNC	156	S_AD6
25	VCC	69	GOZ	113	GND	157	GND
26	S_AD23	70	P_RST	114	P_PERR	158	S_AD7
27	S_C/BE3	71	GND	115	P_SERR	159	S_C/BE0
28	S_AD24	72	P_CLK	116	P_PAR	160	S_AD8
29	GND	73	P_VCCP	117	P_C/BE1	161	VCC
30	S_AD25	74	P_GNT	118	VCC	162	S_AD9
31	S_AD26	75	P_REQ	119	P_AD15	163	S_AD10
32	VCC	76	P_AD32	120	P_AD14	164	S_AD11
33	S_AD27	77	GND	121	P_AD13	165	GND
34	S_AD28	78	P_AD30	122	GND	166	S_AD12
35	S_AD29	79	P_AD29	123	P_AD12	167	S_AD13
36	GND	80	P_AD28	124	P_AD11	168	VCC
37	S_AD30	81	VCC	125	P_AD10	169	S_AD14
38	S_AD31	82	P_AD27	126	VCC	170	S_AD15
39	S_REQ0	83	P_AD26	127	P_AD9	171	GND
40	S_REQ1	84	P_AD25	128	P_AD8	172	S_C/BE1
41	NC	85	NC	129	NC	173	NC
42	S_REQ2	86	P_AD24	130	GND	174	MS1/BPCC
43	NC	87	NC	131	NC	175	NC
44	VCC	88	VCC	132	MSO	176	VCC

Table 3–2. 160-Terminal PQFP Signal Names Sorted by Terminal Number

NO.	SIGNAL NAME	NO.	SIGNAL NAME	NO.	SIGNAL NAME	NO.	SIGNAL NAME
1	GND	41	GND	81	GND	121	GND
2	S_PAR	42	S_REQ3	82	P_C/BE3	122	P_C/BE0
3	S_SERR	43	S_GNT0	83	P_IDSEL	123	P_AD7
4	S_PERR	44	S_GNT1	84	P_AD23	124	P_AD6
5	S_MFUNC	45	S_GNT2	85	P_AD22	125	VCC
6	S_STOP	46	VCC	86	GND	126	P_AD5
7	S_DEVSEL	47	S_GNT3	87	P_AD21	127	P_AD4
8	VCC	48	S_RST	88	P_AD20	128	GND
9	S_TRDY	49	S_CFN	89	P_AD19	129	P_AD3
10	S_IRDY	50	GND	90	VCC	130	P_AD2
11	S_FRAME	51	S_CLK	91	P_AD18	131	VCC
12	GND	52	S_VCCP	92	P_AD17	132	P_AD1
13	S_C/BE2	53	S_CLKOUT0	93	P_AD16	133	P_AD0
14	S_AD16	54	GND	94	GND	134	S_AD0
15	VCC	55	S_CLKOUT1	95	P_C/BE2	135	GND
16	S_AD17	56	VCC	96	P_FRAME	136	S_AD1
17	S_AD18	57	S_CLKOUT2	97	P_IRDY	137	S_AD2
18	S_AD19	58	GND	98	VCC	138	S_AD3
19	GND	59	S_CLKOUT3	99	P_TRDY	139	VCC
20	S_AD20	60	VCC	100	P_DEVSEL	140	S_AD4
21	S_AD21	61	S_CLKOUT4	101	P_STOP	141	S_AD5
22	S_AD22	62	NO/HSLED	102	P_MFUNC	142	S_AD6
23	VCC	63	GOZ	103	GND	143	GND
24	S_AD23	64	P_RST	104	P_PERR	144	S_AD7
25	S_C/BE3	65	GND	105	P_SERR	145	S_C/BE0
26	S_AD24	66	P_CLK	106	P_PAR	146	S_AD8
27	GND	67	P_VCCP	107	P_C/BE1	147	VCC
28	S_AD25	68	P_GNT	108	VCC	148	S_AD9
29	S_AD26	69	P_REQ	109	P_AD15	149	S_AD10
30	VCC	70	P_AD32	110	P_AD14	150	S_AD11
31	S_AD27	71	GND	111	P_AD13	151	GND
32	S_AD28	72	P_AD30	112	GND	152	S_AD12
33	S_AD29	73	P_AD29	113	P_AD12	153	S_AD13
34	GND	74	P_AD28	114	P_AD11	154	VCC
35	S_AD30	75	VCC	115	P_AD10	155	S_AD14
36	S_AD31	76	P_AD27	116	VCC	156	S_AD15
37	S_REQ0	77	P_AD26	117	P_AD9	157	GND
38	S_REQ1	78	P_AD25	118	P_AD8	158	S_C/BE1
39	S_REQ2	79	P_AD24	119	GND	159	MS1/BPCC
40	VCC	80	VCC	120	MSO	160	VCC

4 Electrical Guidelines

4.1 Pullup Resistors

This discussion on PCI pullup requirements is taken from the *PCI Local Bus Specification Rev 2.2*, and is provided for reference in designing in the PCI2250.

PCI control signals always require pullup resistors on the motherboard (NOT the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{STOP}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{INTD}}$, $\overline{\text{INTC}}$, $\overline{\text{INTB}}$, $\overline{\text{INTA}}$, and when used, $\overline{\text{REQ64}}$, and $\overline{\text{ACK64}}$. The point-to-point and shared 32-bit signals do not require pullups; bus parking ensures their stability.

Table 4–1. Minimum and Typical PCI Pullup Resistor Values

SIGNALING RAIL	R_{MIN}	$R_{TYPICAL}$	R_{MAX}
5.0 V	963 W	2.7 kΩ at 10%	Dependent on number of loads. See equation 1.
3.3 V	2.42 kW	8.2 kΩ at 10%	Dependent on number of loads. See equation 1.

Equation to calculate R_{MAX}:

$$R_{MAX} = \left[V_{CC(MIN)} - V_X\right] \Big/ \left[\text{num\_loads} \times I_{IH}\right] \quad (1)$$

Where:

V_X = 2.7 V for 5.0-V signaling and V_X = 2.3 V for 3.3-V signaling.

In addition to those specified by PCI, the table below contains both PCI control signals and other PCI2250 specific signals which should have pullup (keeper) resistors. Texas Instruments also recommends, when possible, that the signals be pulled up to 3.3 V to reduce leakage current.

Table 4–2. PCI2250 Pullups

160 PQFP TERMINAL NO.	176 LQFP TERMINAL NO.	TERMINAL NAME	160 PQFP TERMINAL NO.	176 LQFP TERMINAL NO.	TERMINAL NAME
7	9	$\overline{\text{S\_DEVSEL}}$	39	42	$\overline{\text{S\_REQ2}}$
11	13	$\overline{\text{S\_FRAME}}$	42	47	$\overline{\text{S\_REQ3}}$
10	12	$\overline{\text{S\_IRDY}}$	48	54	$\overline{\text{S\_RST}}$
4	6	$\overline{\text{S\_PERR}}$	3	5	$\overline{\text{S\_SERR}}$
37	39	$\overline{\text{S\_REQ0}}$	6	8	$\overline{\text{S\_STOP}}$
38	40	$\overline{\text{S\_REQ1}}$	9	11	$\overline{\text{S\_TRDY}}$

The signals in Table 4–3 may need pullups. The designer should refer to the section related to the signal to determine if a pullup resistor is necessary.

Table 4–3. Optional Pullups

160 PQFP TERMINAL NO.	176 LQFP TERMINAL NO.	TERMINAL NAME	REFER TO SECTION ON
63	69	$\overline{\text{GOZ}}$	N/A
102	112	P_MFUNC	Multifunction terminals
49	55	$\overline{\text{S\_CFN}}$	External arbiter
5	7	S_MFUNC	Multifunction terminals

The signals listed in Table 4–4 can be hardwired to GND or 3.3 V, if they are not going to be used in the design. Texas Instruments strongly recommends that all active-low signals listed in Table 4–4, be hardwired to 3.3 V. All other signals can be hardwired to GND or 3.3 V.

Table 4–4. Signals Which Could Be Hardwired to GND or 3.3 V

160 PQFP TERMINAL NO.	176 LQFP TERMINAL NO.	TERMINAL NAME	160 PQFP TERMINAL NO.	176 LQFP TERMINAL NO.	TERMINAL NAME
63	69	$\overline{GOZ}$	39	42	$\overline{S\_REQ2}$
37	39	$\overline{S\_REQ0}$	42	47	$\overline{S\_REQ3}$
38	40	$\overline{S\_REQ1}$			

4.2 Power and Signal Levels

The PCI2250 supports both 3.3-V and 5.0-V signaling environments. This is accomplished by the P_VCCP and S_VCCP clamping rails. These two rails are not power rails. They only clamp the signals at the rail voltage (3.3 V or 5 V). All I/O buffers are powered by the V_{CC} rail. Because V_{CC} powers both the core and the I/O buffers, it must always be at 3.3 V. The table below depicts the signaling combinations supported by the PCI2250 and the P_VCCP and S_VCCP voltages needed to operate in these signaling environments.

Table 4–5. V_{CC} Combinations Based on Signaling Environment

PRIMARY BUS SIGNALING ENVIRONMENT [V]	SECONDARY BUS SIGNALING ENVIRONMENT [V]	P_VCCP [V]	S_VCC [V]	VCC [V]
5	5	5	5	3.3
5	3.3	5	3.3	3.3
3.3	5	3.3	5	3.3
3.3	3.3	3.3	3.3	3.3

Table 4–6 contains the power measurements for the PCI2250. The measurements were taken under the following conditions: 33-MHz PCI bus clock, V_{CC} = 3.3 V, P_VCCP = 5.0 V, and S_VCCP = 5.0 V.

Table 4–6. PCI2250 Power Measurements

DEVICE STATE	I_{VCC} (mA)	I_{P_VCCP} (μA)	I_{S_VCCP} (μA)
D0	55	500	500
D1	50	500	500
D2	15	500	$\overline{500}$
$D3_{Hot}$	15	500	500

4.3 Bypass Capacitors

Standard design rules for the supply bypass should be followed. Low-inductance ceramic-chip capacitors are best for bypass capacitors. A value of 0.1 μF is recommended for each of the power supply terminals V_{CC}, P_VCCP, and S_VCCP.

4.4 Secondary Clocks

The PCI2250 has five secondary clocks based on the primary PCI clock. Each secondary clock can be enabled or disabled through the secondary clock control register located at PCI offset 68h. We suggest the configuration software or BIOS disable any clocks which are not in use to conserve power. When a secondary clock is disabled, the PCI2250 will drive the clock signal low until the clock is reenabled. Texas Instruments also recommends the use of a 50-Ω series terminator resistor to be connected to each secondary clock to reduce reflections.

The primary clock and the secondary clocks have the following relationships:

- They both operate at the same frequency.
- The maximum clock frequency is 33 MHz.

- The skew between P_CLK and S_CLKOUT[0:4] has a range of 2.72 ns at 0°C to 5.8 ns at 115°C.
- The skew between secondary clocks is less than 0.1 ns with similar loading.

To ensure that the skew between the S_CLK input and the clock inputs to the secondary devices is minimized, the trace length between S_CLKOUT4 and S_CLK should match the trace length of the other S_CLKOUT traces. If one or more of the S_CLKOUT terminals is being routed to a socket, then the clock trace lengths to the built-on devices should be 2.5 inches longer than the clock traces to the sockets.

5 Functional Considerations

5.1 External Arbiter

The PCI2250 allows an external arbiter to be used in place of the default internal arbiter. This function is controlled by terminal 63 ($\overline{GOZ}$). In order to use an external arbiter with the PCI2250, terminal 63 must be pulled up with a 10-kΩ resistor or hardwired to 3.3 V. If an external arbiter is not going to be used (the PCI2250 internal arbiter will be used instead), then terminal 63 must be hardwired to GND.

When an external secondary bus arbiter is used, the PCI2250 internally reconfigures the $\overline{S\_REQ0}$ and $\overline{S\_GNT0}$ signals, so that $\overline{S\_REQ0}$ becomes the secondary bus master grant for the bridge and the $\overline{S\_GNT0}$ becomes the secondary bus master request for the PCI2250. This is done because $\overline{S\_REQ0}$ is an input and can be used to provide the grant input to the bridge and $\overline{S\_GNT0}$ is an output and can provide the request output from the bridge.

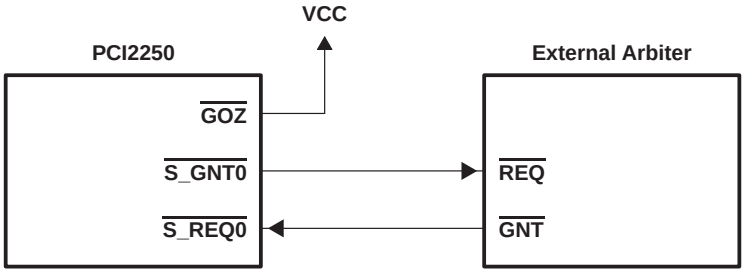

Figure 5–1. External Arbiter

When an external arbiter is used, all unused secondary bus grant outputs ($\overline{S\_GNT3}$–$\overline{S\_GNT1}$) are in a high-impedance state. Any unused secondary bus request lines ($\overline{S\_REQ3}$–$\overline{S\_REQ1}$) should be pulled high or hardwired to 3.3 V, to prevent the inputs from oscillating.

5.2 PCI Interrupts and IDSEL Mapping

The PCI2250 can support up to four devices on the secondary side. Each device IDSEL should be connected to a secondary address line (S_AD[31:16]). In order to reduce capacitive load on the secondary address line, the connection can be made through a 1-kΩ series resistor.

Because the PCI2250 is a bridge device, all parallel PCI interrupts on the secondary interface must be routed as sideband signals to the PCI interrupts on the primary interface. When using multiple devices behind the PCI2250, a device ID and how the PCI interrupts are routed should be very important considerations in a design. Some operating systems like Windows 95™ expect a device PCI interrupt to be routed to a specific interrupt on the motherboard based on its ID number. For example, if a device ID is 4 and its PCI $\overline{INTA}$ is routed to PCI $\overline{INTB}$ on the motherboard, Windows 95™ will not configure the device properly. In order to reduce any chance of incompatibilities, we suggest the designer implement the interrupt routing scheme outlined in section 2.2.6 of the *PCI Local Bus Specification Revision 2.2*. Table 6–1 summarizes section 2.2.6.

Windows 95 is a trademark of Microsoft Corporation.

Table 5–1. Interrupt Routing

DEVICE NUMBER ON SECONDARY BUS	INTERRUPT TERMINAL ON DEVICE	INTERRUPT TERMINAL ON CONNECTOR
0, 4, 8, 16, 20, 24, 28	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$
1, 5, 9, 13, 17, 21, 25, 29	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$
2, 6, 10, 14, 18, 22, 26, 30	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$
3, 7, 11, 15, 19, 23, 27, 31	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$

5.3 Multifunction Terminals

The PCI2250 has two multifunction terminals that can be used in three different modes of operation. The modes are Intel™ 21152 compatible mode, TI clock run mode, and TI cPCI hot-swap mode. The mode of operation is controlled by the mode select terminals MS0 and MS1 as shown in the Table 7–1.

Table 5–2. Multifunction Terminal Definition Based on Mode Select Terminals

MS0	MS1	P_MFUNC	S_MFUNC	MODE
0	0	$\overline{\text{HS\_ENUM}}$	$\overline{\text{HS\_SWITCH}}$	TI hot-swap
0	1	$\overline{\text{P\_CLKRUN}}$	$\overline{\text{S\_CLKRUN}}$	TI clock run
1	BPCC	$\overline{\text{P\_LOCK}}$	$\overline{\text{S\_LOCK}}$	Intel

5.3.1 CompactPCI Hot-Swap Mode

In cPCI hot-swap mode, the PCI2250 uses P_MFUNC to signal $\overline{\text{ENUM}}$, S_MFUNC as the input for the switch, and the NAND out pin as the output for the blue LED.

5.3.2 Clock Run Mode

The PCI2250 supports the PCI clock run protocol as defined in the *PCI Mobile Design Guide, Revision 1.0*.

Clock run functionality is implemented in the PCI2250 to reduce power during periods of inactivity. Clock run is typically implemented in mobile computers, but can also be used in desktop systems if there is additional hardware support (chipset, PAL, etc.).

In order to use the PCI2250 clock run functionality, a couple of things must be done in hardware. First, MS0 should be tied to GND and MS1 should be tied to 3.3 V. Second, a 10-kΩ pullup resistor should be connected to the secondary clock run signal (terminal 5). Third, determine if a pullup resistor is needed on the primary clock run signal (terminal 102). Typically, a pullup resistor is already installed on the motherboard. If one is not already installed, Texas Instruments recommends using a 10-kΩ pullup resistor on the primary clock run signal.

Next, the operating system must determine how to initialize the PCI2250 to stop the primary clock and secondary clocks. All clock run initializing is done through the clock run control register at PCI configuration offset 5Bh.

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The operating system should do the following to initialize the PCI2250 for clock run support.

- Set bits 3 and 1 to enable primary and secondary clock run. If the designer is only going to support clock run on the secondary interface and not on the primary interface, only set bit 1 to enable secondary clock run.
- Determine the clock run mode in bit 4. PCI2250 supports two modes for clock run. One is to stop the secondary clock only on request from the primary bus which is the default operation. The second is to stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus.
- Determine if the PCI2250 wants to keep the primary bus running if the secondary bus is stopped. This is set in bit 2.

NOTE:

If clock run is not going to be supported on the primary bus, the primary clock run signal must be hardwired to GND. Failure to do so will result in the bridge functioning unpredictably.

5.3.3 Intel 21152 Compatible Mode

In Intel 21152 compatible mode P_MFUNC and S_MFUNC are used as the PCI $\overline{\text{LOCK}}$ signals. When supporting $\overline{\text{LOCK}}$, P_MFUNC and S_MFUNC should be pulled up.

5.4 Clock Run Mode

When using the PCI2250 in a power managed environment, it is important to remember that $\overline{\text{PME}}$ and 3.3 Vaux are sideband signals as far as the bridge is concerned. If any devices on the secondary bus need $\overline{\text{PME}}$ or 3.3 Vaux, these signals must be routed around the bridge.

5.5 Sample Schematics

For sample schematics see the *PCI2250 Evaluation Module Users Guide*, TI Literature Number – SCPU005.