

# SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

SDAS032A – DECEMBER 1983 – REVISED MARCH 1985

- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - B to A
  - Register to A and/or B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B input Data
  - Serial Transmission of Data from Either A or B Port
  - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

## description

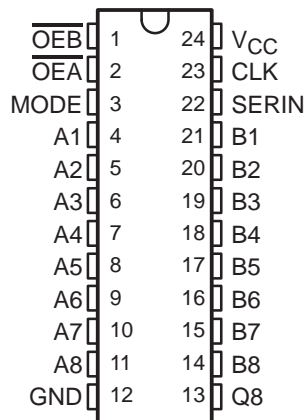
The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines  $\overline{OEA}$ ,  $\overline{OEB}$ , and  $\overline{MODE}$ . These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state).

Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS856 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

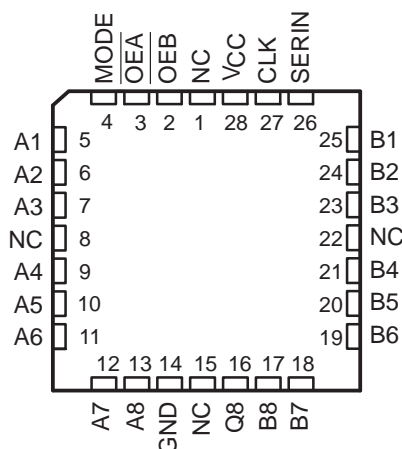
SN54AS856 . . . JT PACKAGE  
SN74AS856 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS856 . . . FK PACKAGE  
SN74AS856 . . . FN PACKAGE

(TOP VIEW)



NC – No internal connection

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FUNCTION TABLE

MODE MODE $\overline{OE}A$ $\overline{OE}B$			CLOCK	SERIN	A1   Q1   B1	A2   Q2   B2	A3   Q3   B3	A4   Q4   B4	A5   Q5   B5	A6   Q6   B6	A7   Q7   B7	A8   Q8   B8	FUNCTION
L	L	L	H or L	X	Q1   Q1   H	Q2   Q2   Q2	Q3   Q3   Q3	Q4   Q4   Q4	Q5   Q5   Q5	Q6   Q6   Q6	Q7   Q7   Q7	Q8   Q8   Q8	Feedback
L	L	L	↑	X	Q1   Q1   H	Q2   Q2   Q2	Q3   Q3   Q3	Q4   Q4   Q4	Q5   Q5   Q5	Q6   Q6   Q6	Q7   Q7   Q7	Q8   Q8   Q8	
L	L	H	H or L	X	B1   Q1   H	B2   Q2   Z	B3   Q3   Z	B4   Q4   Z	B5   Q5   Z	B6   Q6   Z	B7   Q7   Z	B8   Q8   Z	B to A
L	L	H	↑	X	B1   B1   L	B2   B2   Z	B3   B3   Z	B4   B4   Z	B5   B5   Z	B6   B6   Z	B7   B7   Z	B8   B8   Z	A to Q
L	H	L	H or L	X	Z   Q1   L	Z   Q2   Q2	Z   Q3   Q3	Z   Q4   Q4	Z   Q5   Q5	Z   Q6   Q6	Z   Q7   Q7	Z   Q8   Q8	A to Q
L	H	L	↑	X	Z   A1   L	Z   A2   A2	Z   A3   A3	Z   A4   A4	Z   A5   A5	Z   A6   A6	Z   A7   A7	Z   A8   A8	Q to B
L	H	H	H or L	X	Z   Q1   L	Z   Q2   Z	Z   Q3   Z	Z   Q4   Z	Z   Q5   Z	Z   Q6   Z	Z   Q7   Z	Z   Q8   Z	A to Q
L	H	H	↑	X	Z   A1   L	Z   A2   Z	Z   A3   Z	Z   A4   Z	Z   A5   Z	Z   A6   Z	Z   A7   Z	Z   A8   Z	
H	L	L	H or L	X	Q1   Q <sub>n</sub> L	Q2   Q <sub>n</sub> Q2	Q3   Q <sub>n</sub> Q3	Q4   Q <sub>n</sub> Q4	Q5   Q <sub>n</sub> Q5	Q6   Q <sub>n</sub> Q6	Q7   Q <sub>n</sub> Q7	Q8   Q <sub>n</sub> Q8	Shift To A and B
H	L	L	↑	H	H   H   L	Q1   Q1   Q1	Q2   Q2   Q2	Q3   Q3   Q3	Q4   Q4   Q4	Q5   Q5   Q5	Q6   Q6   Q6	Q7   Q7   Q7	
H	L	L	↑	L	L   L   L	Q1   Q1   Q1	Q2   Q2   Q2	Q3   Q3   Q3	Q4   Q4   Q4	Q5   Q5   Q5	Q6   Q6   Q6	Q7   Q7   Q7	
H	L	H	H or L	X	Q1   Q <sub>n</sub> L	Q2   Q <sub>n</sub> Z	Q3   Q <sub>n</sub> Z	Q4   Q <sub>n</sub> Z	Q5   Q <sub>n</sub> Z	Q6   Q <sub>n</sub> Z	Q7   Q <sub>n</sub> Z	Q8   Q <sub>n</sub> Z	Shift
H	L	H	↑	H	H   H   L	Q1   Q1   Z	Q2   Q2   Z	Q3   Q3   Z	Q4   Q4   Z	Q5   Q5   Z	Q6   Q6   Z	Q7   Q7   Z	To
H	L	H	↑	L	L   L   L	Q1   Q1   Z	Q2   Q2   Z	Q3   Q3   Z	Q4   Q4   Z	Q5   Q5   Z	Q6   Q6   Z	Q7   Q7   Z	A
H	H	L	H or L	X	Z   Q <sub>n</sub> L	Z   Q <sub>n</sub> Q2	Z   Q <sub>n</sub> Q3	Z   Q <sub>n</sub> Q4	Z   Q <sub>n</sub> Q5	Z   Q <sub>n</sub> Q6	Z   Q <sub>n</sub> Q7	Z   Q <sub>n</sub> Q8	Shift
H	H	L	↑	H	Z   H   L	Z   Q1   Q1	Z   Q2   Q2	Z   Q3   Q3	Z   Q4   Q4	Z   Q5   Q5	Z   Q6   Q6	Z   Q7   Q7	To
H	H	L	↑	L	Z   L   L	Z   Q1   Q1	Z   Q2   Q2	Z   Q3   Q3	Z   Q4   Q4	Z   Q5   Q5	Z   Q6   Q6	Z   Q7   Q7	B
H	H	H	H or L	X	Z   Q <sub>n</sub> L	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Z   Q <sub>n</sub> Z	Shift
H	H	H	↑	H	Z   H   L	Z   Q1   Z	Z   Q2   Z	Z   Q3   Z	Z   Q4   Z	Z   Q5   Z	Z   Q6   Z	Z   Q7   Z	
H	H	H	↑	L	Z   L   L	Z   Q1   Z	Z   Q2   Z	Z   Q3   Z	Z   Q4   Z	Z   Q5   Z	Z   Q6   Z	Z   Q7   Z	

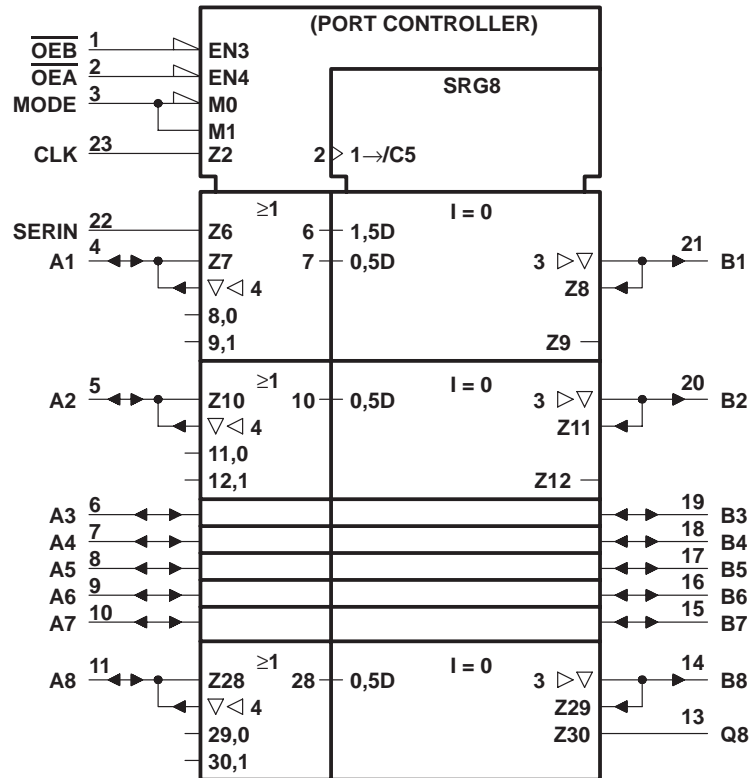
n = level of Q<sub>n</sub>(n = 1, 2 . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as the data travels from port to port are ignored in this table.

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logic symbol†



Pin numbers shown are for DW, JT, and NT packages.

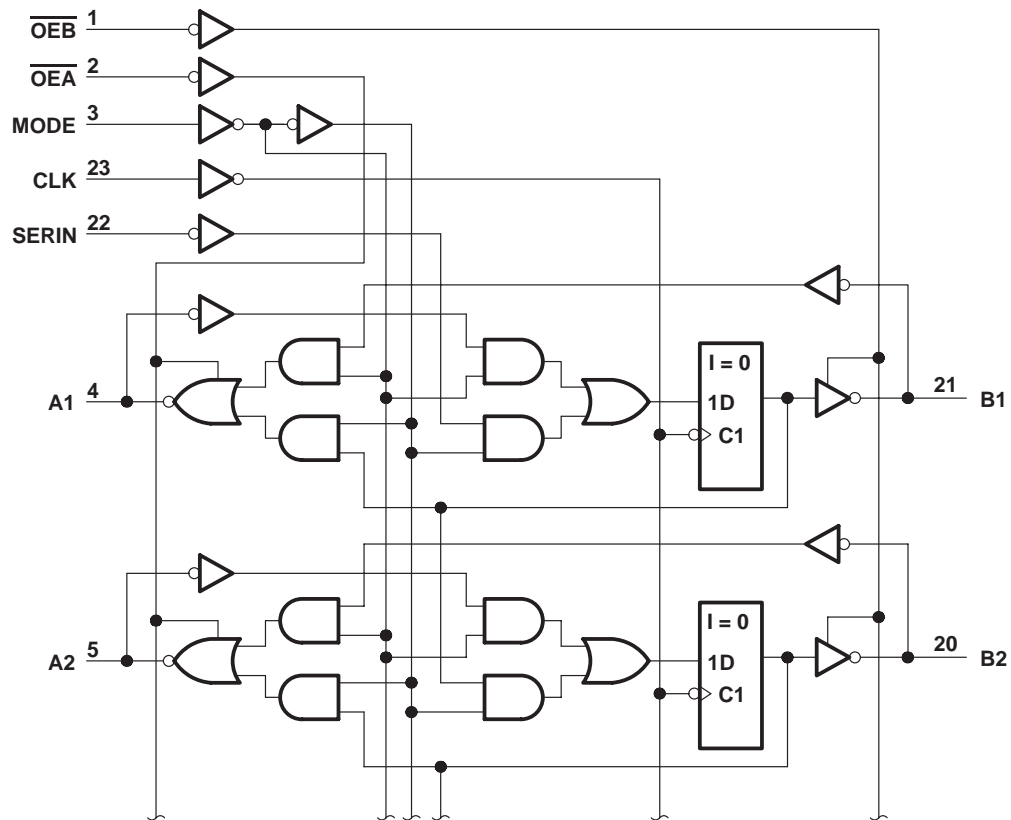
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

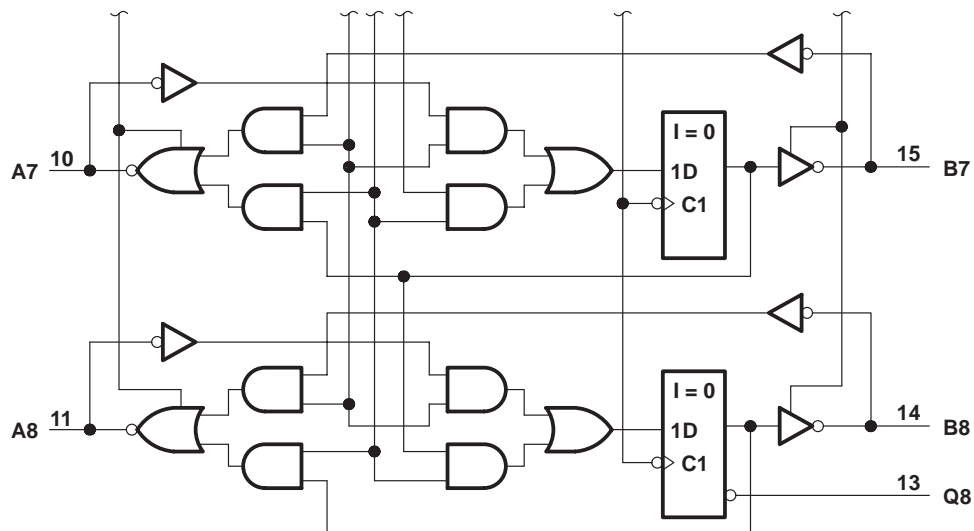
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### logic diagram (positive logic)



Four Identical Channels Not Shown  
Inputs/Outputs Not Shown:

(6) A3	(19) B3
(7) A4	(18) B4
(8) A5	(17) B5
(9) A6	(16) B6



Pin numbers shown are for DW, JT, and NT packages.

**TEXAS**  
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## 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

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### absolute maximum ratings over free-air temperature range

Supply voltage, $V_{CC}$	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS856	–55°C to 125°C
SN74AS856	0°C to 70°C
Storage temperature range	–65°C to 150°C

### recommended operating conditions

			SN54AS856			SN74AS856			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage					0.8			V
I <sub>OH</sub>	High-level output current	A1-A8, B1-B8				−12			mA
		Q8				−2			
I <sub>OL</sub>	Low-level output current	A1-A8, B1-B8				32			mA
		Q8				20			
f <sub>clock</sub>	Clock frequency		0			45			MHz
t <sub>w</sub>	Duration of clock pulse		11			10			ns
t <sub>su</sub>	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		OEB, OEA, MODE	5.5			5.5			
t <sub>h</sub>	Hold-time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		OEB, OEA, MODE	0			0			
T <sub>A</sub>	Operating free-air temperature		−55			125			°C

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54AS856		SN74AS856		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.2		−1.2		V
V <sub>OH</sub>	A1-A8	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = −12 mA	2	3.2			V
	B1-B8	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = −15 mA			2	3.3	
	All outputs	V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −2 mA	V <sub>CC</sub> −2		V <sub>CC</sub> −2		
V <sub>OL</sub>	All outputs except Q8	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 32 mA	0.25 0.5				V
		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA			0.35 0.5		
	Q8	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA	0.5		0.5		
I <sub>I</sub>	OEB, OEA, MODE	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.2		0.2		mA
	CLK and SERIN			0.1		0.1		
	A1-A8, B1-B8	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V	0.2		0.2		
I <sub>IH</sub>	OEB, OEA, MODE	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	40		40		μA
	CLK and SERIN			20		20		
	A1-A8, B1-B8‡			70		70		
I <sub>IL</sub>	OEB, OEA, MODE	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−1		−1		mA
	CLK and SERIN			−0.5		−0.5		
	A1-A8, B1-B8‡			−0.5		−0.5		
I <sub>O§</sub>	Except Q8	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−30	−112	−30	−112	mA
	Q8			−20	−112	−20	−112	
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V		118	200	118	200	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_I$  and  $I_{IL}$  include the output currents  $I_{OZH}$  and  $I_{OZL}$ , respectively.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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### switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX				UNIT
			SN54AS856		SN74AS856		
			MIN	MAX	MIN	MAX	
fmax			45		50		MHz
tPLH	Any B port	Any A port	2	8	2	7	ns
tPHL			2	10.5	2	9.5	
tPLH	↑MODE	Any A or B port	2	8.5	2	7.5	ns
tPHL			5	20	5	19	
tPLH	↓MODE †	Any A or B port	2	8.5	2	7.5	ns
tPHL			2	9.5	2	8	
tPLH	CLK	Any A or B port	3	12	3	9	ns
tPHL			3	12	3	11	
tPLH	CLK	Q8	2	9	2	7.5	ns
tPHL			2	10	2	9	
tPHZ	OE $\overline{\text{A}}$ or OE $\overline{\text{B}}$	Any A or B port	2	9	2	7	ns
tPLZ			2	12	2	9.5	
tPZH			2	8	2	7	ns
tPZL			2	11	2	10	

$\dagger$  The positive transition of the MODE control will cause low-level data at the A output bus or stored in Q to be invalid for 12 ns.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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