

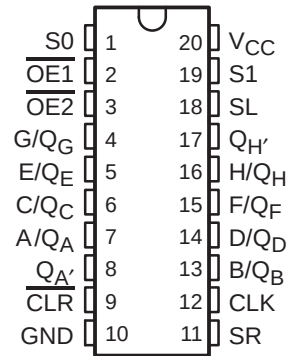
SN74F323

8-BIT UNIVERSAL SHIFT-STORAGE REGISTER WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDFS072A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Four Modes of Operation:**
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operates With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Synchronous Clear
- Applications:
 - Stacked or Push-Down Registers
 - Buffer Storage
 - Accumulator Registers
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)



description

This 8-bit universal register features multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when the clear (CLR) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN74F323 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn	H	QGn
	H	L	H	L	L	↑	X	L	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn	L	QGn
Shift Left	H	H	L	L	L	↑	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. These data inputs are loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

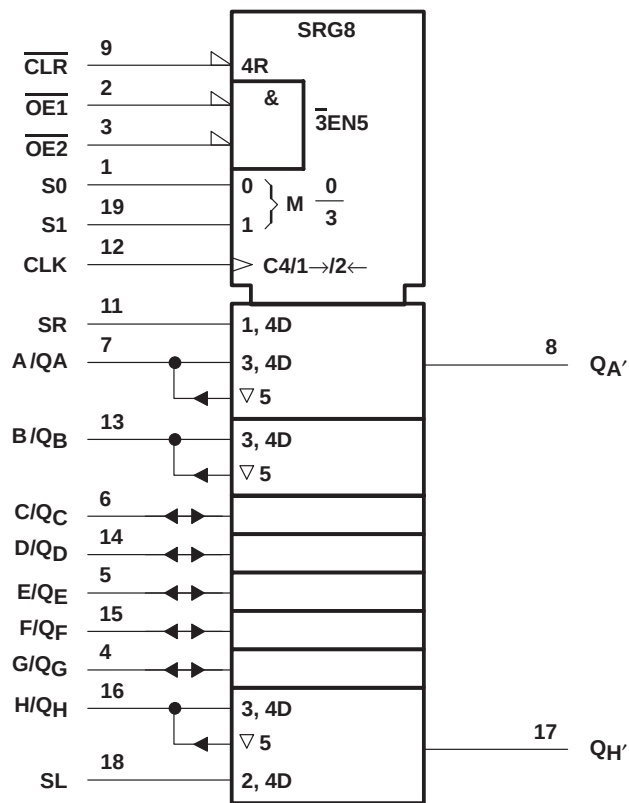
† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

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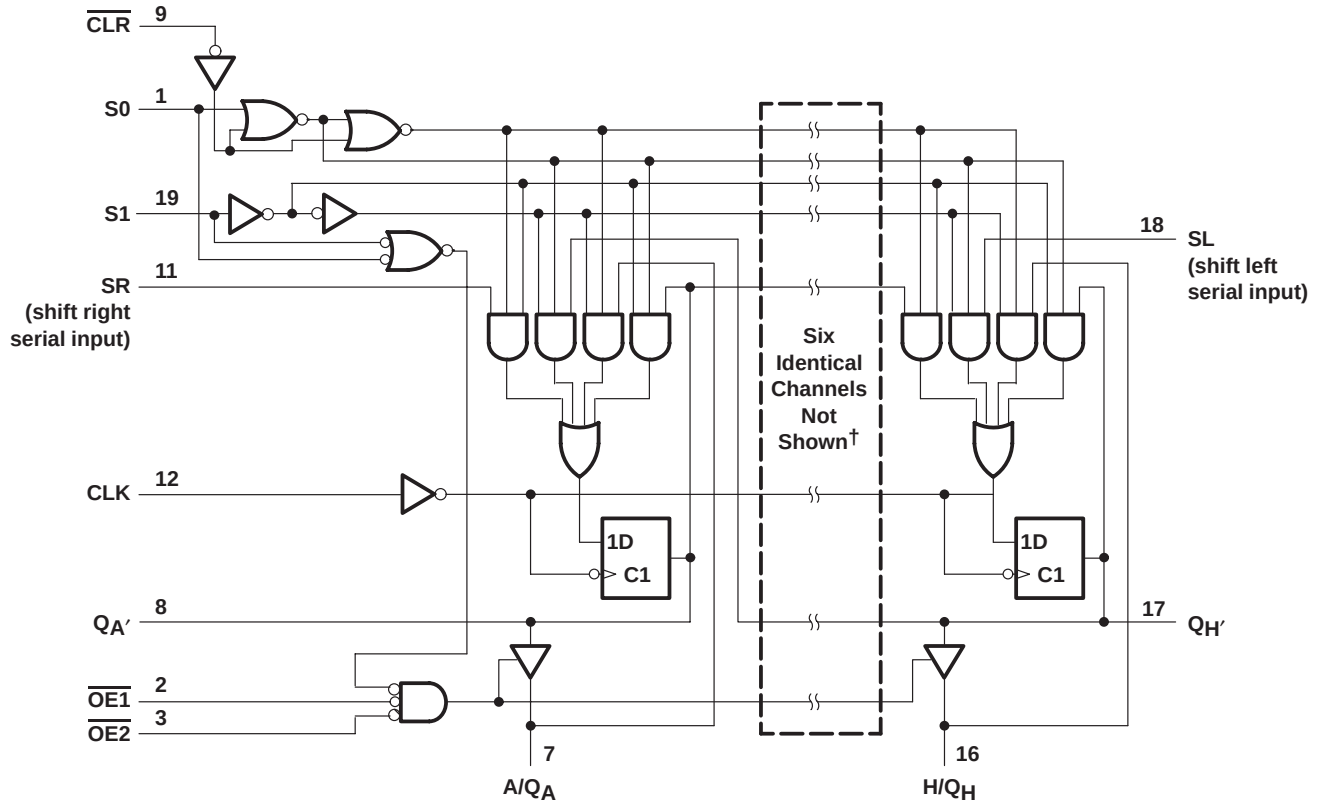
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$	40 mA
Q_A thru Q_H	48 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current	Q_A' or Q_H'		–1	mA
		Q_A thru Q_H		–3	
I_{OL}	Low-level output current	Q_A' or Q_H'		20	mA
		Q_A thru Q_H		24	
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			–1.2	V
V_{OH}	Q_A' or Q_H'	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
	Q_A thru Q_H		$I_{OH} = -1\text{ mA}$	2.5	3.4		
	Q_A thru Q_H		$I_{OH} = -3\text{ mA}$	2.4	3.3		
	Any output	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$	2.7			
V_{OL}	Q_A' or Q_H'	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$		0.3	0.5	V
	Q_A thru Q_H		$I_{OL} = 24\text{ mA}$		0.35	0.5	
I_I	A thru H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$			1	mA
	Any other		$V_I = 7\text{ V}$			0.1	
$I_{IH}^{\ddagger}$	A thru H	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	μA
	Any other					20	
$I_{IL}^{\ddagger}$	A thru H	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			–0.65	mA
	S0 or S1					–1.2	
	Any other					–0.6	
$I_{OS}^{\S}$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	–60		–150	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	See Note 2		68	95	mA

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with $\overline{OE}1$, $\overline{OE}2$, and CLK at 4.5 V.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	70	0	70	MHz
t_w	Pulse duration	CLK high or low	7		7		ns
t_{su}	Setup time before CLK $\uparrow$	S0 or S1	High or low	8.5	8.5		ns
		A/QA thru H/QH, SR, or SL	High or low	5	5		
		CLR	High or low	10	10		
t_h	Hold time after CLK $\uparrow$	S0 or S1	High or low	0	0		ns
		A/QA thru H/QH, SR, or SL	High or low	2	2		
		CLR	High or low	0	0		

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}^\dagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			70	100		70		MHz
t_{PLH}	CLK	QA' or QH'	3.2	6.6	9	3.2	10	ns
t_{PHL}			2.7	6.1	8.5	2.7	9.5	
t_{PLH}	CLK	QA thru QH	3.2	6.6	9	3.2	10	ns
t_{PHL}			4.2	8.1	11	4.2	12	
t_{PZH}	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	QA thru QH	2.7	5.6	8	2.7	9	ns
t_{PZL}			3.2	6.6	10	3.2	11	
t_{PHZ}	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	QA thru QH	1.7	4.1	6	1.7	7	ns
t_{PLZ}			1.2	3.6	5.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

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