TEXAS INSTRUMENTS

TAS3001C

Stereo Audio Digital Equalizer

Data Manual

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1 Introduction

The TAS3001C is a 32-bit processor that performs digital audio signal processing providing parametric equalization, bass, treble, and volume control, as well as dynamic range compression. This results in superior audio quality normally not available in a low-cost solution. Applications for this technology are speaker equalization, microphone equalization, and any audio application where tone, volume, and dynamic range management are important functions.

The TAS3001C provides two digital stereo audio inputs, which are scaled and mixed prior to processing. The parametric EQ consists of multiple cascaded independent biquad filters per left/right channel. Each biquad is composed of five 24-bit coefficients. The user may dynamically adjust the volume, bass, and treble controls without causing the output signal to degrade. The audio control functions (mixer, volume, treble, and bass), dynamic range compression controls, and parametric EQ coefficients are downloaded via the I^2C control port.

The TAS3001C supports three serial audio formats: I^2S, left justified, and right justified. Data word lengths of 16, 18, and 20 bits are supported. See section 2.5 *Serial Audio Interface* for more details. The typical sampling frequency (fs) is 44.1 kHz or 48 kHz.

The digital audio processor and on-chip logic are sequenced via an internal system clock that is derived from an external MCLK (master clock). Also derived from MCLK are LRCLKOUT and SCLKOUT signals that provide clocks to the TAS3001C and other devices in the system.

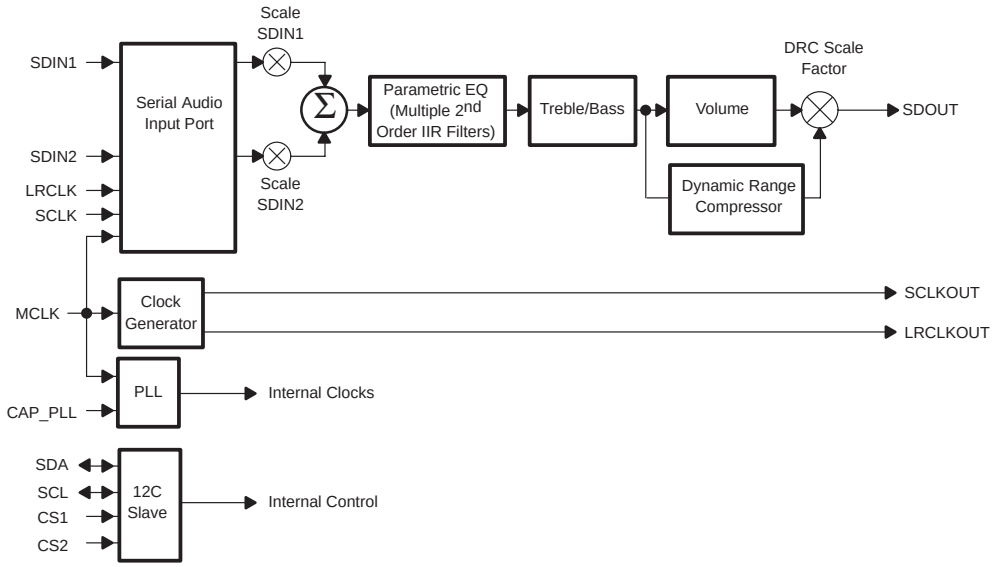
Two address-select pins are provided to allow multiple TAS3001Cs to be cascaded on the I^2C bus. This allows speaker EQ to be provided to 3-channel systems consisting of left, right, and subwoofer speakers as well as 6-channel systems consisting of left, right, center, rear left, rear right, and subwoofer speakers.

1.1 Features

- Programmable Serial Audio Port
- Two Input Data Channels (SDIN1 and SDIN2)
- Single Digital Output Data Channel (SDOUT)
- Programmable Digital Mixer
- Programmable Multiband Digital Parametric EQ
- Programmable Digital Bass and Treble Control (dynamically updateable)
- Programmable Digital Volume Control (dynamically updateable)
- Dynamic Range Compression (DRC)
- Serial I^2C Slave Port Allows Downloading of Control Data to the Device
- Two I^2C Address Pins Allow Cascading of Multiple Devices on the I^2C Bus
- Supports 2 Speaker, 3 Speaker†, and 6 (5.1) Speaker† Systems
- Soft Mute via Software Control
- Single 3.3-V Power Supply Operation
- 28-Pin PW Package

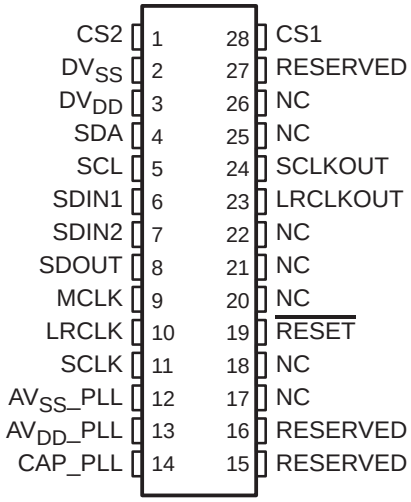
† Requires multiple TAS3001C devices

1.2 Functional Block Diagram



1.3 Terminal Assignments

PW PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 70°C	TAS3001CPW

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}_PLL	13	I	Analog power supply for the PLL
AV_{SS}_PLL	12	I	Analog ground for the PLL
CAP_PLL	14	I	C1 = 1500 pF // R1 = 27 Ω + C2 = 0.068 μF (recommended)
CS1	28	I	I^2C address bit A0; low = 0, high = 1
CS2	1	I	I^2C address bit A1; low = 0, high = 1
DV_{DD}	3	I	Digital power supply
DV_{SS}	2	I	Digital ground
LRCLK	10	I	I^2S left/right clock sampling frequency (f_S)
LRCLKOUT	23	O	LRCLK generated from input MCLK (usually 256 f_S) – normally routed on PCB to pin 10 (LRCLK) as input f_S sample clock.
MCLK	9	I	Master clock
NC	17, 18, 20–22, 25, 26		Reserved – No connection for normal operation
$\overline{\text{RESET}}$	19	I	Reset, high = normal operation, low = reinitialize the device
RESERVED	15, 16, 27		Reserved – digital ground for normal operation
SCL	5	I/O	Slave serial I^2C clock
SCLK	11	I	Shift clock (bit clock)
SCLKOUT	24	O	SCLK generated from input MCLK (usually 256 f_S) – normally routed on PCB to pin 11 (SCLK) as input 64 f_S bit clock.
SDA	4	I/O	Slave serial I^2C data
SDIN1	6	I	Serial audio data input one
SDIN2	7	I	Serial audio data input two
SDOUT	8	O	Serial audio data output

2 Description

2.1 Serial Audio Interface

- Programmable serial audio port
  - I^2S, left justified, and right justified
- Dual input data channels (SDIN1 and SDIN2)
  - 16-,18-, or 20-bit resolution (see Section 6.1, *Audio Data*)
- Single output data channel (SDOUT)
  - 16-,18-, or 20-bit resolution (see Section 6.1, *Audio Data*)
- Accepts 32 f_S or 64 f_S (SCLK)†
- Two I^2C programmable address pins (CS1 and CS2)

2.2 Serial Control Interface

- I^2C slave port
- Downloads EQ coefficients
- Volume, bass, treble, and mixer control
- DRC control
- Write only

2.3 Audio Processing

- Programmable multiband digital parametric EQ (dynamically updateable)
- Programmable volume control (dynamically updateable)
- Soft mute software controlled
- Digital mixing of SDIN1 and SDIN2 with independent gain control
- Programmable bass and treble tone control (dynamically updateable)
- Dynamic range compression (DRC)

2.4 Power Supply

- Digital supply voltage – DV_{DD}, DV_{SS} of 3.3 V
- Analog supply voltage – AV_{DD}_PLL, AV_{SS}_PLL of 3.3 V

† 32 f_S serial input mode is left justified 16 bit only

2.5 Serial Audio Interface

2.5.1 I²S Serial Format

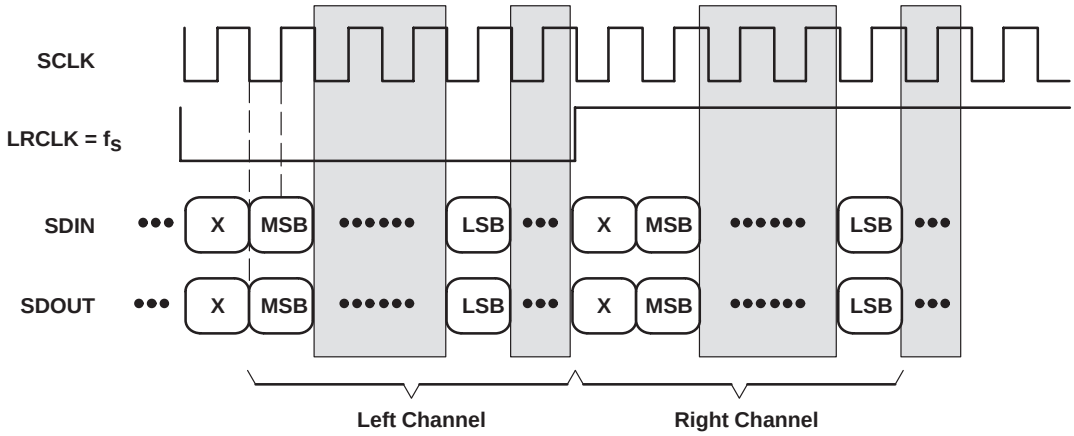


Figure 2–1. I²S Compatible Serial Format

2.5.2 Protocol

1. LRCLK = Sampling frequency (f_S)
2. Left channel is transmitted when LRCLK is low.
3. SCLK = 64 × LRCLK. SCLK is sometimes referred to as the bit clock.
4. Serial data is sampled with the rising edge of SCLK.
5. Serial data is transmitted on the falling edge of SCLK.
6. LRCLK must have a 50% duty cycle.

2.5.3 Implementation

1. LRCLK and SCLK are both inputs.

2.5.4 Timing

See Figure 4–1 for I²S timing.

2.6 Left-Justified Serial Format

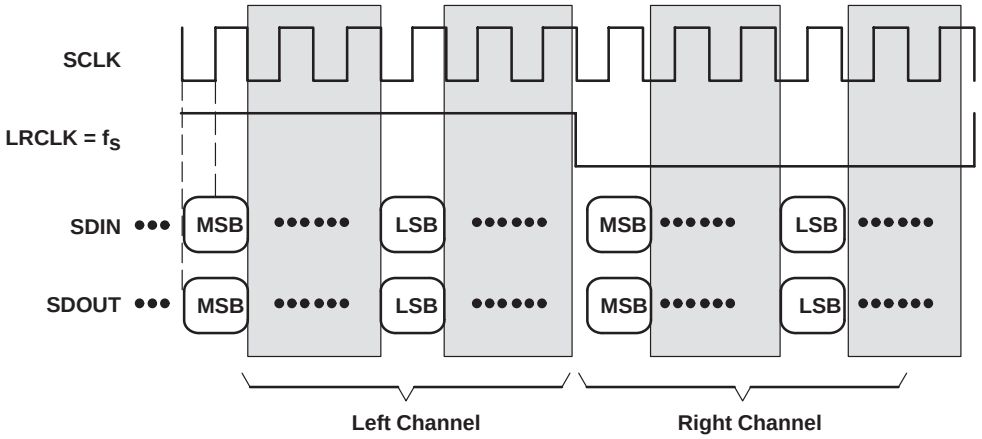


Figure 2–2. Left-Justified Serial Format

2.6.1 Protocol

1. LRCLK = Sampling frequency (f_S)
2. Left channel is transmitted when LRCLK is high.
3. The SDIN1 data is justified to the leading edge of the LRCLK.
4. Serial data is sampled on the rising edge of SCLK.
5. Serial data is transmitted on the falling edge of SCLK.
6. SCLK = 32 LRCLK (32 f_S SCLK is only supported for 16 bit data) or 64 LRCLK
7. In this mode, LRCLK does not have to be a 50% duty cycle clock. The number of bits used in the interface sets the minimum duty cycle. There must be enough SCLK pulses to shift all of the data.

2.6.2 Implementation

1. LRCLK and SCLK are both inputs.

2.6.3 Timing

See Figure 4–1 for I^2S timing.

2.7 Right-Justified Serial Format

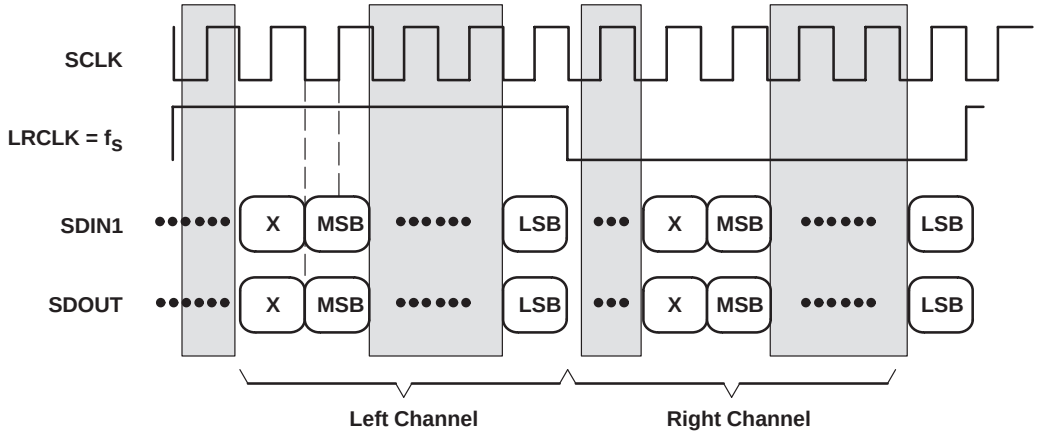


Figure 2–3. Right-Justified Serial Format

2.7.1 Protocol

1. LRCLK = Sampling frequency (f_S)
2. Left channel is transmitted when LRCLK is high.
3. The SDIN1 data is justified to the trailing edge of the LRCLK.
4. Serial data is sampled on the rising edge of SCLK.
5. Serial data is transmitted on the falling edge of SCLK.
6. SCLK = 64 LRCLK
7. In this mode, LRCLK does not have to be a 50% duty cycle clock. The number of bits used in the interface sets the minimum duty cycle. There must be enough SCLK pulses to shift all of the data.

2.7.2 Implementation

1. LRCLK and SCLK are both inputs.

2.7.3 Timing

See Figure 4–1 for I^2S timing.

2.8 System Clocks – Master Mode and Slave Mode

The TAS3001 allows multiple system clocking schemes. In this document, master mode indicates that the TAS3001 provides system clocks (LRCLK and SCLK) to other parts of the system. Slave mode indicates that a system master other than theTAS3001 provides system clocks (LRCLK and SCLK) to the TAS3001. These are depicted in Figures 2–4 and 2–5.

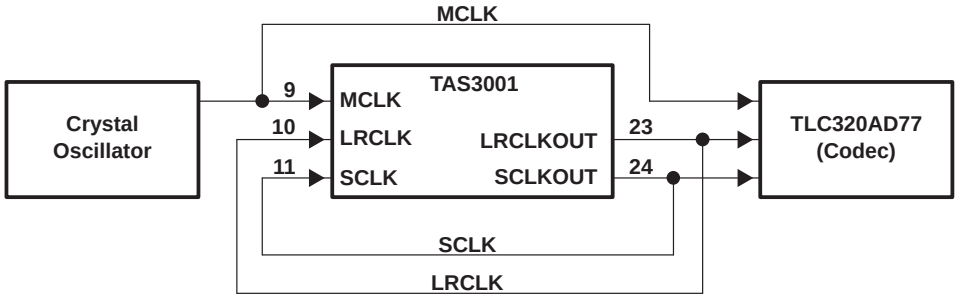


Figure 2–4. Master Mode

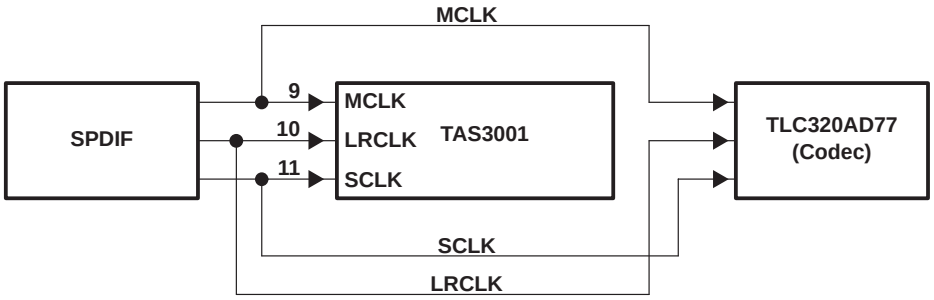


Figure 2–5. Slave Mode

2.9 Serial Control Interface

Control parameters for the TAS3001C are loaded with an I^2C master interface. Information is loaded into the registers defined in Appendix A, *Software Interface*. The I^2C bus uses two pins, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. This device may be addressed by sending a unique 7-bit slave address plus R/W bit (1 byte). All I^2C compatible devices share the same pins via a bidirectional bus using a wire-ANDed connection. A pullup resistor must be used to set the high level on the bus. The TAS3001C operates in standard I^2C mode up to 100 kbps with as many devices on the bus as desired up to the capacitance load limit of 400 pF. Additionally, the TAS3001C operates only in slave mode; therefore, at least one device connected to the I^2C bus with this device must operate in master mode.

2.9.1 I^2C Protocol

The bus standard uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop condition. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 2–6. These start and stop conditions for the I^2C bus are required by standard protocol to be generated by the master. The master must also generate the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The slave holds the SDA bit low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master begins transmitting. After each 8-bit word, an acknowledgment must be transmitted by the receiving device. There is no limit on the number of bytes that may be transmitted between a start and stop condition. When the last word has been transferred, the master must generate a stop condition to release the bus. A generic data transfer sequence is shown in Figure 2–6.

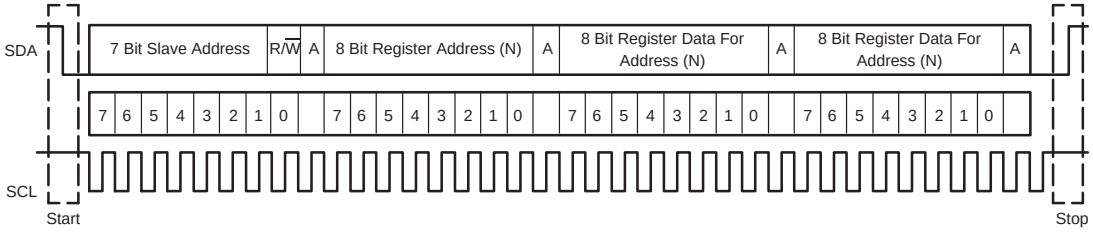


Figure 2–6. Typical I²C Data Transfer Sequence

The definitions used by the I²C protocol are listed below.

Transmitter	The device that sends data
Receiver	The device that receives data
Master	The device that initiates a transfer, generates clock signals, and terminates the transfer
Slave	The device addressed by the master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure to ensure the message is not corrupted when two masters attempt to control the bus
Synchronization	Procedure to synchronize the clock signals of two or more devices

2.9.2 Operation

The 7-bit address for the TAS3001C is 01101XX, where X is a programmable address bit. Using the CS1 and CS2 pins on the device, the two LSB address bits may be programmed. These four addresses are licensed I²C addresses and will not conflict with other licensed I²C audio devices. To communicate with the TAS3001C, the I²C master must use 01101XX. In addition to the 7-bit device address, subaddresses are used to direct communication to the proper memory location within the device. A complete table of subaddresses and control registers is provided in the Appendix A, *Software Interface*. For example, to change the bass setting to 10-dB gain, Section 2.8.2.1, *Write Cycle* shows how the subaddress and data are written to the I²C port:

Table 2–1. I²C Address Byte

I²C ADDRESS BYTE	A6–A2	CS2(A1)	CS1(A0)	R/$\overline{W}$†
0x68	01101	0	0	0
0x6A	01101	0	1	0
0x6C	01101	1	0	0
0x6E	01101	1	1	0

† The TAS3001C is a write only device.

2.9.2.1 Write Cycle

When writing to a subaddress, the correct number of data bytes must follow in order to complete the write cycle. For example, if the volume control register with subaddress 04 (hex) is written to, six bytes of data must follow, otherwise the cycle will be incomplete. The correct number of bytes corresponding to each subaddress is shown in Appendix A, *Software Interface*.

Start	Slave Address	R/W	A	Subaddress	A	Data	A	Stop

FUNCTION	DESCRIPTION
Start	Start condition as defined in I^2C
Slave address	0110100 (CS1 = CS2 = 0)
R/$\overline{W}$	0 (write)
A	Acknowledgement as defined in I^2C (slave)
Subaddress	00000110 (see Appendix A, *Software Interface*)
Data	00011100 (see Appendix A, *Software Interface*)
Stop	Stop condition as defined in I^2C

NOTE: This table applies to serial data (SDA). Serial clock (SCL) information is not shown since the same conditions apply as well.

2.10 Filter Processor

2.10.1 Biquad Block

The biquad block consists of multiple digital biquad filters per channel organized in a cascade structure as shown in Figure 2–7. Each of these biquad filters has five downloadable 24-bit (4.20) coefficients. Each stereo channel has independent coefficients. Note that the filters are implemented with 32-bit arithmetic and 56-bit accuracy for some internal calculations.

Figure 2–7. Biquad Cascade Configuration

2.10.2 Filter Coefficients

The filter coefficients for the TAS3001C are downloaded through the I^2C port and loaded into the biquad memory space. Digital audio data coming into the device is processed by the biquad filters and then output from the device usually to an external DAC. Any biquad filter may be downloaded and processed by the TAS3001C. The biquad structure that is used for the parametric equalization filters is as follows:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}$$

NOTE: a_0 is fixed at value 1 and is not downloadable

The coefficients for these filters are quantized and represented in 4.20 format – 4 bits for the integer part and 20 bits for the fractional part. In order to transmit them over I^2C, it is necessary to separate each coefficient into three bytes. The first nibble of byte 2 is the integer part, and the second nibble of byte 2 and bytes 1 and 0 are the fractional parts.

2.11 Volume Control Functions

2.11.1 Soft Volume Update

The TAS3001C implements a TI proprietary soft volume update. This update allows a smooth and pleasant-sounding change from one volume level to another over the entire range of volume (18 dB to mute). The volume is adjustable by downloading a 4.16 (see NOTE) gain coefficient through the I^2C interface. Tables converting the 4.16 coefficient to dB in a range from –70 dB to 18 dB in 0.5 dB increments are found in Table A–6.

4.16 values other than those listed in Table A–6 are also allowed.

2.11.2 Software Soft Mute

Mute is implemented by loading all zeros in the volume control register. This will cause the volume to ramp down over a maximum of 2048 samples to a final output of zero (– infinity dB).

2.11.3 Mixer Control

The TAS3001C is capable of mixing and muxing two channels of serial audio data. This is accomplished by loading values into the MIXER1 and MIXER2 control registers. The values loaded into these registers are in 4.20 (see NOTE) format. Table A–9 contains 4.20 numbers converted into dB for the range –70 dB to 18 dB, although any positive 4.20 number may be used.

NOTE:

The 4.N number is a two's complement number with 1 sign bit, 3 integer bits, and N bits of fraction. Only positive numbers should be used for the volume and gain controls. The formula for converting a 4.N number to dB is: dB = 20 LOG(X), where X is a positive 4.N number.

To mute either channel, zeros are loaded into either of the mixer control registers.

The mixer controls are updated instantly and may cause audible artifacts when updated dynamically outside of fast load mode.

2.11.4 Treble Control

The treble gain level may be adjusted within the range of 18 dB to –18 dB with 0.5 dB step resolution. The level changes are accomplished by downloading treble codes shown in Appendix A, *Software Interface* Section.

2.11.5 Bass Control

The bass gain level may be adjusted within the range of 18 dB to –18 dB with 0.5 dB step resolution. The level changes are accomplished by downloading bass codes shown in Appendix A, *Software Interface*.

2.11.6 Dynamic Range Compression

The TAS3001C provides the user with the ability to manage the dynamic range of the audio system. The dynamic range compressor receives data after the bass control block, and affects scaling after the volume control block. Refer to Figure 2–8. The compressor does not employ a delay as used in many common compressors. This makes the compressor appropriate for this low-cost application without significantly degrading performance since the saturation logic, which is applied after the compressor scale factor, serves as a hard limiter that will not allow the signal to extend beyond the available range. Of course, the compressor can be adjusted such that the signal will not generally reach the hard limit value.

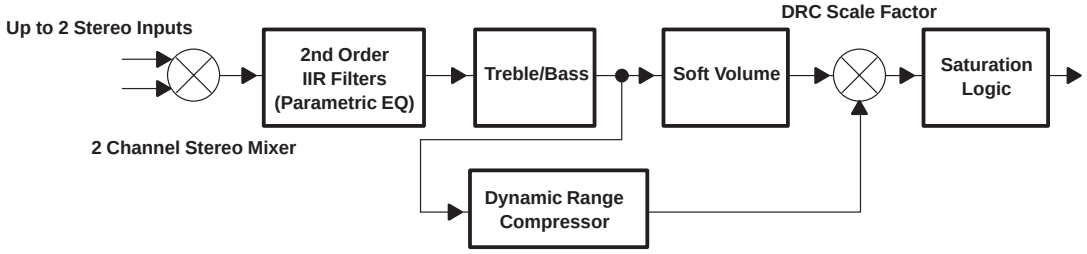


Figure 2–8. TAS3001C Digital Signal Processing Block Diagram

The compression threshold is adjustable in increments of 1/2 dB between 0 dB and approximately –36 dB. The compression ratio is set to 3:1.

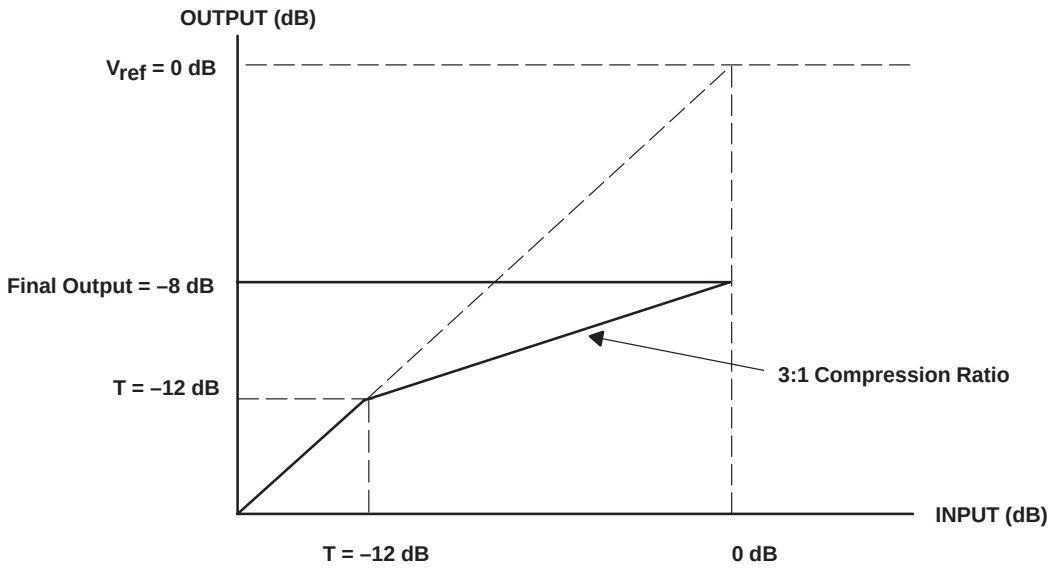


Figure 2–9. DRC Example With Threshold = –12 dB

From the DRC example shown in Figure 2–7, the formula for calculating the output with a given threshold and the fixed compression ratio of 3:1 is:

$$\text{Final output (dB)} = [\text{T (dB)} + [\text{Vref (dB)} - \text{T (dB)}] \times (1/\text{CR})]$$

Where

CR = compression ratio = 3
T = Threshold (dB) = –12 dB
V_{ref} = Reference voltage (normally 0 dB)

As show in Figure 2–7, with the threshold set to –12 dB, if the input exceeds this value, then the output will be compressed at a 3:1 ratio until the max input of 0 dB yields an output of –8 dB.

2.12 Device Initialization

2.12.1 Reset

The reset pin allows the device to be reset. That is, the TAS3001C returns to its default state as defined in this section. The device does not reset automatically when power is applied to the device. A reset is required after the following condition occurs:

- Power is applied to any of the power pins.

Since the MCR sets the serial mode and fast load, it is recommended that it is written to only once, following reset. However, there are systems in which the user modifies the MCR without having to reset it first.

Required conditions for a successful reset:

- MCLK is running
- RESET is low for a minimum of 1 μs.

2.12.2 Device Power On Plus Reset

When power is applied to the TAS3001C, the device will power up in an unknown state. It must be reset before the device will be in a known state. Upon reset, the TAS3001C will initialize to its default state (fast load mode). The main control register will be configured to 1XXXXXXX, where X is not initialized, as shown in Figure 2–10 (see Appendix A for complete description of MCR). Only the fast load bit will be set to a 1

in the main control register. This puts the device into fast load mode (see Section 2.12.3, *Fast Load*). All random access memory (RAM) will be initialized (previous data will be overwritten).

Bit 7							Bit 0
1	X	X	X	X	X	X	X

Figure 2–10. Main Control Register (MCR)

The I^2C address pins (CS1 and CS2) should be driven or biased to set the TAS3001C to a known I^2C address. This also ensures the I^2C port will be active immediately after the reset initialization phase. Furthermore, when implementing a three or six speaker system, the CS1 and CS2 pins must always be driven or set to unique addresses on all devices. The I^2C port will be powered up but will not acknowledge any I^2C bus activity until the entire device has been initialized. This initialization typically takes 5 ms.

2.12.3 Fast Load

Upon entering fast load mode, the following occurs as part of initialization:

- All of the parametric EQ will be initialized to 0 dB (all-pass).
- The tone (bass/treble) will be set to 0 dB.
- The mix function will set SDIN1 to 0 dB and SDIN2 to mute (no-pass).
- The volume will be set to mute.

While in fast load mode, it is possible to update the parametric EQ without any audio processing delay. The audio processor will be paused while the RAM is being updated in this mode. It is recommended that parametric EQ be downloaded in this mode. Bass and treble may not be downloaded in this mode. Mixer1 and Mixer2 registers may be downloaded in this mode or normal mode (FL bit = 0). It is not recommended to download the volume control register and mixer registers in this mode. Once the download is complete, the fast load bit needs to be cleared by writing a 0 into bit 7 of the main control register. This puts the TAS3001C into normal mode.

NOTE:

When writing to the FL bit in the MCR, the serial audio format is also written to at this time. However, the device will not recognize any serial audio until it has returned to normal mode. Entering fast load mode by resetting the TAS3001C is recommended. Once back in normal mode, treble, bass, and volume control may be downloaded to complete device setup.

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD}_PLL, DV_{DD} . . . . . –0.3 to 4.2 V
Digital Input voltage range . . . . . –0.3 to V_{DD} + 0.3 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 10 seconds . . . . . 122.3°C
Lead temperature from case for 10 seconds . . . . . 97.8°C
ESD tolerance‡ . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Human Body Model per Method 3015.2 of MIL-STD-883B.

3.2 Recommended Operating Conditions

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
PLL supply voltage, AV_{DD}		3	3.3	3.6	V
Digital IC supply voltage, DV_{DD}		3	3.3	3.6	V
PLL and digital IC supply current, I_{DD}	V_{DD} = 3.3 V, No load		20		mA
Capacitive load for each bus line $C_{L(bus)}$	SDA, SCL			400	pF
Operating free-air temperature, T_A		0	25	70	°C

3.3 Static Digital Specifications, T_A = 0°C to 70°C, all V_{DD} = 3.3 V ± 0.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{DD} +0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_O = –1 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_O = 4 mA			0.4	V
I_{IH}	High-level input leakage current		–10		10	µA
I_{IL}	Low-level input leakage current		–10		10	µA
I_{OZH}	High-level output leakage current	SCL, SDA	–10		10	µA
I_{OZL}	Low-level output leakage current	SCL, SDA	–10		10	µA

3.4 Audio Serial Port Timing Requirements (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$f_{(SCLK)}$	Frequency, SCLK	32 f_S†		64 f_S	MHz
$f_{(SCLKOUT)}$	Frequency, SCLKOUT		$\frac{MCLK}{4}$		MHz
$f_{(LRCLKOUT)}$	Frequency, LRCLKOUT		$\frac{MCLK}{256}$		MHz
$t_{r(SCLK)}$	Rise time, SCLK (see Note 2)	5	16.3	25	ns
$t_{f(SCLK)}$	Fall time, SCLK (see Note 2)	5	16.3	25	ns
$t_{d(SLR)}$	Delay time, SCLK rising to LRCLK edge (see Note 3)	50	$\frac{T_{SCLK}}{2}$		ns
$t_{d(SDOUT)}$	Delay time, SDOUT valid from SCLK falling			100	ns
$t_{su(SDIN)}$	Setup time, SDIN before SCLK rising edge	10			ns
$t_{h(SDIN)}$	Hold time, SDIN from SCLK rising edge	100			ns

† Valid in 16-bit left justified mode only.

NOTES: 1. Timing relative to 256 f_S MCLK.
2. SCLK rising and falling are measured from 20% to 80%.
3. The rising edge of SCLK must not occur at the same time as either edge of LRCLK.

3.5 I^2C Serial Port Timing Requirements

PARAMETER		MIN	MAX	UNIT
$f_{(scl)}$	SCL clock frequency	0	100	kHz
t_{BUF}	Bus free time between start and stop	4.7		µs
$t_{w(low)}$	Pulse duration, SCL clock low (see Note 4)	4.7		µs
$t_{w(high)}$	Pulse duration, SCL clock high (see Note 5)	4		µs
$t_{h(STA)}$	Hold time, repeated start	4		µs
$t_{su(STA)}$	Setup time, repeated start	4.7	20	µs
$t_{h(DAT)}$	Hold time, data	0†		µs
$t_{su(DAT)}$	Setup time, data	250		ns
t_r	Rise time for SDA and SCL		1000	ns
t_f	Fall time for SDA and SCL		300	ns
$t_{su(STO)}$	Setup time for stop condition	4		µs

† A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

NOTES: 4. $t_{w(low)}$ is measured from the end of t_f to the beginning of t_r.
5. $t_{w(high)}$ is measured from the end of t_r to the beginning of t_f.

4 Parameter Measurement Information

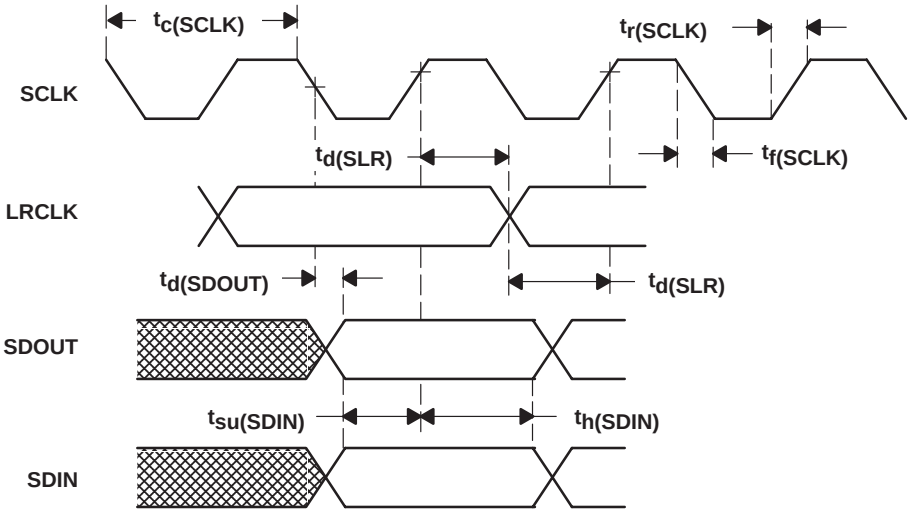


Figure 4–1. I^2S Timing

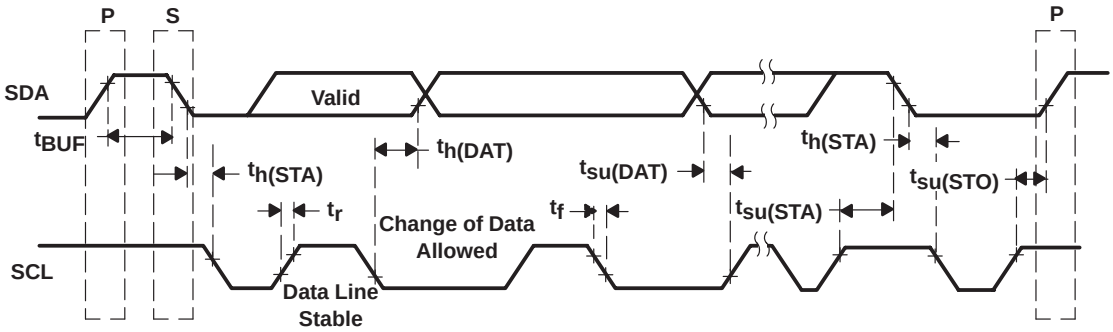


Figure 4–2. I^2C Timing

5 Application Information

Typical applications for the TAS3001C include:

- PC laptop audio
- Digital speakers
- Multimedia monitors with speakers
- USB audio devices
- MP3 players
- Portable stereo

Appendix A
Software Interface

Table A–1. Register Map

REGISTER	ADDRESS	NO. of BYTES	BYTE DESCRIPTION
Reserved	0x00		
MCR	0x01	1	C(7–0)
DRC	0x02	2	See DRC section
Reserved	0x03		
Volume†	0x04	6	VL(23–16), VL(15–8), VL(7–0), VR(23–16), VR(15–8), VR(7–0)
Treble	0x05	1	T(7–0)
Bass	0x06	1	B(7–0)
Mixer 1‡	0x07	3	S(23–16), S(15–8), S(7–0)
Mixer 2‡	0x08	3	S(23–16), S(15–8), S(7–0)
Reserved	0x09		
Left Biquad 0	0x0A	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Left Biquad 1‡	0x0B	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Left Biquad 2‡	0x0C	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Left Biquad 3‡	0x0D	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Left Biquad 4‡	0x0E	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Left Biquad 5‡	0x0F	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0) A_2(23–16), A_2(15–8), A_2(7–0)
Reserved	0x10		
Reserved	0x11		
Reserved	0x12		

† The volume value is a 4.16 coefficient. In order to transmit it over I^2C, it is necessary to separate the value into three bytes. Byte 2 is the integer part and bytes 1 and 0 are the fractional parts.

‡ The mixer gain values and biquad coefficients are 4.20 coefficients. In order to transmit them over I^2C, it is necessary to separate the value into three bytes. The first nibble of byte 2 is the integer part and the second nibble of byte 2 and bytes 1 and 0 being the fractional parts.

Table A–1. Register Map (Continued)

REGISTER	ADDRESS	NO. of BYTES	BYTE DESCRIPTION
Right Biquad 0‡	0x13	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Right Biquad 1‡	0x14	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Right Biquad 2‡	0x15	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Right Biquad 3‡	0x16	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Right Biquad 4‡	0x17	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Right Biquad 5‡	0x18	15	B_0(23–16), B_0(15–8), B_0(7–0), B_1(23–16), B_1(15–8), B_1(7–0), B_2(23–16), B_2(15–8), B_2(7–0), A_1(23–16), A_1(15–8), A_1(7–0), A_2(23–16), A_2(15–8), A_2(7–0)
Reserved	0x19 to 0xFF		

† The volume value is a 4.16 coefficient. In order to transmit it over I^2C, it is necessary to separate the value into three bytes. Byte 2 is the integer part and bytes 1 and 0 are the fractional parts.

‡ The mixer gain values and biquad coefficients are 4.20 coefficients. In order to transmit them over I^2C, it is necessary to separate the value into three bytes. The first nibble of byte 2 is the integer part and the second nibble of byte 2 and bytes 1 and 0 being the fractional parts.

Main Control Register (MCR)

Configuration of the digital serial audio interface is set up through the main control register as shown below. Bits F0 and F1 allow selection between three different serial data formats (right justified = 00, right justified = 01, and I^2S standard = 10). The output serial port mode set by E0 and E1 must be set to the same value as the input serial port mode set by F0 and F1. Bits W0 and W1 allow selection between three different word widths (16-bit word = 00, 18-bit word = 01, and 20-bit word = 10). The SC bit selects $32f_S$ (0) or $64f_S$ (1) bit clock. The FL bit is primarily for use during initialization and is defined in the device initialization section. See Section 2.8 *Serial Control Interface* for additional information on how to address the main control register.

Table A–2. Main Control Register (MCR)

C7	C6	C5	C4	C3	C2	C1	C0
FL	SC	E1	E0	F1	F0	W1	W0
1	x	x	x	x	x	x	x

Table A–3. Main Control Register (MCR) Description

BIT	DESCRIPTOR	FUNCTION	VALUE	FUNCTION
C(7)	FL	Fast load	0	Normal operating mode
			1 (default)	Fast load mode
C(6)	SC	SCLK frequency	0	SCLK = 32 f_S
			1	SCLK = 64 f_S
C(5,4)	E(1,0)	Output serial port mode	00	Left justified
			01	Right justified
			10	I^2S
			11	Reserved
C(3,2)	F(1,0)	Input serial port mode	00	Left justified
			01	Right justified
			10	I^2S
			11	Reserved
C(1,0)	W(1,0)	Serial port word length	00	16 bit
			01	18 bit
			10	20 bit
			11	Reserved

Table A–4. DRC Interface (Byte 1)

B7	B6	B5	B4	B3	B2	B1	B0
CR1	CR0	X	X	X	X	X	EN

BIT	DESCRIPTOR	FUNCTION	VALUE	FUNCTION
B0	EN	Enable DRC	0	Disabled
			1	Enabled
B7, B6	CR1, CR0	Compression ratio	00	Invalid
			01	Invalid
			10	Invalid
			11	3:1

Table A–5. DRC Interface (Byte 2)

DRC Interface Byte 2 sets the threshold value. It is a 4.4 number and *should always be greater than 9.0* (10010000). Legal values range from hex 91 to F0.

BYTE 2 (BITS) MIN	BYTE 2 (BITS) MAX	HEX MIN – MAX	DECIMAL MIN – MAX	DESCRIPTION
10010000	10010000	90	9.0	ILLEGAL
10010001	10011111	91 – 9F	9.0625 – 9.9375	91 ~ –36 dB
10100000	10101111	A0 – AF	10.0 – 10.9375	A0 = –30 dB
10110000	10111111	B0 – BF	11.0 – 11.9375	B0 = –24 dB
11000000	11001111	C0 – CF	12.0 – 12.9375	C0 = –18 dB
11010000	11011111	D0 – DF	13.0 – 13.9375	D0 = –12 dB
11100000	11101111	E0 – EF	14.0 – 14.9375	E0 = –6 dB
11110000	11110000	F0	15.0	F0 = 0 dB

Table A–6. Volume Gain Values
[The gain error is less than 0.12 dB (excluding mute)]

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
18.0	07, F1, 7B
17.5	07, 7F, BB
17.0	07, 14, 57
16.5	06, AE, F6
16.0	06, 4F, 40
15.5	05, F4, E5
15.0	05, 9F, 98
14.5	05, 4F, 10
14.0	05, 03, 0A
13.5	04, BB, 44
13.0	04, 77, 83
12.5	04, 37, 8B
12.0	03, FB, 28
11.5	03, C2, 25
11.0	03, 8C, 53
10.5	03, 59, 83
10.0	03, 29, 8B
9.5	02, FC, 42
9.0	02, D1, 82
8.5	02, A9, 25
8.0	02, 83, 0B
7.5	02, 5F, 12
7.0	02, 3D, 1D
6.5	02, 1D, 0E
6.0	01, FE, CA
5.5	01, E2, 37
5.0	01, C7, 3D
4.5	01, AD, C6
4.0	01, 95, BC
3.5	01, 7F, 09
3.0	01, 69, 9C
2.5	01, 55, 62
2.0	01, 42, 49
1.5	01, 30, 42
1.0	01, 1F, 3D
0.5	01, 0F, 2B

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
0.0	01, 00, 00
–0.5	00, F1, AE
–1.0	00, E4, 29
–1.5	00, D7, 66
–2.0	00, CB, 59
–2.5	00, BF, F9
–3.0	00, B5, 3C
–3.5	00, AB, 19
–4.0	00, A1, 86
–4.5	00, 98, 7D
–5.0	00, 8F, F6
–5.5	00, 87, E8
–6.0	00, 80, 4E
–6.5	00, 79, 20
–7.0	00, 72, 5A
–7.5	00, 6B, F4
–8.0	00, 65, EA
–8.5	00, 60, 37
–9.0	00, 5A, D5
–9.5	00, 55, C0
–10.0	00, 50, F4
–10.5	00, 4C, 6D
–11.0	00, 48, 27
–11.5	00, 44, 1D
–12.0	00, 40, 4E
–12.5	00, 3C, B5
–13.0	00, 39, 50
–13.5	00, 36, 1B
–14.0	00, 33, 14
–14.5	00, 30, 39
–15.0	00, 2D, 86
–15.5	00, 2A, FA
–16.0	00, 28, 93
–16.5	00, 26, 4E
–17.0	00, 24, 29
–17.5	00, 22, 23
–18.0	00, 20, 3A

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–18.5	00, 1E, 6D
–19.0	00, 1C, B9
–19.5	00, 1B, 1E
–20.0	00, 19, 9A
–20.5	00, 18, 2B
–21.0	00, 16, D1
–21.5	00, 15, 8A
–22.0	00, 14, 56
–22.5	00, 13, 33
–23.0	00, 12, 20
–23.5	00, 11, 1C
–24.0	00, 10, 27
–24.5	00, 0F, 40
–25.0	00, 0E, 65
–25.5	00, 0D, 97
–26.0	00, 0C, D5
–26.5	00, 0C, 1D
–27.0	00, 0B, 6F
–27.5	00, 0A, CC
–28.0	00, 0A, 31
–28.5	00, 09, 9F
–29.0	00, 09, 15
–29.5	00, 08, 93
–30.0	00, 08, 18
–30.5	00, 07, A5
–31.0	00, 07, 37
–31.5	00, 06, D0
–32.0	00, 06, 6E
–32.5	00, 06, 12
–33.0	00, 05, BB
–33.5	00, 05, 69
–34.0	00, 05, 1C
–34.5	00, 04, D2
–35.0	00, 04, 8D
–35.5	00, 04, 4C
–36.0	00, 04, 0F
–36.5	00, 03, D5

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–37.0	00, 03, 9E
–37.5	00, 03, 6A
–38.0	00, 03, 39
–38.5	00, 03, 0B
–39.0	00, 02, DF
–39.5	00, 02, B6
–40.0	00, 02, 8F
–40.5	00, 02, 6B
–41.0	00, 02, 48
–41.5	00, 02, 27
–42.0	00, 02, 09
–42.5	00, 01, EB
–43.0	00, 01, D0
–43.5	00, 01, B6
–44.0	00, 01, 9E
–44.5	00, 01, 86
–45.0	00, 01, 71
–45.5	00, 01, 5C
–46.0	00, 01, 48
–46.5	00, 01, 36
–47.0	00, 01, 25
–47.5	00, 01, 14
–48.0	00, 01, 05
–48.5	00, 00, F6
–49.0	00, 00, E9
–49.5	00, 00, DC
–50.0	00, 00, CF
–50.5	00, 00, C4
–51.0	00, 00, B9
–51.5	00, 00, AE
–52.0	00, 00, A5
–52.5	00, 00, 9B
–53.0	00, 00, 93
–53.5	00, 00, 8B
–54.0	00, 00, 83
–54.5	00, 00, 7B
–55.0	00, 00, 75

Table A–6. Volume Gain Values
[The gain error is less than 0.12 dB (excluding mute)] (Continued)

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–55.5	00, 00, 6E
–56.0	00, 00, 68
–56.5	00, 00, 62
–57.0	00, 00, 5D
–57.5	00, 00, 57
–58.0	00, 00, 53
–58.5	00, 00, 4E
–59.0	00, 00, 4A

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–59.5	00, 00, 45
–60.0	00, 00, 42
–60.5	00, 00, 3E
–61.0	00, 00, 3A
–61.5	00, 00, 37
–62.0	00, 00, 34
–62.5	00, 00, 31
–63.0	00, 00, 2E

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–63.5	00, 00, 2C
–64.0	00, 00, 29
–64.5	00, 00, 27
–65.0	00, 00, 25
–65.5	00, 00, 23
–66.0	00, 00, 21
–66.5	00, 00, 1F
–67.0	00, 00, 1D

GAIN (dB)	VOLUME V(23–16), V(15–8), V(7–0)
–67.5	00, 00, 1C
–68.0	00, 00, 1A
–68.5	00, 00, 19
–69.0	00, 00, 17
–69.5	00, 00, 16
–70.0	00, 00, 15
Mute	00, 00, 00

Table A–7. Treble Control Register
(Both left and right channel will be given the same treble gain setting)

Gain (dB)	T(7–0) (hex)
18.0	0x01
17.5	0x09
17.0	0x10
16.5	0x16
16.0	0x1C
15.5	0x22
15.0	0x28
14.5	0x2D
14.0	0x32
13.5	0x36
13.0	0x3A
12.5	0x3E
12.0	0x42
11.5	0x45
11.0	0x49
10.5	0x4C
10.0	0x4F
9.5	0x52
9.0	0x55

Gain (dB)	T(7–0) (hex)
8.5	0x57
8.0	0x5A
7.5	0x5C
7.0	0x5E
6.5	0x60
6.0	0x62
5.5	0x63
5.0	0x65
4.5	0x66
4.0	0x68
3.5	0x69
3.0	0x6B
2.5	0x6C
2.0	0x6D
1.5	0x6E
1.0	0x70
0.5	0x71
0.0	0x72

Gain (dB)	T(7–0) (hex)
–0.5	0x73
–1.0	0x74
–1.5	0x75
–2.0	0x76
–2.5	0x77
–3.0	0x78
–3.5	0x79
–4.0	0x7A
–4.5	0x7B
–5.0	0x7C
–5.5	0x7D
–6.0	0x7E
–6.5	0x7F
–7.0	0x80
–7.5	0x81
–8.0	0x82
–8.5	0x83
–9.0	0x84
–9.5	0x85

Gain (dB)	T(7–0) (hex)
–10.0	0x86
–10.5	0x87
–11.0	0x88
–11.5	0x89
–12.0	0x8A
–12.5	0x8B
–13.0	0x8C
–13.5	0x8D
–14.0	0x8E
–14.5	0x8F
–15.0	0x90
–15.5	0x91
–16.0	0x92
–16.5	0x93
–17.0	0x94
–17.5	0x95
–18.0	0x96

Table A–8. Bass Control Register
(Both left and right channel will be given the same bass setting)

Gain (dB)	B(7–0) (hex)
18.0	0x01
17.5	0x03
17.0	0x06
16.5	0x08
16.0	0x0A
15.5	0x0B
15.0	0x0D
14.5	0x0F
14.0	0x10
13.5	0x12
13.0	0x13
12.5	0x14
12.0	0x16
11.5	0x17
11.0	0x18
10.5	0x19
10.0	0x1C
9.5	0x1F
9.0	0x21

Gain (dB)	B(7–0) (hex)
8.5	0x23
8.0	0x25
7.5	0x26
7.0	0x28
6.5	0x29
6.0	0x2B
5.5	0x2C
5.0	0x2E
4.5	0x30
4.0	0x31
3.5	0x33
3.0	0x35
2.5	0x36
2.0	0x38
1.5	0x39
1.0	0x3B
0.5	0x3C
0.0	0x3E

Gain (dB)	B(7–0) (hex)
–0.5	0x40
–1.0	0x42
–1.5	0x44
–2.0	0x46
–2.5	0x49
–3.0	0x4B
–3.5	0x4D
–4.0	0x4F
–4.5	0x51
–5.0	0x53
–5.5	0x54
–6.0	0x55
–6.5	0x56
–7.0	0x58
–7.5	0x59
–8.0	0x5A
–8.5	0x5C
–9.0	0x5D

Gain (dB)	B(7–0) (hex)
–9.5	0x5F
–10.0	0x61
–10.5	0x64
–11.0	0x66
–11.5	0x69
–12.0	0x6B
–12.5	0x6D
–13.0	0x6E
–13.5	0x70
–14.0	0x72
–14.5	0x74
–15.0	0x76
–15.5	0x78
–16.0	0x7A
–16.5	0x7D
–17.0	0x7F
–17.5	0x82
–18.0	0x86

Table A–9. Mixer1 and Mixer2 Gain Values
[The gain error is less than 0.12 dB (excluding mute)]

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
18.0	7F, 17, AF
17.5	77, FB, AA
17.0	71, 45, 75
16.5	6A, EF, 5D
16.0	64, F4, 03
15.5	5F, 4E, 52
15.0	59, F9, 80
14.5	54, F1, 06
14.0	50, 30, A1
13.5	4B, B4, 46
13.0	47, 78, 28
12.5	43, 78, B0
12.0	3F, B2, 78
11.5	3C, 22, 4C

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
11.0	38, C5, 28
10.5	35, 98, 2F
10.0	32, 98, B0
9.5	2F, C4, 20
9.0	2D, 18, 18
8.5	2A, 92, 54
8.0	28, 30, AF
7.5	25, F1, 25
7.0	23, D1, CD
6.5	21, D0, D9
6.0	1F, EC, 98
5.5	1E, 23, 6D
5.0	1C, 73, D5
4.5	1A, DC, 61

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
4.0	19, 5B, B8
3.5	17, F0, 94
3.0	16, 99, C0
2.5	15, 56, 1A
2.0	14, 24, 8E
1.5	13, 04, 1A
1.0	11, F3, C9
0.5	10, F2, B4
0.0	10, 00, 00
–0.5	0F, 1A, DF
–1.0	0E, 42, 90
–1.5	0D, 76, 5A
–2.0	0C, B5, 91
–2.5	0B, FF, 91

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
–3.0	0B, 53, BE
–3.5	0A, B1, 89
–4.0	0A, 18, 66
–4.5	09, 87, D5
–5.0	08, FF, 59
–5.5	08, 7E, 80
–6.0	08, 04, DC
–6.5	07, 92, 07
–7.0	07, 25, 9D
–7.5	06, BF, 44
–8.0	06, 5E, A5
–8.5	06, 03, 6E
–9.0	05, AD, 50
–9.5	05, 5C, 04

Table A–9. Example Mixer1 and Mixer2 Gain Values
[The gain error is less than 0.12 dB (excluding mute)] (Continued)

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
–10.0	05, 0F, 44
–10.5	04, C6, D0
–11.0	04, 82, 68
–11.5	04, 41, D5
–12.0	04, 04, DE
–12.5	03, CB, 50
–13.0	03, 94, FA
–13.5	03, 61, AF
–14.0	03, 31, 42
–14.5	03, 03, 8A
–15.0	02, D8, 62
–15.5	02, AF, A3
–16.0	02, 89, 2C
–16.5	02, 64, DB
–17.0	02, 42, 93
–17.5	02, 22, 35
–18.0	02, 03, A7
–18.5	01, E6, CF
–19.0	01, CB, 94
–19.5	01, B1, DE
–20.0	01, 99, 99
–20.5	01, 82, AF
–21.0	01, 6D, 0E
–21.5	01, 58, A2
–22.0	01, 45, 5B
–22.5	01, 33, 28
–23.0	01, 21, F9
–23.5	01, 11, C0
–24.0	01, 02, 70
–24.5	00, F3, FB

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
–25.0	00, E6, 55
–25.5	00, D9, 73
–26.0	00, CD, 49
–26.5	00, C1, CD
–27.0	00, B6, F6
–27.5	00, AC, BA
–28.0	00, A3, 10
–28.5	00, 99, F1
–29.0	00, 91, 54
–29.5	00, 89, 33
–30.0	00, 81, 86
–30.5	00, 7A, 48
–31.0	00, 73, 70
–31.5	00, 6C, FB
–32.0	00, 66, E3
–32.5	00, 61, 21
–33.0	00, 5B, B2
–33.5	00, 56, 91
–34.0	00, 51, B9
–34.5	00, 4D, 27
–35.0	00, 48, D6
–35.5	00, 44, C3
–36.0	00, 40, EA
–36.5	00, 3D, 49
–37.0	00, 39, DB
–37.5	00, 36, 9E
–38.0	00, 33, 90
–38.5	00, 30, AE
–39.0	00, 2D, F5
–39.5	00, 2B, 63

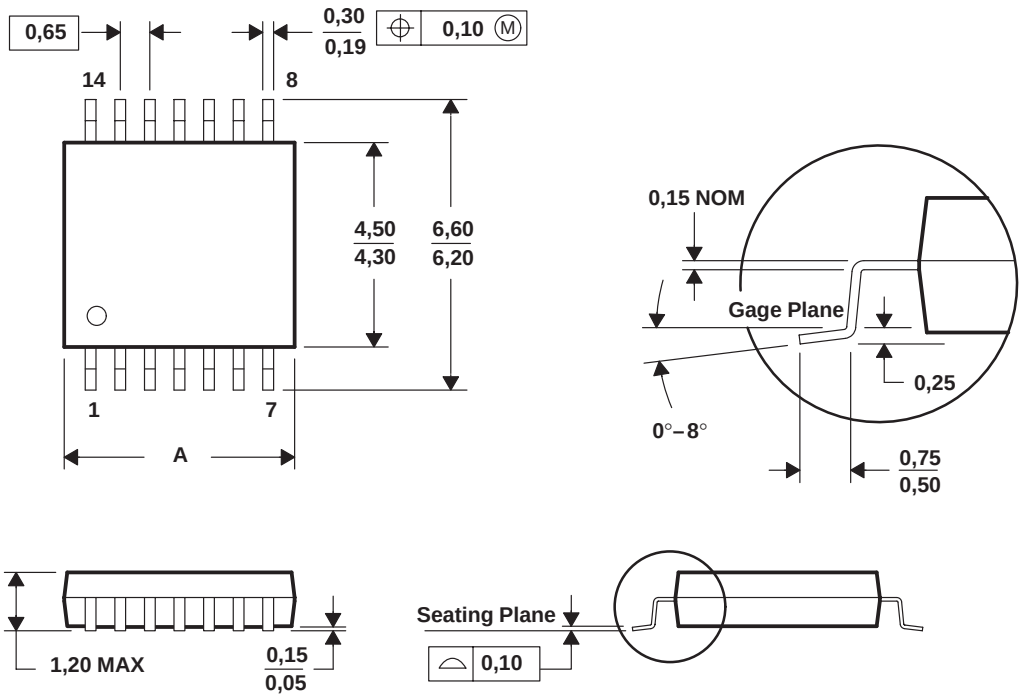
Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
–40.0	00, 28, F5
–40.5	00, 26, AB
–41.0	00, 24, 81
–41.5	00, 22, 76
–42.0	00, 20, 89
–42.5	00, 1E, B7
–43.0	00, 1C, FF
–43.5	00, 1B, 60
–44.0	00, 19, D8
–44.5	00, 18, 65
–45.0	00, 17, 08
–45.5	00, 15, BE
–46.0	00, 14, 87
–46.5	00, 13, 61
–47.0	00, 12, 4B
–47.5	00, 11, 45
–48.0	00, 10, 4E
–48.5	00, 0F, 64
–49.0	00, 0E, 88
–49.5	00, 0D, B8
–50.0	00, 0C, F3
–50.5	00, 0C, 3A
–51.0	00, 0B, 8B
–51.5	00, 0A, E5
–52.0	00, 0A, 49
–52.5	00, 09, B6
–53.0	00, 09, 2B
–53.5	00, 08, A8
–54.0	00, 08, 2C
–54.5	00, 07, B7
–55.0	00, 07, 48

Gain (dB)	Gain S(23–16), S(15–8), S(7–0)
–55.5	00, 06, E0
–56.0	00, 06, 7D
–56.5	00, 06, 20
–57.0	00, 05, C9
–57.5	00, 05, 76
–58.0	00, 05, 28
–58.5	00, 04, DE
–59.0	00, 04, 98
–59.5	00, 04, 56
–60.0	00, 04, 18
–60.5	00, 03, DD
–61.0	00, 03, A6
–61.5	00, 03, 72
–62.0	00, 03, 40
–62.5	00, 03, 12
–63.0	00, 02, E6
–63.5	00, 02, BC
–64.0	00, 02, 95
–64.5	00, 02, 70
–65.0	00, 02, 4D
–65.5	00, 02, 2C
–66.0	00, 02, 0D
–66.5	00, 01, F0
–67.0	00, 01, D4
–67.5	00, 01, BA
–68.0	00, 01, A1
–68.5	00, 01, 8A
–69.0	00, 01, 74
–69.5	00, 01, 5F
–70.0	00, 01, 4B
Mute	00, 00, 00

Appendix B
Mechanical Data

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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