Winbond
Integrated Media Reader
W83L519D

W83L519D

Datasheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		02/Jul.	1.0	1.0	1st Release
2					
3					
4					
5					
6					
7					
8					

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1 GENERAL DESCRIPTION

W83L519D is Winbond's innovative solution to a new class of storage devices for IA Noetebook, Desktop PC and PC system-related products. It incorporates a security Application: Smart Card Interface and two most promising compact storage interfaces: Memory Stick interface, and Secure Digital Memory Card interface in IT era.

To cater boundless IT implementation possibilities, W83L519D can be configured to interface with host through ISA bus. Base on the ISA interface, one Smart Card Interface port and an optional Memory Stick/SD memory Interface ports are provided. The kind of versatility allows user to design very cost-effective products in a very flexible way.

The whole chip of W83L519D operates at voltage level of 3.3 V except Smart Card Interface port's I/O pins and ISA bus interface that are at 5 V to be compatible with mainstream Smart Card implementations. Advanced power management feature further optimizes power consumption whether in operation or in power down mode.

W83L519D comes as a 48-pin LQFP streamline package. Combining with powerful functions, effective power management, and versatile configurability, this integrated media reader offers a perfect approach for design of storage device of IT products.

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2 FUNCTIONS

2.1 General

- Support ISA bus
- Programmable configuration settings
- 48 MHz crystal inputs

2.2 Smart Card Interface

- ISO-7816 compliant
- PC/SC T=0, T=1 compliant
- 16-byte transmitter FIFO and 16-byte receiver FIFO
- FIFO threshold interrupt to optimize system performance
- Programmable transmission clock frequency
- Versatile baud rate configuration
- UART-like register file structure

2.3 Memory Stick Interface

- Memory Stick Standard Format Specifications ver. 1.3 compliant
- Support interrupt polling transmission
- Support FIFO threshold interrupt to optimize system performance
- Automatic clock halt to prevent underrun/overrun
- 16 MHz interface clock

2.4 SD Memory Card Interface

- SD Memory Card Specifications: Part 1 PHYSICAL LAYER SPECIFICATION Version 1.0 Compliant
- Support interrupt polling transmission
- Support FIFO threshold interrupt to leverage system performance
- 24 MHz interface clock

2.5 Package

- 48-pin LQFP

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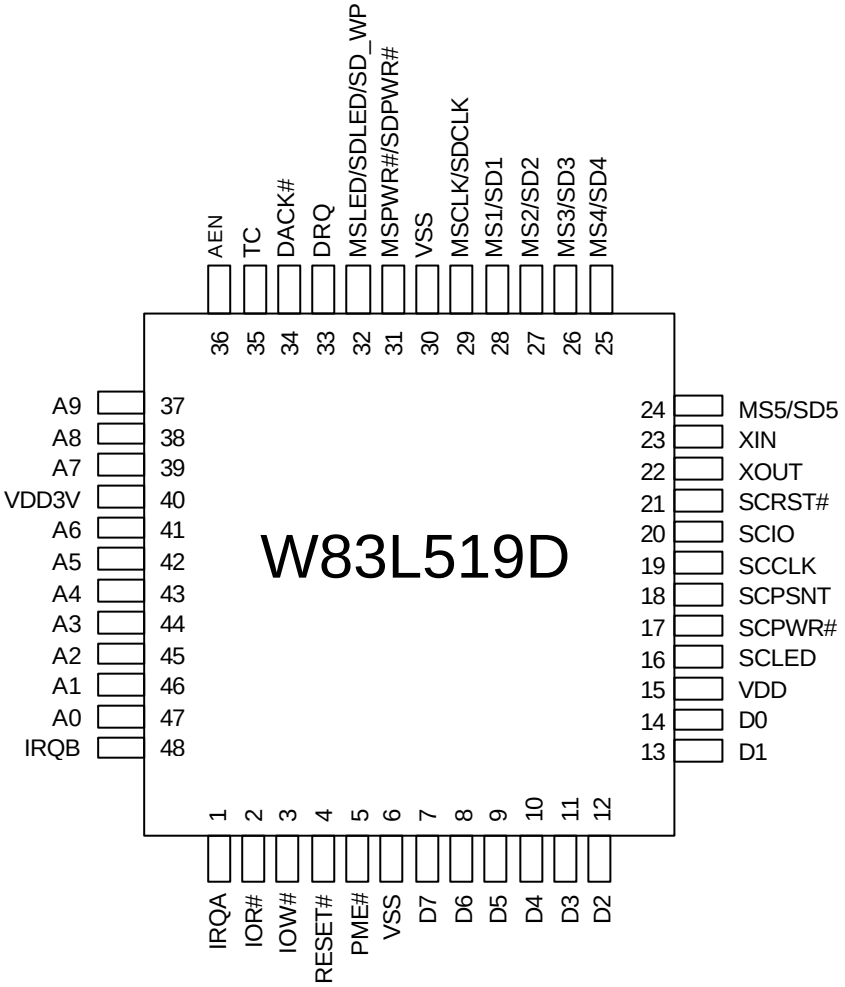
3 PIN CONFIGURATION



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4 PIN DESCRIPTION

Note:

IN_{tp3} - 3.3V TTL level input pin

IN_{ts} - 5V TTL level Schmitt-trigger input pin

IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin

I/O_{12t} - 5V TTL level bi-directional pin with 12 mA drive-sink capability

I/O_{24t} - 5V TTL level bi-directional pin with 24 mA drive-sink capability

I/O_{24tp3} - 3.3V TTL level bi-directional pin with 24 mA drive-sink capability

O_{2} - 5V output pin with 2 mA drive-sink capability

O_{12} - 5V output pin with 12 mA drive-sink capability

O_{24p3} - 3.3V output pin with 24 mA drive-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

4.1 Bus Interface

SYMBOL	PIN	I/O	FUNCTION
RESET#	4	IN_{tsp3}	Active-low system reset signal.
IOW#	3	IN_{tsp3}	ISA configuration: Active-low signal to enable ISA I/O write accesses.
IOR#	2	IN_{tsp3}	ISA configuration: Active-low signal to enable ISA I/O read accesses.
IRQA	1	O_{24p3}	ISA configuration: Interrupt output of Smart Card interface port.
IRQB	48	O_{24p3}	ISA configuration: Interrupt output of Memory Stick/SD Memory Card interface port.
A0	47	IN_{tp3}	ISA configuration: Address bit 0.
A1	46	IN_{tp3}	ISA configuration: Address bit 1.
A2	45	IN_{tp3}	ISA configuration: Address bit 2.
A3	44	IN_{tp3}	ISA configuration: Address bit 3.
A4	43	IN_{tp3}	ISA configuration: Address bit 4.
A5	42	IN_{tp3}	ISA configuration: Address bit 5.
A6	41	IN_{tp3}	ISA configuration: Address bit 6.
A7	39	IN_{tp3}	ISA configuration: Address bit 7.
A8	38	IN_{tp3}	ISA configuration: Address bit 8.
A9	37	IN_{tp3}	ISA configuration: Address bit 9.

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4.1 Bus Interface (continued.)

SYMBOL	PIN	I/O	FUNCTION
AEN	36	IN_{tp3}	ISA configuration: Active-low I/O address enable signal. It is pulled high in DMA accesses.
TC	35	IN_{tp3}	ISA configuration: This pin signals termination of DMA accesses.
DACK#	34	IN_{tp3}	ISA configuration: DMA acknowledge. This active-low signal validates DMA accesses.
DRQ	33	O_{24p3}	ISA configuration: DMA request signal.
D7	7	I/O_{12t}	ISA configuration: System data bit 7.
D6	8	I/O_{12t}	ISA configuration: System data bit 6.
D5	9	I/O_{12t}	ISA configuration: System data bit 5.
D4	10	I/O_{12t}	ISA configuration: System data bit 4.
D3	11	I/O_{12t}	ISA configuration: System data bit 3.
D2	12	I/O_{12t}	ISA configuration: System data bit 2.
D1	13	I/O_{24t}	ISA configuration: System data bit 1.
D0	14	I/O_{24t}	ISA configuration: System data bit 0.
PME#	5	OD_{12}	Active-low PME event.

4.2 Smart Card Interface Pins

SYMBOL	PIN	I/O	FUNCTION
SCLED	16	O_{24}	This pin outputs an oscillating clock signal of various frequencies depending on traffic of primary Smart Card interface.
SCPWR#	17	O_{24}	Primary Smart Card interface power control signal.
SCPSNT	18	IN_{ts}	Primary Smart Card interface card present detection Schmitt-trigger input.
SCCLK	19	O_2	Primary Smart Card interface clock output.
SCIO	20	I/O_{12t}	Primary Smart Card interface data I/O channel.
SCRST#	21	O_{12}	Primary Smart Card interface reset output.

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4.3 Memory Stick Interface/SD Memory Interface Pins

SYMBOL	PIN	I/O	FUNCTION
MSLED	32	O_{24p3}	MS/SD select = 0, MS function - This pin outputs an oscillating clock signal of various frequencies depending on traffic of primary Memory Stick interface;
SDLED		O_{24p3}	MS/SD select = 1, SD function - This pin outputs an oscillating clock signal of various frequencies depending on traffic of primary SD memory card interface.
SD_WP		IN_{ts}	MS/SD select = 1, SD function – Write protect input signal.
MSPWR#	31	O_{24p3}	MS/SD select = 0, MS function - This pin is power control signal for primary Memory Stick interface;
SDPWR#		O_{24p3}	MS/SD select = 1, SD function - This pin is power control signal for primary SD memory card interface.
MSCLK	29	O_{24p3}	MS/SD select = 0, MS function - This pin is SCLK for primary Memory Stick interface;
SDCLK		O_{24p3}	MS/SD select = 1, SD function - This pin is CLK for primary SD memory card interface.
MS1	28	O_{24p3}	MS/SD select = 0, MS function - This pin is MS1 for primary Memory Stick interface;
SD1		I/O_{24tp3}	MS/SD select = 1, SD function - This pin is SD1 for primary SD memory card interface.
MS2	27	I/O_{24tp3}	MS/SD select = 0, MS function - This pin is MS2 for primary Memory Stick interface;
SD2		I/O_{24tp3}	MS/SD select = 1, SD function - This pin is SD2 for primary SD memory card interface.
MS3	26	---	MS/SD select = 0, MS function - This pin is MS3 for primary Memory Stick interface;
SD3		I/O_{24tp3}	MS/SD select = 1, SD function - This pin is SD3 for primary SD memory card interface.
MS4	25	IN_{tsp3}	MS/SD select = 0, MS function - This pin is MS4 for primary Memory Stick interface;
SD4		I/O_{24tp3}	MS/SD select = 1, SD function - This pin is SD4 for primary SD memory card interface.

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4.3 Memory Stick Interface/SD Memory Interface Pins (Continued.)

SYMBOL	PIN	I/O	FUNCTION
MS5	24	---	MS/SD select = 0, MS function - This pin is MS5 for primary Memory Stick interface;
SD5		I/O_{24tp3}	MS/SD select = 1, SD function - This pin is SD5 for primary SD memory card interface.

4.4 Crystal and Power Pins

SYMBOL	PIN	FUNCTION
XOUT, XIN	22, 23	Connected to a 48 MHz crystal and function as the working clock for all the media reader interfaces.
VDD3V	40	+3.3V power supply for host interface, MSI/SDI interfaces, and internal core.
VDD	15	+5V power supply for Smart Card interface I/O pins.
VSS	6, 30	Ground.

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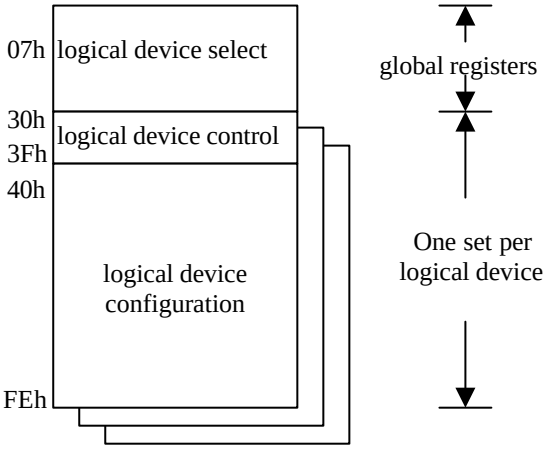
5 CONFIGURATION REGISTER

5.1 Plug and Play Configuration

W83L519D implement compatible PNP protocol to access configuration registers for setting up different types of configurations. There are three Logical Devices (Logical Device 0 to Logical Device 2) in W83L518D/W83L519D which correspond to three major functions: Smart Card Interface (logical device 0), Memory Stick Interface/SD memory Interface (logical device 1), GPIO (logical device 2). Each Logical Device has its own configuration registers (CR30 and above). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7 first.



5.2 Compatible PnP

5.2.1 Extended Function Register

W83L518D/W83L519D provide two methods to enter Extended Function mode (compatible PnP) and access configuration registers dependent on value of HEFRAS (bit 6 of CR26) as follows:

HEFRAS	address and value
0	write 83h to I/O address 2Eh twice
1	write 83h to I/O address 4Eh twice

In Compatible PnP, a specific value (83h) must be written twice to the Extended Function Enable Register (EFER at I/O address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Function Index Register (EFIR, I/O address at 2Eh or 4Eh which is the same as EFER) to identify which configuration register is to be accessed. User can then access the addressed configuration register through the Extended Function Data Register (EFDR, I/O address at 2Fh or 4Fh).

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After programming of the configuration register is completed, another specific value (AAh) should be written to EFER to leave Extended Function mode to prevent inadvertent accesses to those configuration registers. User may write a "1" to bit 5 of CR26 (LOCKREG) to prevent configuration registers from accidental accesses.

5.2.2 Extended Functions Enable Register (EFER)

After a power-on reset, W83L518D/W83L519D enters the default operation mode. A specific value must be programmed into the Extended Function Enable Register (EFER) so that configuration registers can be accessed. On a PC/AT system, its I/O address is 2Eh or 4Eh (as described in previous section).

5.2.3 Extended Function Index Register (EFIR), Extended Function Data Register (EFDR)

After entering Extended Function mode, Extended Function Index Register (EFIR) must be written with an index value (02h, 07h-FEh) to specify which configuration register is to be accessed through Extended Function Data Register (EFDR). EFIR is a write-only register at I/O address 2Eh or 4Eh (as described in section 6.2.1) on a PC/AT system and EFDR is a read/write register at I/O address 2Fh or 4Fh.

5.3 Configuration Sequence

To program configuration registers, specific configuration sequence must be followed:

(1) Write 83h to EFER twice to enter Extended Function mode.

(2) Select logical device select register by writing 07h to EFIR.

(3) Select logical device by writing a value to EFDR.

(4) Select control/configuration register by writing its index to EFIR.

(5) Access selected control/configuration register through EFDR.

(6) Repeat step 4 ~ 5 as needed.

(7) Leave Extended Function mode by writing AAh to EFER.

Step 2 and step 3 are not necessary for accessing global register (index 00h to 2Fh).

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5.3.1 Software programming example

The following example is written in Intel 8086 assembly language. EFER and EFIR are assumed to be at 2Eh, and EFDR is at 2Fh. Use 4Eh/4Fh instead of 2Eh/2Fh if HEFRAS (bit 6 of CR26) is set.

```
;--------------------------------------------------------------------------------
; Enter Extended Function mode, interruptible double-write    |
;--------------------------------------------------------------------------------
MOV         DX, 2Eh
MOV         AL, 83h
OUT         DX, AL
OUT         DX, AL
;--------------------------------------------------------------------------
; Configure logical device 1, configuration register CRF0   |
;--------------------------------------------------------------------------
MOV         DX, 2Eh
MOV         AL, 07h
OUT         DX, AL              ; point to Logical Device Number Reg.
MOV         DX, 2Fh
MOV         AL, 01h
OUT         DX, AL              ; select logical device 1
;
MOV DX, 2Eh
MOV         AL, F0H
OUT         DX, AL              ; select CRF0
MOV         DX, 2Fh
MOV         AL, 3Ch
OUT         DX, AL              ; update CRF0 with value 3CH
;---------------------------------------
; Exit extended function mode     |
;---------------------------------------
MOV         DX, 2Eh
MOV         AL, AAh
OUT         DX, AL
```

5.4 Global Registers

CR02 (Default 00h, write only)

Bit [7:1]: Reserved.

Bit 0: SWRST

= 0 Normal operation.

= 1 Software reset.

CR07 (Default 00h)

Bit [7:0]: Logical Device Number.

CR20 (read only)

Bit [7:0]: Device ID number (higher byte).

= 71h

CR21 (read only)

Bit [7:0]: Device ID number (lower byte)

= 2Xh

CR22 (Default 80h)

Bit 7: SCPWD

= 0 Power down Smart Card interface.

= 1 No Power down.

Bit 6: MSPWD

= 0 Power down Memory Stick interface.

= 1 No Power down.

Bit 5: SDPWD

= 0 Power down SD memory card interface.

= 1 No Power down.

Bit [4:0]: Reserved.

CR23 (Default 00h)

Bit 7: PME_EN. Power management event enable bit.

= 0 PME_L function is disabled.

= 1 Enable to issue a low pulse on PME_L when a power management event occurs.

Bit 6: MSPME_EN. Memory Stick interface power management event enable bit.

= 0 Memory Stick interface power management event is disabled.

= 1 Enable Memory Stick interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit 5: SDPME_EN. SD memory card interface power management event enable bit.

= 0 SD memory card interface power management event is disabled.

= 1 Enable SD memory card interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit 4: SCPME_EN. Smart Card interface power management event enable bit.

= 0 Smart Card interface power management event is disabled.

= 1 Enable Smart Card interface power management event to issue a low pulse on PME_L when PME_EN is also enabled.

Bit [3:0]: Reserved.

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CR24 (Default 00h)

Bit 7: Reserved.

Bit 6: MSPME_STS. Memory Stick interface power management event status bit.

= 0 No Memory Stick interface power management event occurs.

= 1 Memory Stick interface power management event occurs.

Bit 5: SDPME_STS. SD memory card interface power management event status bit.

= 0 No SD memory card interface power management event occurs.

= 1 SD memory card interface power management event occurs.

Bit 4: SCPME_STS. Smart Card interface power management event status bit.

= 0 No Smart Card interface power management event occurs.

= 1 No Smart Card interface power management event occurs.

Bit [3:0]: Reserved.

CR26 (Default 00h)

Bit 7: Reserved

Bit 6: HEFRAS, Extended Function Register Address Select.

= 0 Extended Function Registers are at 2Eh/2Fh.

= 1 Extended Function Registers are at 4Eh/4Fh.

Bit 5: LOCKREG

= 0 Enable accesses of Configuration Registers.

= 1 Disable accesses of Configuration Registers.

Bit [4:0]: Reserved

5.5 Logical Device 0 (Smart Card Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0 Logical device is inactive.

= 1 Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Smart Card interface.

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CRF0 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: SCPSNT_POL (Smart Card PreSeNT POLarity). SCPSNT polarity bit.

= 0 SCPSNT is active high.

= 1 SCPSNT is active low.

5.6 Logical Device 1 (Memory Stick Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0: Logical device is inactive.

= 1: Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select MSI base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for MSI.

CR74 (Default 0x04)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select DRQ resource for MSI.

5.7 Logical Device 2 (GPIO)

CR30 (Default 00h)

Bit [7:3]: Reserved.

Bit 2: Individual disable/enable bit for GPIO2.

= 0 GPIO2 is disabled if bit 0 is also "0".

= 1 GPIO2 is enabled.

Bit 1: Individual disable/enable bit for GPIO1.

= 0 GPIO1 is disabled if bit 0 is also "0".

= 1 GPIO1 is enabled.

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Bit 0: Logical device disable/enable bit.

= 0 GPIO1 and GPIO2 are disabled/enabled dependent on bit 1 and 2 respectively.

= 1 Activates GPIO1 and GPIO2.

CR60, CR61 (Both default 00h)

Base address configuration registers: programmable at addresses from 0100h to 0FF8h on 4-byte boundary. Base address + 0 and base address + 1 are for GPIO1 as direction register and data register respectively while base address + 2 and base address + 3 are for GPIO2 as direction register and data register respectively.

CRF0 (GP10 ~ GP17 direction register. Default FFh)

When set to "1", respective GPIO port is programmed as an input port. When set to a "0", respective GPIO port is programmed as an output port.

CRF1 (GP10 ~ GP17 data register. Default 00h)

If a port is programmed to be an output port, its respective bit can be read/written and output to respective pin. If a port is programmed to be an input port, its respective bit reflects what is on respective pin.

CRF2 (GP10 ~ GP17 inversion register. Default 00h)

When set to "1", respective incoming/outgoing port value is inverted. When set to "0", respective incoming/outgoing port value is the same as in data register.

CRF3 (GP20 ~ GP27 direction register. Default FFh)

When set to "1", respective GPIO port is programmed as an input port. When set to a "0", respective GPIO port is programmed as an output port.

CRF4 (GP20 ~ GP27 data register. Default 00h)

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If a port is programmed to be an output port, its respective bit can be read/written and output to respective pin. If a port is programmed to be an input port, its respective bit reflects what is on respective pin.

CRF5 (GP20 ~ GP27 inversion register. Default 00h)

When set to "1", respective incoming/outgoing port value is inverted. When set to "0", respective incoming/outgoing port value is the same as in data register.

5.8 Logical Device 3 (SD Memory Interface)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: Logical device active bit.

= 0 Logical device is inactive.

= 1 Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select SD Card interface base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for SD interface.

CR74 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select DRQ resource for SD interface.

CRF0 (Default 0x01)

Bit [7:6]: Reserved.

Bit 5: Set the output value of the DATA3 pin when bit4 is setted 1.

= 0 The DATA3 pin will output low.

= 1 The DATA3 pin will output high.

Bit 4: Set the DATA3 (MS1 or MSB1) pin to output pin.

= 0 Set the DATA3 pin to bi-direction pin.

= 1 Set the DATA3 pin to output pin.

Bit 3: Reserved.

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Bit 2: Select the pole of the GP11 card-detect pin.

= 0 When detecting the low signal indicate the card is inserted and high signal indicate the card is extracted.

= 1 When detecting the high signal incicate the card is inserted and low signal indicate the card is extracted.

Bit 1: Select GP11 pin to detect card.

= 0 Don' t use the GP11 pin to detect card.

= 1 Use the GP11 (SCBPWR_L) pin to detect card.

Bit 0: Select DATA3 pin to detect card.

= 0 Don' t use the DATA3 (MS1 or MSB1) to detect card.

= 1 Use the DATA3 (MS1 or MSB1) pin to detect card.

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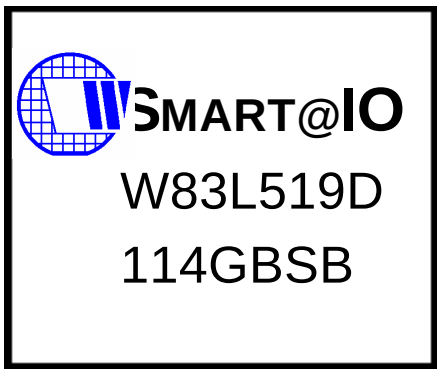
6 ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83L519D	48-pin LQFP	

7 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the SMART@IO Trademark

2nd line: The chip part number.

3rd line: Tracking code 114 G BSB

114: packages made in '01, week 14

G: assembly house ID; O means OSE, G means GR, …

BSB: IC revision

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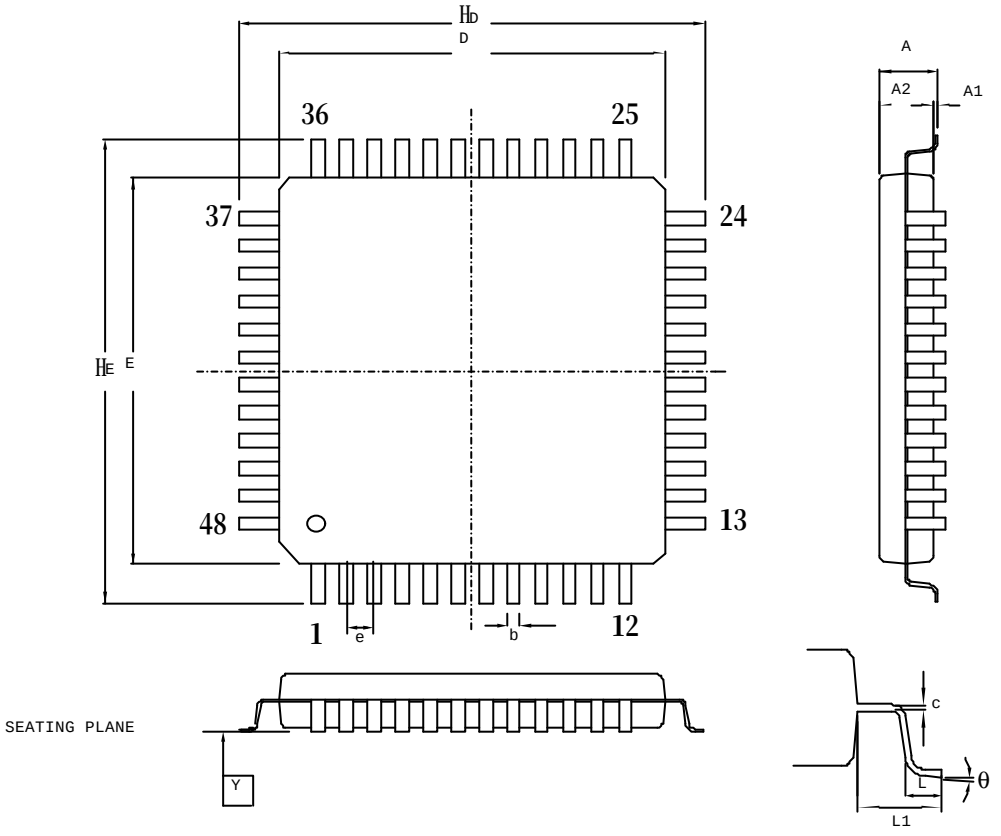
8 PACKAGE DRAWING AND DIMENSIONS

Package- 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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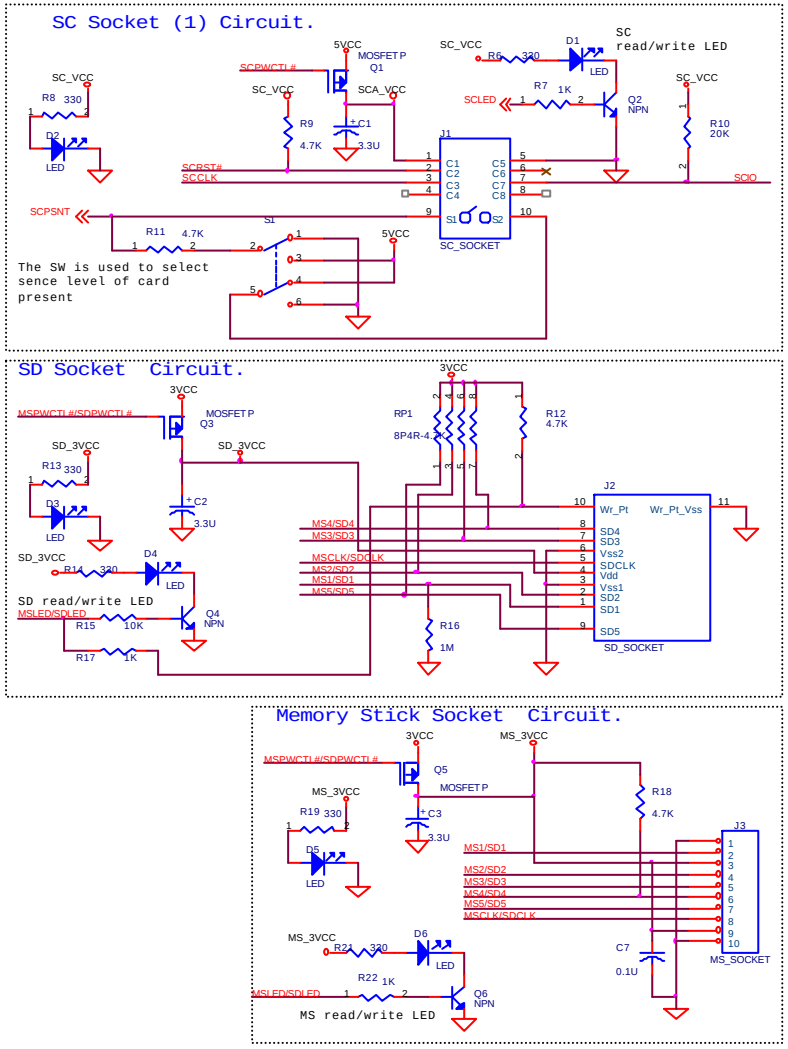
9 THE W83L519D SCHEMATIC



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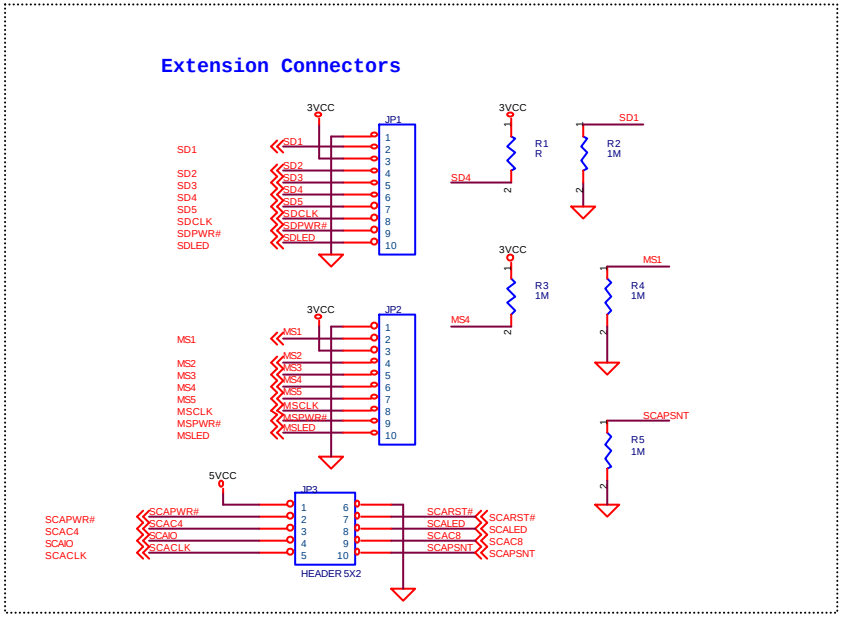
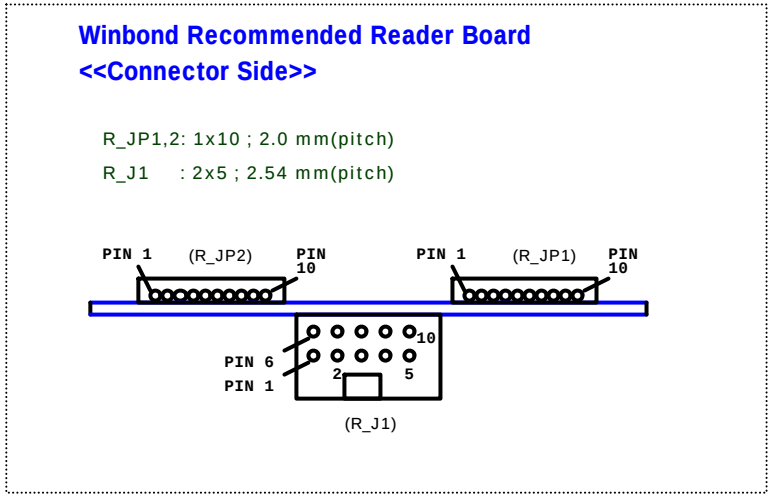
The W83L519D Schematic





Note 1: These IRQ signals (IRQA,IRQB) can tie to IRQX(IRQ3,4,...) of ISA bus or compatible ones.

Note 2: These DMA signals (DRQ,DACK#) can tie to which pair (DRQ1,DACK1#,...) of ISA bus or compatible ones.(except 16 bits DMA transaction)

Note 3: The RESET# should be connected with a low asserted signal.(active low)

Note 4: There is either function of SD and MS can be used and depeneded on the design.

Note 5: If any of SC or MS/SD function isn't intened to use, signal SCPSNT should be tied to a pull-down resitor and MS4/SD4 to a pull-high one. (recommended: 4.7K Ohm)

Note 6: The trade marks and intellectual property rights of Memory Stick belong to SONY Corporation.
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Size B	Document Number W83L519D schematic circuit	Rev 0.2
Date: Monday, February 18, 2002	Sheet 2 of 2	

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Headquarters

No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office

9F, No. 480, Rueiguang Road, Neihu District,
Taipei, 114, Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics
(North America) Corp.

2727 North First Street
San Jose, California 95134
TEL: 1-408-9436666
FAX: 1-408-9436668

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