₂ Printer Enhancement ASIC

(Preliminary)

1. General Description

The Printer Enhancement ASIC provides state-of-the-art resolution enhancement for text, line art, and photo images for all printing modes including fax. The design gives the Printer Controller designer the ability to add the Enhancement Technology into new or existing designs with minimal effort and cost. The Printer Enhancement ASIC operates on the serial video data stream to enhance the output print quality and minimize design interfacing requirement.

Operating on a typical 600 DPI engine and with 200, 300, or 600 DPI source data, the edge enhancement logic determines the additional small fractional dots to be added to fill jaggies so that effective resolution is doubled. Gray scale enhancement also operates on 600x1 bit serial data requiring no additional memory to improve gray scale rendering. An additional breakthrough feature is the ability to accept 1200 DPI source data to render 1200 DPI quality for text and gray scale on a 600 DPI engine.

A direct digital copy mode allows a Multi-Function Device to pass 8-bit scanner data directly to the printer for higher quality copying. Internal programmable look-up-tables are provided to optimize print quality for different print engines.

2. Features

- Photo Enhancement
    - 144 Gray Levels in 1-bit Mode
    - 256 Gray Levels in 8-bit Mode
- Text & Line Art Edge Enhancement:
    - Source Data (DPI) = 1/3X, 1/2X, or 1X Engine Resolution
- 1200 DPI Mode
- Fax Enhancement for 200 DPI Source Data
- Digital Copy Modes
- Multiple Print Engine Support
    - 300 - 600 DPI
- Internal Precision Modulator

3 Image Enhancement Module Functions

3.1 Setup

Setup requirements consist of programming the control registers and downloading LUT (look_up_table) information into LUT memory. All internal register and memory locations can be read by the host CPU to check status and/or hardware integrity. In addition to the LUT memory and control registers, the Line Store memory can be written and read for testing. The memory map for the control registers and internal memories are:

Memory Map	From PA[9:0]	To PA[9:0]
Internal LUT (512 x 8)	000	1FF
Control Registers (18 x 8)	200	2FF
Line Store Memory (8K x 16)	UpperLineStoreAddress[3:0] = 0, PA[8:0] = 000	UpperLineStoreAddress[3:0] = F, PA[8:0] = 1FF

POWER-UP CONDITIONS:

Control Registers are powered up in their inactive state. In order to make any mode operational, specific values must be written to the control registers as well as the LUT's, which will be powered up in a random state.

LOOK-UP TABLES:

Look-up tables are required to be loaded by the CPU. Final tables will be provided after characterization on a sampling of representative engines.

LINE MEMORY SIZE:

Line store memory is organized as 8K words. This is segmented by the hardware architecture according to what operating mode is selected.

MODE	BUFFERS
600x600x1	8
300x300x1	16
200x200x1	16
200x100x1	16
1200x1200x1	4
600x600x8	NOT BUFFERED
300x300x8	1

3.2 Margin Offset Control:

Control register **C** contains the 11 bit register that sets the left-hand margin position of the image. The count will reflect the amount of 600dpi positions (1/600) from the selected edge of the beam detect (BD) signal, regardless of the mode selected.

3.3 Vertical Margin Control

The top of page detection is controlled by fsync_en (frame synch enable - control register **A**, bit 10) and frame sync, (fsynch). Fsync_en is set by software to begin a page (lsynch s will be ignored until the fsynch signal is received). When fsync_en is high we wait for fsynch to go high and then lsynch clocks will begin counting the vertical margin counter. When the vertical margin counter equals the vertical margin top register, (control register **E**) data transfer will begin. The vertical margin counter will continue to increment on each hysnc and when it reaches the value set in the vertical margin bottom register, (control register **F**) data

transfer will terminate for the remainder of the page. The CPU is required to reset fsync_en after it has moved the all of the line data into the PRINTER ENHANCEMENT ASIC chip and allowed it to image that data. (one, two, or three additional lines depending on mode). The CPU will then set fsync_en again to prepare the fsynch logic for the next page synch signal, fsynch.

3.4 Input Ports
The data input is parallel, eight bit. Data is transferred into the design on the rising edge of the parallel video clock. The first clock after the hysnc signal will transfer the first eignt bits of data into the design.

3.5 Look-Up Table Memory (LUT):
To Load or Read the LUT memory the following bit in control register **A** must be set:

CPU2InternalLUT = Load LUT Memory (512x8)

Subsequent reading or writing to memory locations 0000-01FF will address the LUT memory, Data Bit 0 = LUT Bit 0. *What are LUT' s for?* Look-up tables translate the fixed image values that are affected by engine linearity, temperature, aging, environmental, toner exhaustion, and other variables as well as features such as toner saver, paper type, type of input, etc. into values that will reproduce the highest quality image possible. The number of variables that influence the printed image are numerous and in order to correctly image the job these variables have to be compensated for. This is the job of the LUT memory..

3.6 OPERATING MODES

3.6.1 1200x1200x1
1200 Mode is selected by programming control register **A** bits [3:0] with a 1010. Source data must be in the two line format that can be used. The two line format requires that two lines of 1200 data must be transferred for each hysnc received by the design. The design will transfer two lines of sequential 1200 data per hysnc. The length of the lines is tracked via the line length register value (control register **D**, [11:0]) and when it reaches the programmed count it repeats the count for the second line. The CPU must program the line length (control register **D**) with the length of a single line of 1200 data into the Image Enhancement module.

To set up the PRINTER ENHANCEMENT ASIC for 1200 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	1010
Mfunction **(see table 2.0)**	[6:5}	XX
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Line Synch Width Register	[15:11}	0 - 1Fh
D: Line Length Register	[11:0]	0 - FFFh

D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.2 600x600x1

600 Mode is selected by programming control register **A**, bits [3:0]. There are four different 600x1 operating modes to choose from. 0h is selected for enhanced text only, 1h is the test mode for 0h. 2h is for enhanced text and enhanced one bit gray scale. 3h is for unenhanced text and enhanced one bit gray scale. The CPU must program the line length (Control Register **D**) of a single line of 300 data into the Winbond chip.

To set up the Winbond chip for 600 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	0h, 1h, 2, 3h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.3 300x300x1

300 Mode is selected by programming control register **A** bits [3:0]. There are two different 300x1 operating modes to choose from. 4h is selected for enhanced text only, 5h is the test mode for 4h.

To set up the PRINTER ENHANCEMENT ASIC chip for 300 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	4h, 5h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00

Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.4 200xNx1

200 Mode is selected by programming control register **A** bits [3:0]. There are four different 200x1 operating modes to choose from. 6h is selected for enhanced text only, 7h is the test mode for 6h. 8h is selected for 200x100x1 enhanced text. 9h is the test mode for 8h.

To set up the Winbond chip for 200 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	6h, 7h, 8h, 9h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.5 600x600x8

600x8 Mode is selected by programming control register **A** bits [3:0].

To set up the PRINTER ENHANCEMENT ASIC chip for 600x8 the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	Bh
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1

bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.6 300x300x8

300x8 Mode is selected by programming control register   A   bits [3:0]. The CPU must program the line length (Control Register   D) of a single line of 300 data into the Winbond chip.

To set up the Winbond chip for 300x8 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register A	BITS	VALUE
Mode	[3:0]	Ch
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register B	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

3.6.7 ONE BIT (600/300/200) TEST MODES

Test modes are different from normal one bit modes in that they bypass the Edge Enhancement Unit, (EEU). The input data is sampled just prior to the LUT memories. Selecting 600x600x1t, 600x600x1tg, 300x300x1t, 200x200x1t, or 200x100x1t one bit modes in register **A** will operate this way. The purpose of the test mode is to be able to bypass the EEU logic and

present the assembled data directly to the modulator in order to isolate faults. Output will appear exactly like the input bit map.

4. Image Enhancement Module Registers

Memory Map

	From PA[9:0]	To PA[9:0]
Internal LUT	000	1FF
Control Register	200	2FF

Control Register A (address= 201, 200)

15(MSB)	**CPU2LineStore**	Enable CPU to access line store memory
14	**Screen150**	Control bit foe 300x150 or 600x300 screen
13	**CPU2InternalLUT**	Enable CPU to access internal LUT
12	**SourceSelect 1**	00: 8-bit parallel video data in,
11	**SourceSelect 0**	11: serial video data in
10	**fsync_n**	Page start detection control bit. Must goes low after a page to reset circuit that looks for page start
9	**vidpol**	video polarity, vidpol XOR (video AND vidkill)
8	**bdedge**	line sync edge sensitivity
7	**vidkill**	Drive video kill output, 0: kill video output
6	**black**	Drive black output
5	**force**	Drive force output
4	**LineStore16_8n**	1: 16-bit line store, 0: 8-bit line store
3	**mode control bit 3**	
2	**mode control bit 2**	
1	**mode control bit 1**	
0	**mode control bit 0**	

Mode Control Bit Table

Mode	mode control bit [3:0]	Description
m600x1e	0000	
m600x1t	0001	Mode 600x1 test
m600x1eg	0010	Mode 600x1 enhanced with 1-bit grayscale
m600x1tg	0011	Mode 600x1 not edge enhanced, just 1-bit gray scale
m300x1e	0100	Mode 300x1 enhanced
m300x1t	0101	Mode 300x1 test
m200x1e	0110	Mode 200x1 enhanced
m200x1t	0111	Mode 200x1 test
m100x1e	1000	Mode 100x2 enhanced
m100x1t	1001	Mode 100x1 test
m1200x1	1010	Mode 1200x1
m600x8	1011	Mode 600x8
m300x8	1100	Mode 300x8

Control Register B (Address = 203, 202)

15 - 11	reserved	
10	**Alignment bit 2**	Select shift register which data to use for serial data in
9	**Alignment bit 1**	
8	**Alignment bit 0**	

7 - 5	reserved	
4	**ShiftDir**	Direction to shift 1-bit data, 1:LSB first, 0:MSB first
1	**ClockSelect 1**	
0	**ClockSelect 0**	

Control Register C (Address = 205, 204)

15 - 11	**LsyncWidth**	Number of clocks in CPUlsync
10 - 0	**HMargin**	Count of engine clocks to delay the start of the line

Control Register D (Address = 207, 206)

15 -12	reserved	
11 - 0	**LineLength**	Number on source pixels in line

Control Register E (Address = 209, 208)

15 - 0	**VMarginTop**	Vertical margin in lines

Control Register F (Address = 20B, 20A)

15 - 0	**VMarginBottom**	

Control Register G (Address = 20D, 20C)

15 - 0	**c_reg[15:0]**	C register for modulator, default = 0xb c_adj[15:0] = c_reg[15:0] window_adj = c_reg[14:0]

Control Register H (Address = 20F, 20E)

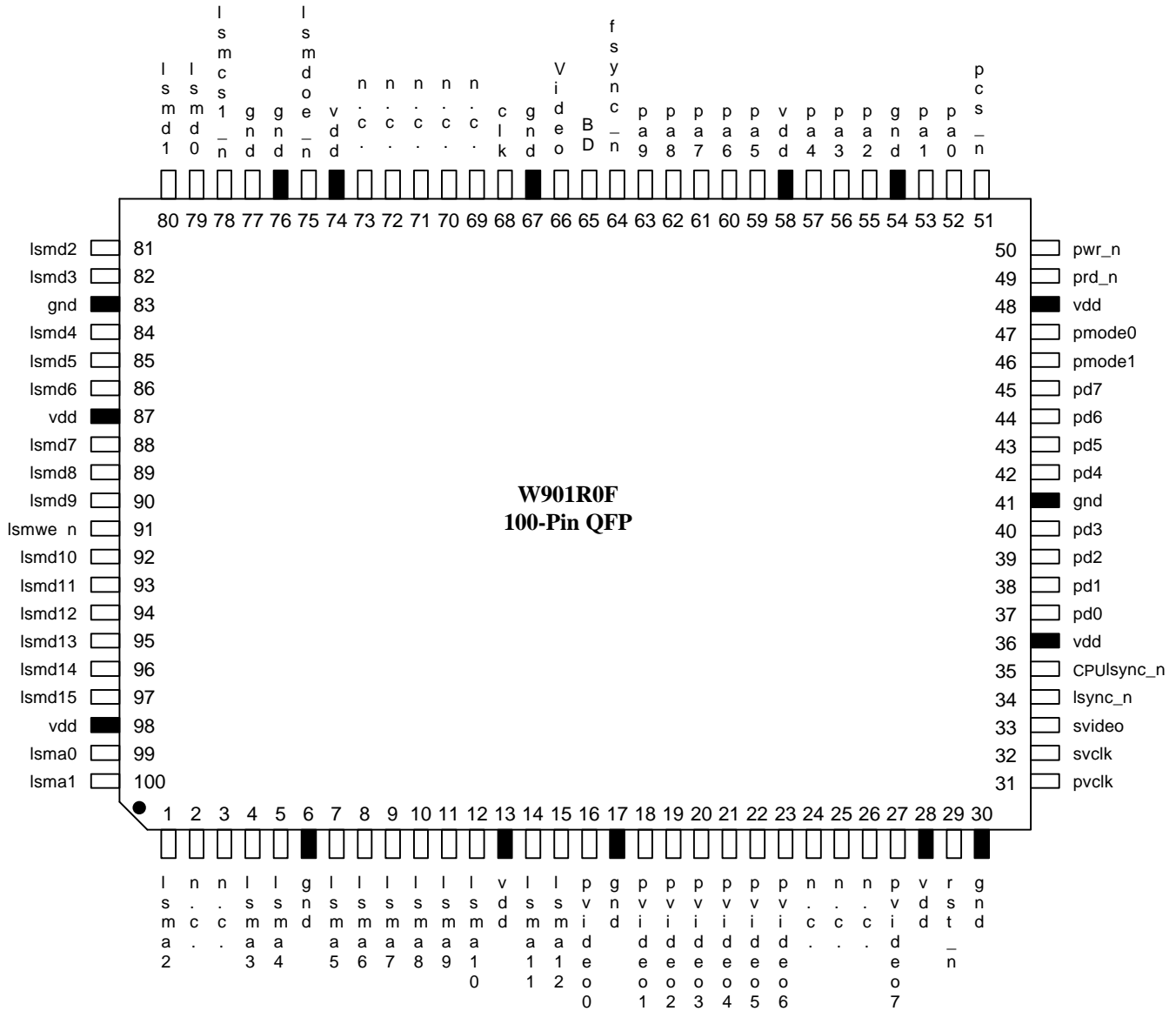| 15 - 4	**VMarginTop**	
3 - 0	**UpperLineStoreAddress [3:0]**	line store address(lsma) = { UpperLineStoreAddress[3:0], pa[8:0] }

Control Register I (Address = 211, 210)

15 - 0	**t_reg[15:0]**	T register for modulator, default = 7fe1 c_lb = t_reg[0] window_adj_lb = t_reg[1]

5. Pin Description

NAME	TYPE	Pin Number	Description
lsmd[15:0]	B	97, 96, 95, 94, 93, 92, 90, 89, 88, 86, 85, 84, 82, 81, 80, 79	Bidirection 16-bit line memory data.
lsma[12:0]	O	15, 14, 12, 11,10, 9, 8, 7, 5, 4, 1, 100, 99	13-bit address for line memory address.
lsmdoe_n	O	75	Active low line memory data output enable.
lsmwe_n	O	91	Active low line memory write strobe.
lsmcs1_n	O	78	Active low line memory chip select.
pvideo[7:0]	I	27, 23, 22, 21, 20, 19, 18, 16	8-bit parallel video data inputs.
rst_n	I	29	Active low reset. rst_n reset all control registse except - register G = 000B - register I = 7FE1
pvclk	O	31	Parallel video strob clock output. pvideo is to be latched into superchip on the rising edge of pvclk.
svideo	I	33	serial video data input
svclk	O	32	Serial video clock. svclk is continuous clock output with SourceSelect[1:0] = 00 when fsync_n is set to 1.
lsync_n	O	34	clocked line sync output
CPUlsync_n	O	35	Line sync output to processor. The width of sync may be programmable by LsyncWidth in control register C[15:11]
pd[7:0]	B	45, 44, 43, 42, 40, 39, 38, 37,	Processor data.
pmode[1:0]	I	46, 47	pmode defins the meaning of pwr_n and prd_n. - pmode[1:0] = 00, prd_n and pwr_n are labelled. - pmode[1:0] = 01, pwr_n become read/write strobe, in this mode prd_n and pwr_n should be tied together.
prd_n	I	49	Active low processor read enable.
pwr_n	I	50	Active low processor write enable.
pcs_n	I	51	Active low processor chip select.
pa[9:0]	I	63, 62, 61, 60, 59, 57, 56, 55, 53, 52	Processor address

fsync_n	I	64	Active low page start sync input.
BD	I	65	Raw beam detect input from engine.
Video	O	66	Video data output to engine.
clk	I	68	Input x1 clock for video processing. It should fit to engine speed.
vdd		13, 28, 36, 48, 58, 74, 87, 98	
gnd		6, 17, 30, 41, 54, 67,76, 77, 83	
N.C.		2, 3, 24, 25, 26, 69, 70, 71, 72, 73	Reserved

6. Pin Assignment

W901R0F
100-Pin QFP

Top pins (left to right, 80–51): lsmd1, lsmd0, lsmcs1_n, gnd, gnd, lsmdoe_n, vdd, nc., nc., nc., nc., nc., clk, gnd, Video, BD, fsync_n, paa9, paa8, paa7, paa6, paa5, vdd, paa4, paa3, paa2, gnd, paa1, paa0, pcs_n

Left pins (top to bottom, 81–100):
- 81 lsmd2
- 82 lsmd3
- 83 gnd
- 84 lsmd4
- 85 lsmd5
- 86 lsmd6
- 87 vdd
- 88 lsmd7
- 89 lsmd8
- 90 lsmd9
- 91 lsmwe_n
- 92 lsmd10
- 93 lsmd11
- 94 lsmd12
- 95 lsmd13
- 96 lsmd14
- 97 lsmd15
- 98 vdd
- 99 lsma0
- 100 lsma1

Right pins (top to bottom, 50–31):
- 50 pwr_n
- 49 prd_n
- 48 vdd
- 47 pmode0
- 46 pmode1
- 45 pd7
- 44 pd6
- 43 pd5
- 42 pd4
- 41 gnd
- 40 pd3
- 39 pd2
- 38 pd1
- 37 pd0
- 36 vdd
- 35 CPUlsync_n
- 34 lsync_n
- 33 svideo
- 32 svclk
- 31 pvclk

Bottom pins (left to right, 1–30): lsma2, nc., nc., lsma3, lsma4, gnd, lsma5, lsma6, lsma7, lsma8, lsma9, lsma10, vdd, lsma11, lsma12, pvideo0, gnd, pvideo1, pvideo2, pvideo3, pvideo4, pvideo5, pvideo6, nc., nc., nc., pvideo7, vdd, rst_n, gnd

Winbond
Electronics Corp.

CORPORATE HEADQUARTERS:

NO. 4, Creation Rd. III

Science-Based Industrial Park

Hsinchu, Taiwan, R.O.C.

TEL: 886-3-5770066

FAX: 886-3-5792646

INFORMATION CONTACTS:

Rongken Yang

Visual Comm. Product Design Dept. I

TEL: 886-3-5796142

E-mail: rkyang@winbond.com.tw

Note: All data and specifications are subject to change without notice.