Dual Timing Circuit

GENERAL DESCRIPTION

The XR-2556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-2556 may be triggered or reset on falling waveforms. Each output can source or sink up to 200 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-2556 are superior to those available from two separate timer packages.

FEATURES

Replaces Two 555-Type Timers
TTL Compatible Pinouts (Gnd—Pin 7, V_{CC}—Pin 14)
Timing from Microseconds Thru Hours
Excellent Matching Between Timer Sections
Operates in Both Monostable and Astable Modes
High Current Drive Capability (200 mA each output)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C
Normally ON and Normally OFF Outputs

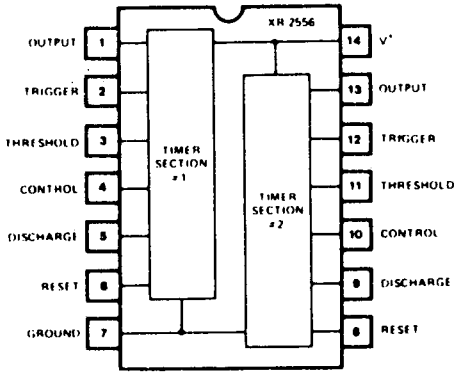
APPLICATIONS

Precision Timing
Pulse Generation
Sequential Timing
Pulse Shaping
Time Delay Generation
Clock Pattern Generation
Missing Pulse Detection
Pulse-Width Modulation
Frequency Division
Clock Synchronization
Pulse-Position Modulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	5 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperate Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2556M	Ceramic	−55°C to +125°C
XR-2556CN	Ceramic	0°C to +70°C
XR-2556CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2556 is a high output dual timing circuit similar to the popular 555-type timer, capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from 4.5 V to 18 V. The output stage can source or sink 200 mA. Each timing section is fully independent.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which produces a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-2556 is high during the timing interval and pulls low at timeout. It is triggered and reset on falling waveforms. The control voltage inputs (Pins 4 and 10) may serve as pulse width modulation points. Matching between sections is typically better than 0.2% initially with temperature drift tracking to ±10 ppm/°C.

For low voltage and/or low power drain applications consider the XR-L556.

XR-2556

ELECTRICAL CHARACTERISTICS

Test Conditions: (Each timer section, T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.)

PARAMETERS	XR-2556M			XR-2556C			UNITS	FIGURE	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Supply Voltage	4.5		18	4.5		16	V	7	
Supply Current (Each Timer Section)		3 10	5 12		3 10	6 15	mA mA	7	Low State Output, Note 1 V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞
Total Supply Current (Both Timer Sections)		6 20	10 24		6 20	12 30	mA mA	7	Low State Output V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage		0.5 30 0.05	2.0 100 0.1		1.0 50 0.05		% ppm/°C %/V	 13 12	R_A, R_B = 1 kΩ to 100kΩ Note 2, C = 0.1 μF
Threshold Voltage		2/3			2/3		x V_{CC}		
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	6	V_{CC} = 5V V_{CC} = 15V
Trigger Current		0.5			0.5		μA		
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V		
Reset Current		0.1			0.1		mA		
Threshold Current		0.1	0.25		0.1	0.25	μA		Note 3
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0			V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		 0.10 0.1 0.4 2.0 2.5	 0.25 0.15 0.5 2.2		 0.25 0.1 0.4 2.0 2.5	 0.35 0.25 0.75 2.5	 V V V V V V	9 11	V_{CC} = 5V I_{sink} = 8.0 mA I_{sink} = 5.0 mA V_{CC} = 15V I_{sink} = 10 mA I_{sink} = 50 mA I_{sink} = 100 mA I_{sink} = 200 mA
Output Voltage Drop (High)	 3.0 13	 3.3 13.3 12.5		 2.75 12.75	 3.3 13.3 12.5		 V V V	8	I_{source} = 100 mA V_{CC} = 5V V_{CC} = 15V I_{source} = 200 mA V_{CC} = 15V
Rise Time of Output		100			100		nsec		
Fall Time of Output		100			100		nsec		
Matching Characteristics Initial Timing Accuracy Timing Drift with Temperature		0.2 ±10	0.6		0.2 ±10		% ppm/°C		Note 4

Note 1: Supply current when output is high is typically 1.0 mA less.
Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 meg-ohms.
Note 4: Matching characteristics refer to the difference between performance characteristics of each timer section.

PRINCIPLES OF OPERATION

Figure 2 is the functional block diagram for each timer section of the XR-2556. These sections share the same V+ and ground leads, but have independent outputs and control terminals. Therefore, each timer section can operate independently of the other. The timing cycle of each section is determined by an external resistor-capacitor network.

MONOSTABLE (ONE-SHOT) OPERATION

When operating either timer section of the XR-2556 in the monostable mode, a single resistor and a capacitor are used to set the timing cycle. The discharge and threshold terminals are also interconnected in this mode, as shown in Figure 3.

Referring to Figure 2, monostable operation of the XR-2556 is explained as follows: the external timing capacitor C is held discharged by the internal transistor, T_O. The internal flip-flop is triggered by lowering the trigger levels (pins 2 or 12) to less than 1/3 V_{CC}. The circuit triggers on a *negative-going* slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pins 1 or 13 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal interval resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

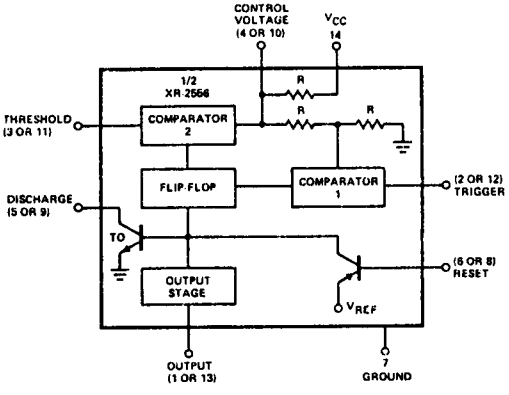


Figure 2. Functional Diagram of One Timer Section

Once the circuit is triggerd it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pins 6 or 8). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to V+ when not used to avoid the possibility of false triggering.

Figure 4 shows the waveforms during the monostable timing cycle. The top waveform is the trigger pulse; the

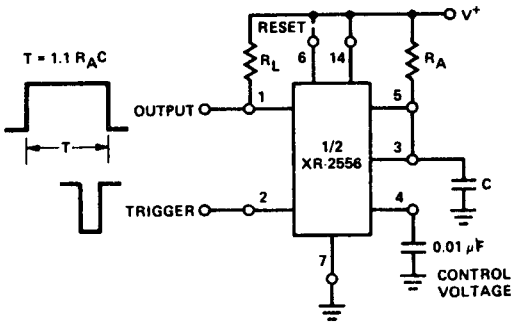


Figure 3. Monostable (One-Shot) Circuit

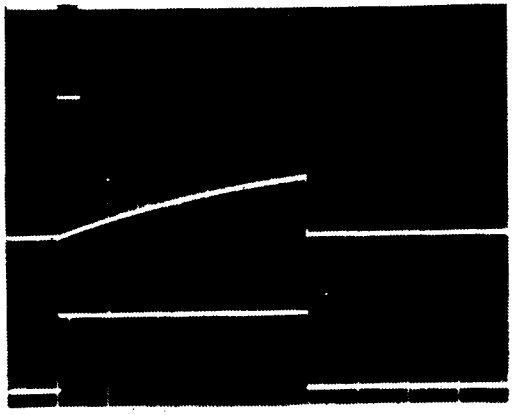


Figure 4. Monostable Waveforms
Top: Trigger Input
Middle: Exponential Ramp across Timing Capacitor
Bottom: Output Logic Level

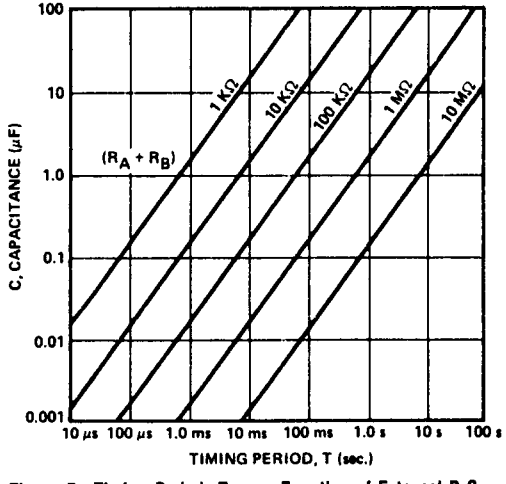


Figure 5. Timing Period, T, as a Function of External R-C Network

TYPICAL CHARACTERISTICS (Each Timer Section)

middle is the exponential ramp across the timing capacitor. The bottom waveform is the output logic state (at pins 1 or 13) during the timing cycle. For proper operation of the circuit, the trigger pulse-width must be less than the timing period.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_A C$$

This time delay varies linearly with the choice or R_A and C as shown by the timing curves of Figure 5.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 15. The external capacitor charges to 2/3 V_{CC} through the parallel combination of R_A and R_B, and discharges to 1.3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with the exponential waveform as shown in Figure 16. The output level at pin 1 (or 13) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 6 or 8)

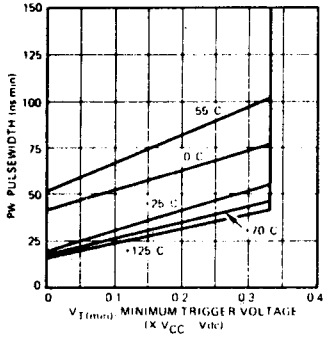


Figure 6. Trigger Pulse Width

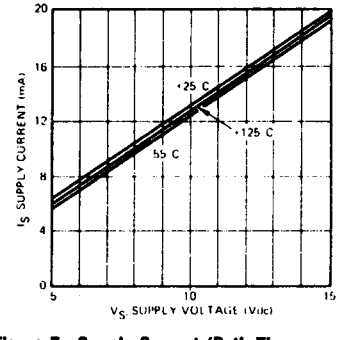


Figure 7. Supply Current (Both Timer Sections)

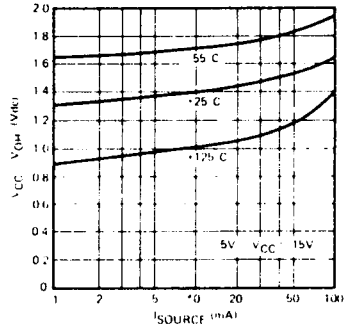


Figure 8. High Output Voltage

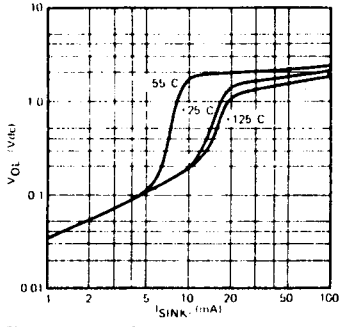


Figure 9. Low Output Voltage V_{CC} = 5.0 Vdc

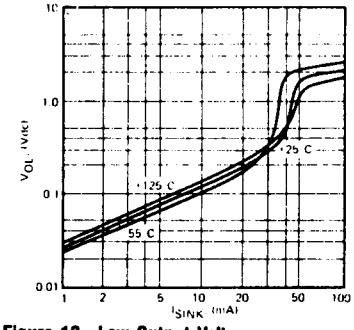


Figure 10. Low Output Voltage V_{CC} = 10 Vdc

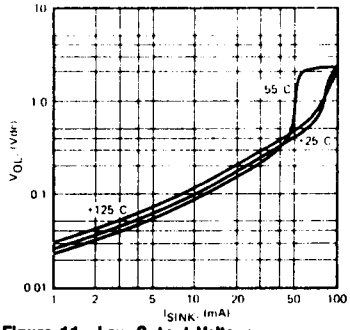


Figure 11. Low Output Voltage V_{CC} = 15 Vdc

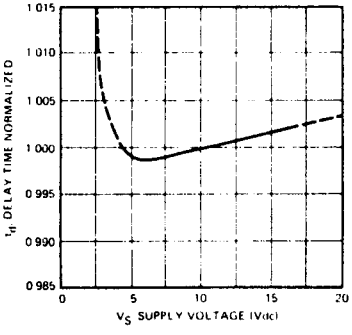


Figure 12. Delay Time vs. Supply Voltage

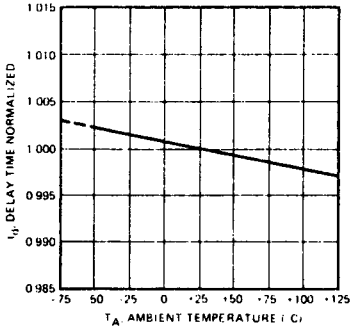


Figure 13. Delay Time vs. Temperature

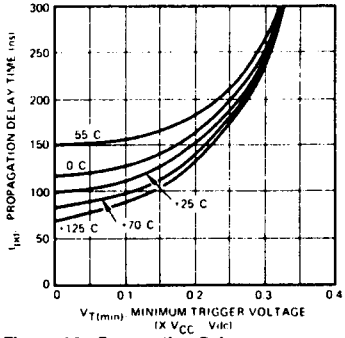


Figure 14. Propagation Delay vs. Trigger Voltage

The charge time (output high) is given by:

$$t_1 = 0.695\,(R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 = 0.695\,(R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\,(R_A + 2R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \text{ and}$$

may be easily found as shown in Figure 17.

The duty cycle, D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

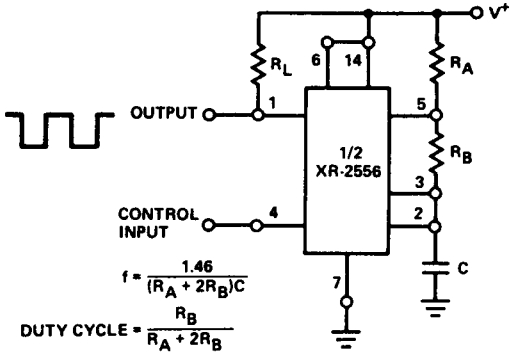


Figure 15. Astable (Free-Running) Circuit

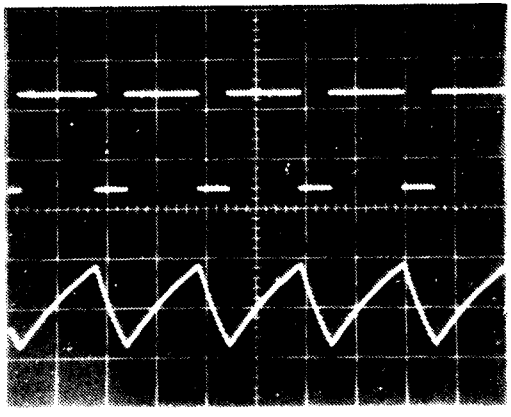


Figure 16. Astable Waveforms
Top: Output Waveform
Bottom: Waveform Across Timing Capacitor

To obtain the maximum duty cycle, R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 5 current) within the maximum rating of the discharge transistor (200 mA).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT (PINS 1 or 13)

The output logic level is normally in a "low" state, and goes "high" during the timing cycle. Each output of the XR-2556 is a "totem pole" type capable of sinking or sourcing 200 mA of load current (see Figure 18).

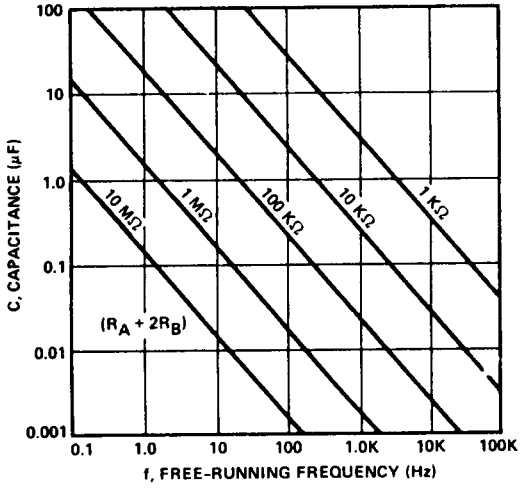


Figure 17. Free Running Frequency as a Function of External Timing Components

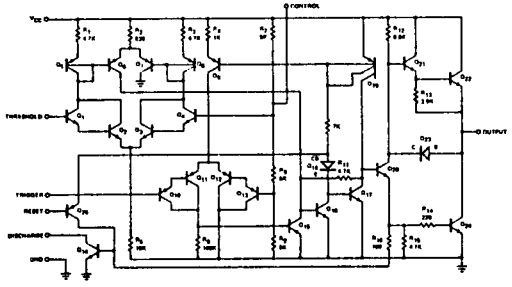


Figure 18. Circuit Schematic—1/2 of XR-2256

TRIGGER (PINS 2 OR 12)

The timing cycle is initiated by lowering the dc level at the trigger terminal below 1/3 V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is completed.

THRESHOLD (PINS 3 or 11)

The timing cycle is completed when the voltage level at the trigger terminal reaches 2/3 V_{CC}. At this point, Comparator #2 of Figure 2 changes state, resets the internal flip-flop, and initiates the discharge cycle.

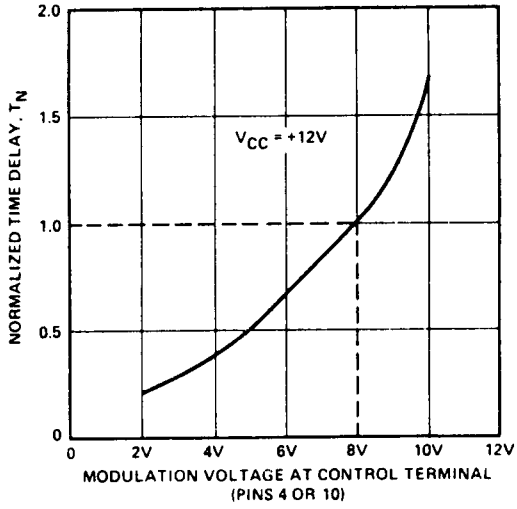


Figure 19. Normalized Time Delay vs. Modulation Voltage

CONTROL OR FM (PINS 4 OR 10)

The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 4 or 10. This terminal is internally biased at 2/3 V_{CC}. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. Figure 19 shows the variation of the timing period, T, as a function of dc voltage at the control terminal. When not in use, the control terminals should be ac grounded through 0.01 μF decoupling capacitors.

DISCHARGE (PINS 5 OR 9)

This terminal corresponds to the collector of the discharge transistor, T_D, of Figure 2. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

RESET (PINS 6 OR 8)

The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the rest voltage is applied. When the reset signal is removed, the output remains "low" until re-triggered. When not used, the reset terminals should be connected to V_{CC} in order to avoid any possibility of false triggering. When the timing circuits are operated in the astable mode, the reset terminals can be used for "on" and "off" keying of the oscillations. (See Figure 22).

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-2556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 20 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\ R_1C_1 \text{ and } T_2 = 1.1\ R_2C_2$$

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 21. When Timer 1 is triggered at pin 2, its output at pin 1 goes "high" for a time duration $T_1 = 1.1\ R_1C_1$. At the end of this timing cycle, pin 1 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 1 and 12. Then, the output at pin 13 goes "high" for a time duration $T_2 = 1.1\ R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 2 by a time delay of T_1.

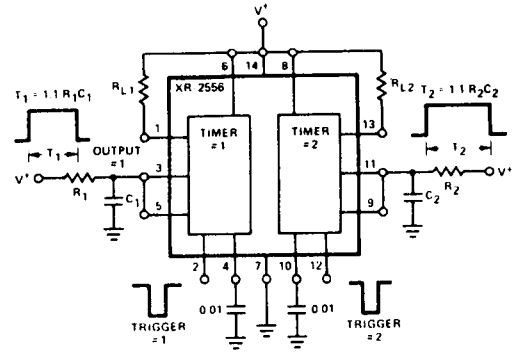


Figure 20. Generation of Two Independent Time Delays

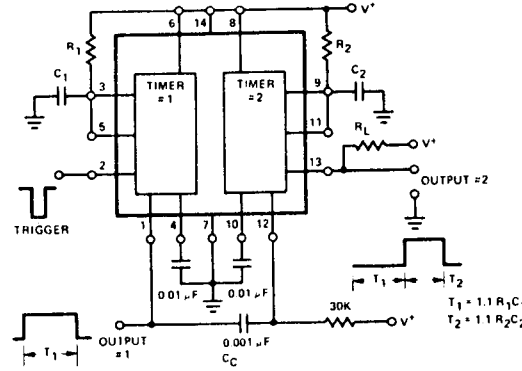


Figure 21. Sequential Timing

KEYED OSCILLATOR

One of the timer sections of the XR-2556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 22. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 8) of Timer 2.

When the circuit is at rest, the logic level at the output of Timer 1 is "low"; and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 22.

FREQUENCY DIVIDER

If the frequency of the input is known, each timer section of the XR-2556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= 1.1 R_1C_1) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than 1.1 R_1C_1 will actually trigger the circuit.

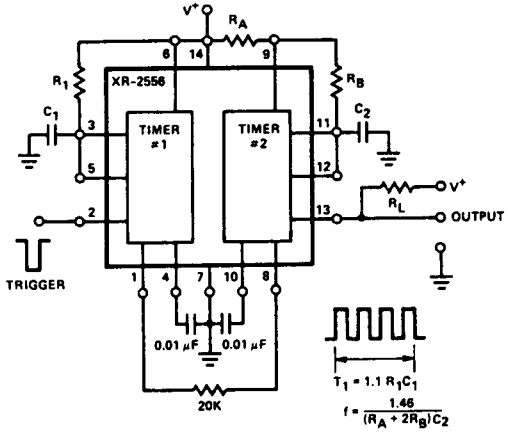


Figure 22. Keyed Oscillator

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\left(\frac{T}{T_P} - 1\right) < N < \frac{T}{T_P}$$

where T_P is the period of the input pulse signal.

Figure 23 shows the circuit waveforms for divide-by-five operation for one of the timer sections of the XR-2556. In this case, the timing period of the circuit is set to be approximately 4.5 times the period of the input pulse.

Since the two timer sections of the XR-2556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-2556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_S/N_1 \text{ and } f_2 = f_S/N_2$$

where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (3, 5) and (9, 11).

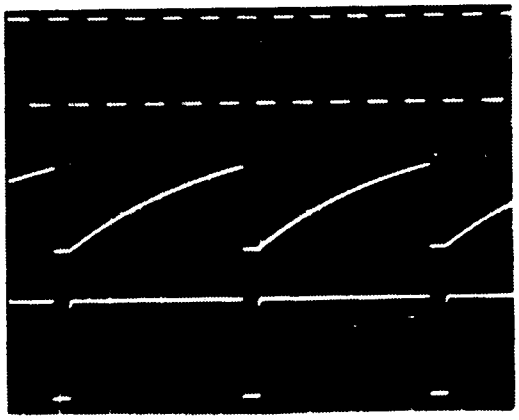


Figure 23. Frequency Divider Waveforms
Top: Input Pulse Train (f = 5 kHz)
Middle: Waveforms Across Timing Capacitor
Bottom: Output Waveform (f = 1 kHz)

FREQUENCY DIVIDER AND PULSE SHAPER

Frequency division can be performed by 1/2 of the XR-2556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 24, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse-shaper.

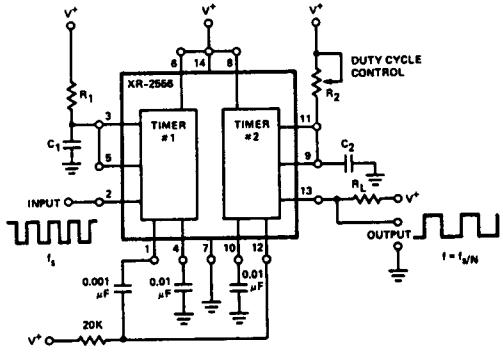


Figure 24. Frequency Divider and Pulse-Shaper

The output of Timer 1 (pin 1) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 13) can be adjusted from 1% to 99% by varying the value of R_2.

Figure 25 shows the circuit waveforms in this application. The top waveform is the input signal of frequency f_S applied to the trigger input (pin 2) of Timer 1. The middle waveform is the output of Timer 1 for divide-by-three operation; and the bottom waveform is the pulse-shaped output obtained from Timer 2 (pin 13).

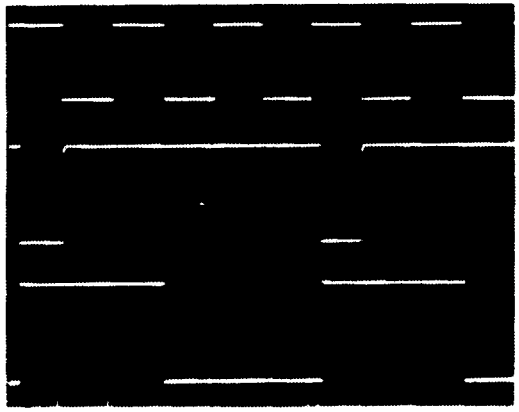


Figure 25. Frequency Divider and Pulse-Shaper Waveforms
Top: Input Signal (f_S = 9 kHz)
Middle: Output at Pin 1 for Divide-by-3
Bottom: Variable Duty Cycle Output at Pin 13

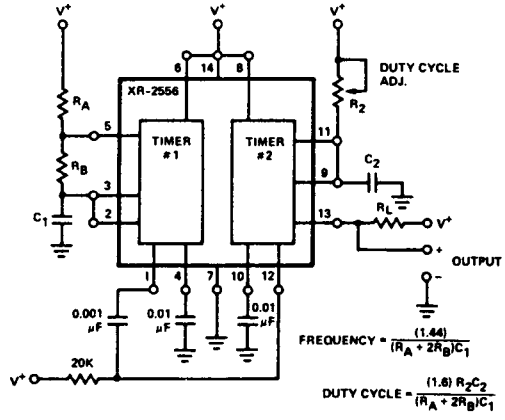


Figure 26. Fixed Frequency Oscillator With Variable Duty Cycle

FIXED-FREQUENCY, VARIABLE DUTY CYCLE OSCILLATOR

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 26, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 13 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

The frequency and the duty cycle of the output waveform are given as:

$$\text{Frequency} = \frac{1.44}{(R_A + 2R_B)C_1}$$

$$\text{Duty Cycle} = \frac{(1.6)\,R_2C_2}{(R_A + 2R_BC_1)}$$

OSCILLATOR WITH SYNCHRONIZED OUTPUTS

The circuit of Figure 26 can also be used as an oscillator with synchronized multiple frequency outputs. Timer 1 generates an output at frequency f_1 at pin 1, as set by resistor R_A, R_B, and C_1. Timer 2 is used as a frequency divider by setting its timing cycle, T_2, to be larger than the period of Timer 1 (see section on frequency division). The resulting output of Timer 2 (pin 13) is at frequency f_2 given as:

$$f_2 = f_{1/N}$$

where N is the divider ratio set by the external R-C networks as described by Figures 23 and 24.

PULSE-WIDTH MODULATION

For pulse-width modulation, one-half of the XR-2556 is connected as shown in Figure 27. The circuit operates in its monostable mode and is triggered with a continuous pulse train. Output pulses are generated at the same rate as the input pulse train, except the output pulse-width is determined by the timing components R_1 and C_1.

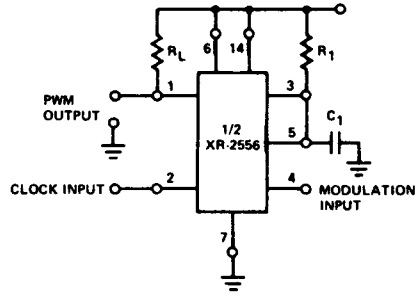


Figure 27. Pulse-Width Modulation

In this mode of operation, the duration of the timing cycle (i.e., the output pulse-width) can be modulated by applying a modulation input to the control voltage terminals (pins 4 or 10). The control characteristics associated with the modulation terminals are depicted in Figure 19. Figure 28 shows the actual circuit waveforms generated in this manner.

When using the XR-2556 for pulse-width modulation, an external clock signal is not necessary, since one section can be operated in its astable mode (see Figure 15) and serve as the clock generator. Figure 29 is the recommended connection for such an application. In this case, Timer 2 is used as the clock generator, and Timer 1 is used as the pulse-width modulator section.

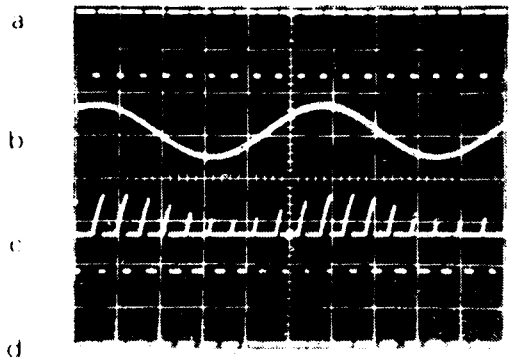


Figure 28. Pulse-Width Modulation Waveforms
a) Clock Input at Pin 2
b) Modulation Input at Pin 4
c) Capacitor Voltage at Pin 3
d) Pulse-Width Modulated Output at Pin 1

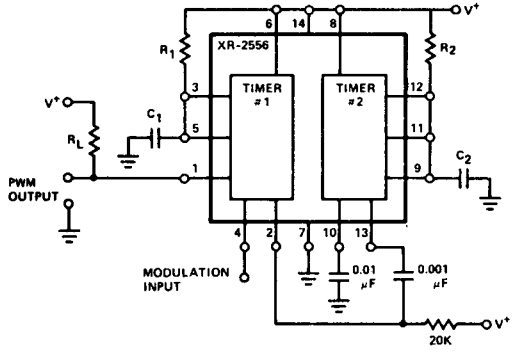


Figure 29. Pulse-Width Modulation With Internal Clock

PULSE-POSITION MODULATION

When a timer section of the XR-2556 is operated in its astable mode (see Figure 15), the period of the output pulse train can be varied by applying a modulation voltage to the corresponding modulation control terminal. In this manner, the repetition rate of the output pulse train can be varied, resulting in a pulse-position modulated output. Typical transfer characteristics between the timing cycle and the modulation voltage are given in Figure 19.

LOGIC "AND" AND "OR" CONNECTION OF OUTPUTS

The individual outputs (pins 1 and 13) of the XR-2556 can be interconnected as shown in Figure 30 to perform logic "or" and "and" functions. Since the output of each timer section is a high-current "totem-pole" type, external diodes are needed to avoid current flow from one output into the other.

Referring to Figure 30(a), the output logic level "P" would read "high" when either one of the outputs at pins 1 or 13 is "high." For Figure 30(b), the output will read "high" only when both outputs at pins 1 and 13 are "high".

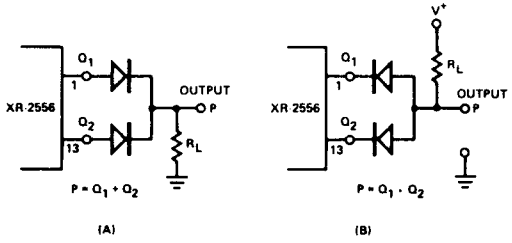
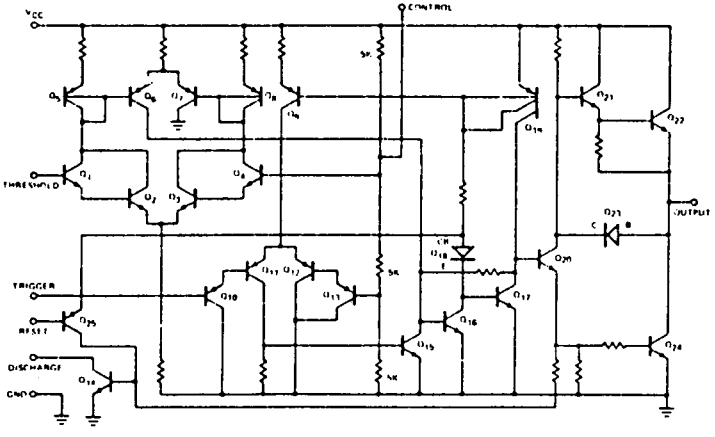


Figure 30. Logic "OR" and "AND"



One section of XR-2556

EQUIVALENT SCHEMATIC DIAGRAM

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

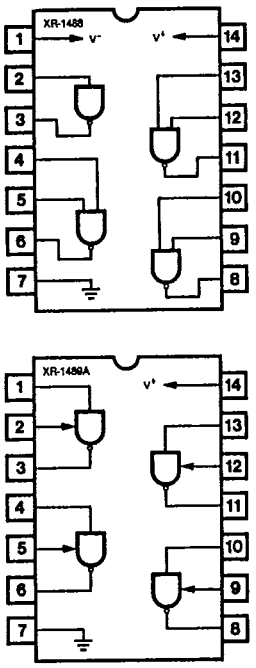
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.