XR-8105

Lithium-Ion Cell Protection System

December 1996-1

FEATURES

- Cell Over-Voltage Detection
- Cell End of Discharge Voltage Detection
- Cell Under-Voltage Detection
- Externally Programmable Trip Voltages
- Low Input Bias Current

APPLICATIONS

- Lithium Ion Battery Pack Protection

BENEFITS

- High Pack Reliability
- Irreparable Cell Damage Avoidance
- Early Warning of Impending Disconnect

GENERAL DESCRIPTION

The lithium Ion Protection circuit is a monolithic IC which will handle all major Lithium Ion battery protection requirements during charge and discharge. Three or four cell systems may be used. This IC is designed to provide highly accurate monitoring of charging conditions for each cell to determine maximum safe cell voltage, and discharging conditions for minimum advisable discharge voltage level.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-8105EID	16 Lead 300 Mil JEDEC SOIC	-40°C to +85°C

BLOCK DIAGRAM

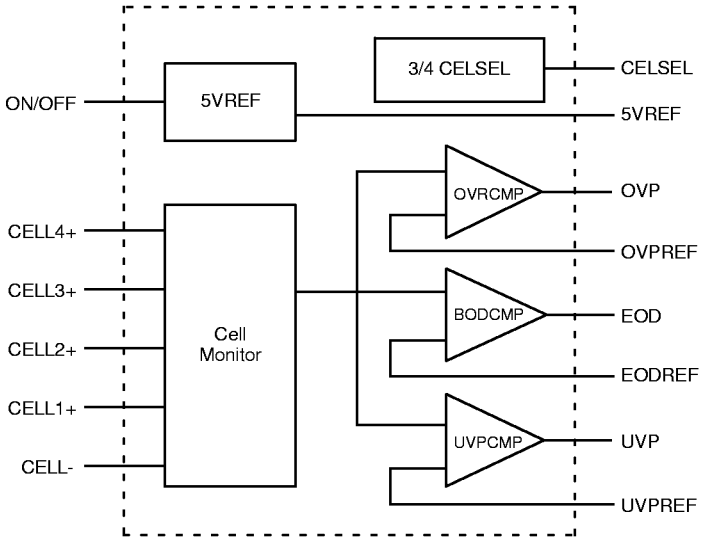
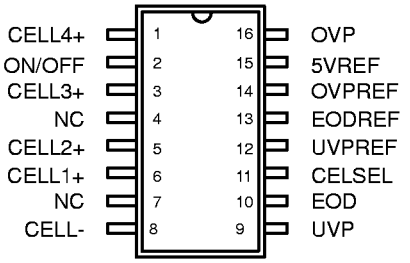


Figure 1. Simplified Li-Ion Protection Block Diagram

PIN CONFIGURATION



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	CELL4+	I	**Cell 4 positive connection.** Cell 4 is connected between CELL4+ and CELL3+ pins.
2	ON/OFF	I	**Used to enable and disable the IC.** IC supply current reduces below 100nA in under voltage condition (shutdown). Connected to negative terminal of the battery charger.
3	CELL3+	I	**Cell 3 positive connection.** Cell 3 is connected between CELL3+ and CELL2+ pins.
4	NC		**No Connect.**
5	CELL2+	I	**Cell 2 positive connection.** Cell 2 is connected between CELL2+ and CELL1+ pins.
6	CELL1+	I	**Cell 1 positive connection.** Cell 1 is connected between CELL1+ and CELL- pins.
7	NC		**No connect.**
8	CELL-	I	**IC ground reference potential.**
9	UVP	O	**Under-voltage protection output.** This pin provides output current when under-voltage condition is detected.
10	EOD	O	**End of discharge output.** This pin provides CMOS logic output when end of discharge condition is detected.
11	CELSEL	I	**Used to set up system for 3 or 4 cell operation.** Connect to 5VREF for 4 cell application and to CELL- for 3 cell application. Short out CELL4+ to CELL3+ for 3 cell application.
12	UVPREF	I	**Input reference voltage for under-voltage detection comparator.** Reference voltage is provided through a resistive divider referenced to on board 5VREF voltage reference.
13	EODREF	I	**Input reference voltage for end of discharge detection comparator.** Reference voltage is provided through a resistive divider referenced to on board 5VREF voltage reference.
14	OVPREF	I	**Input reference voltage for over-voltage detection comparator.** Reference voltage is provided through a resistive divider referenced to on board 5VREF voltage reference.
15	5VREF	O	**Reference voltage provided to set up EODREF, UVREF and OVREF reference voltages through a resistive divider (see application circuit).**
16	OVP	O	**Over-voltage detection output.** This pin provides output current when over-voltage condition is detected.

ELECTRICAL CHARACTERISTICS

Test Conditions: 4 Cells, Each Cell Voltage = 4 VDC, T_A = 25°C, See Test Circuit

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Characteristics						
I_{CELL4+}	Supply Current, ON State	200	265	350	µA	Each Cell Voltage = 4V
I_{CELL4+}	Supply Current, OFF State			100	nA	UVP (Shut-Down) mode, (V_{CELL4+} -$V_{ON/OFF}$) < 1.0V
V_{CELL4+}	Operating Voltage	5.3		25	V	Total Cell Voltage; Measured on CELL4+ Pin.
5VREF	5V Reference Voltage	4.9	5.0	5.1	V	Load Resistor = 500kΩ
I_{5VREF}	5VREF Output Current		10	200	µA	ΔV_{5VREF} < 50mV
I_{CELL3+}	Cell 3 Input Bias Current	-10	-1	10	nA	Each Cell Voltage = 4V
I_{CELL2+}	Cell 2 Input Bias Current	-10	-2	10	nA	Each Cell Voltage = 4V
I_{CELL1+}	Cell1 Input Bias Current	-20	-8	-2	nA	Each Cell Voltage = 4V
V_{EOD}	EOD Output Voltage, High Level	4.0	4.27	4.5	V	I_{EOD} = 50µA, Activated State
V_{EOD}	EOD Output Voltage, Low Level	0.70	0.67	0.80	V	I_{EOD} = 50µA, Normal State
I_{EOD}	EOD Output Source Current	400	600		µA	V_{EOD} > 4V, Activated State
I_{EOD}	EOD Output Sink Current	200	300		µA	V_{EOD} < 0.80V, Normal State
I_{OVP}	OVP Output Current, Normal		10	100	pA	Each Cell Voltage = 4V, V_{OVP} = 0V
I_{OVP}	OVP Output Current, Activated	10	18	26	µA	Each Cell Voltage = 4V, V_{OVP} = V_{CELL4+} -0.5V
I_{UVP}	UVP Output Current, Normal		10	100	pA	Each Cell Voltage = 4V, V_{UVP} = 0V
I_{UVP}	UVP Output Current, Activated	10	18	25	µA	Each Cell Voltage = 4V, V_{UVP}= V_{CELL4+} -0.5V
V_{ON}	ON/OFF ON Threshold	3.2	3.5	3.8	V	Each Cell Voltage = 2.3V, Apply Voltage Between ON/OFF Pin and CELL4+ Pin.
V_{OFF}	ON/OFF OFF Threshold	2.8	3.1	3.4	V	Each Cell Voltage = 2.3V, Apply Voltage Between ON/OFF Pin and CELL4+ Pin.
Voltage Sense Threshold						
OVP	Over Voltage Protection Turn-ON Threshold	4.15	4.2	4.25	V	Each Cell Voltage = 4V. Increasing Voltage Applied to Cell Under Such Test Until Trip Point.
UVP	Under Voltage Protection Turn-ON Threshold	2.4	2.5	2.6	V	Each Cell Voltage = 2.3V. Increasing Voltage Applied to Cell Under Test Until Trip Point.
ΔOVP	OVP Turn-ON Threshold Matching Between Cells		10	20	mV	Each Cell Voltage = 4V
ΔUVP	UVP Turn-ON Threshold Matching Between Cells		60	120	mV	Each Cell Voltage = 2.3V
ΔEOD	EOD Turn-On Threshold Matching Between Cells		70	140	mV	Each Cell Voltage = 2.5V

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
OVP_{HYS}	OVP Threshold Hysteresis	70	100	130	mV	Each Cell Voltage = 4V
UVP_{HYS}	UVP Threshold Hysteresis	70	100	130	mV	Each Cell Voltage = 4V
EOD_{HYS}	EOD Threshold Hysteresis	15	25	35	mV	Each Cell Voltage = 4V
Cell Imbalance						
$ICELL_{IMB}$	Maximum Cell Imbalance Current			60 40	nA nA	4 Cell Application 3 Cell Application

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage . . . . . $-0.5V < V_{CELL4+} < 30V$

OVP Output . . . . . $-28V < V_{OVP} < V_{CELL4+}$

UVP Output . . . . . $-0.5V < V_{UVP} < 28V$

EOD Output . . . . . $-0.5V < V_{EOD} < 28V$

Storage Temperature . . . . . -65°C to +150°C

Operating Temperature . . . . . -40°C to +85°C

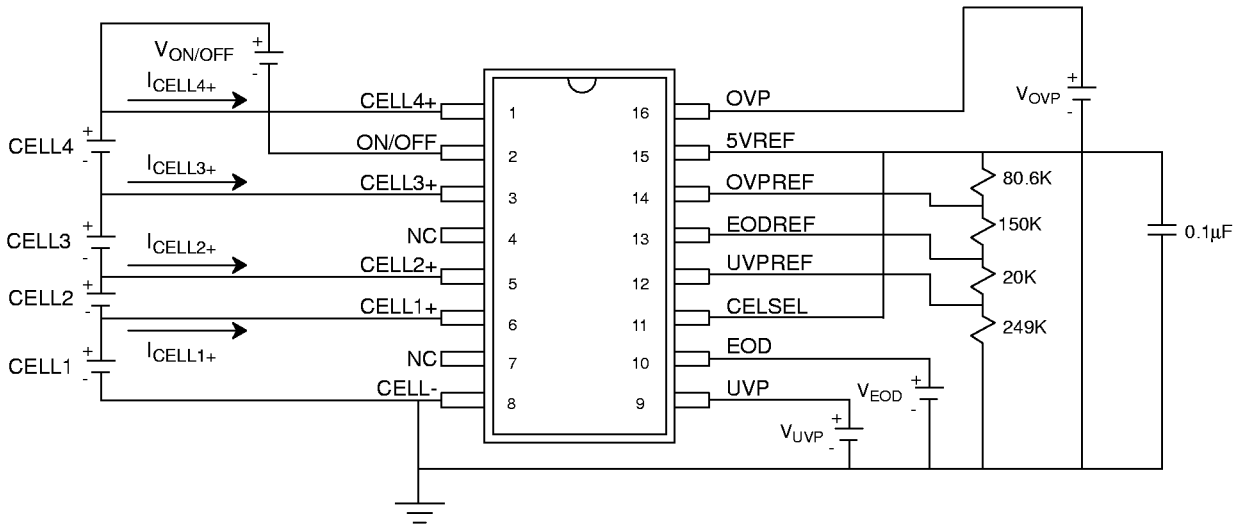


Figure 2. Test Circuit

SYSTEM DESCRIPTION

Cell Over-Voltage Detection

If any cell, or group of parallel cells exceeds an adjustable maximum Over-Voltage threshold level (set via external resistor divider network, typically 4.2V), the protection circuit will shut off output current source (typically 15µA) at the OVP output, removing gate drive for the external MOS switch which disrupts battery current charge path. OVP comparator has built in threshold hysteresis of 100mV typical. Thus the charge path will remain open until cell voltage drops below 4.1V at which point the battery can be charged again.

Cell End of Discharge Voltage Detection

When any cell in the pack first discharges to an adjustable (via external resistor divider network), End of Discharge voltage level, typically set at 2.7V, the protection circuit will output a compatible TTL and CMOS compatible high level on the EOD pin. EOD provides low output level under normal conditions. This signal is intended to be used as warning to the user to prepare his/her system for battery recharging.

Cell Under-Voltage Detection

If any cell, or group of parallel cells drops to an adjustable minimum Under-Voltage threshold level (set via external resistor divider network, typically 2.5V), the protection circuit will shut off output current source (typically 15µA) at the UVP output, removing gate drive for the external MOS switch which disrupts battery current discharge path. UVP comparator has built in threshold hysteresis of 100mV typical. Thus the discharge path will remain open until cell voltage increases above 2.6V at which point the battery can be discharged again.

Cell Imbalance

The cell voltage monitor current is less than 20nA. However, the maximum cell imbalance current can get as high as 60nA. A 4 cell battery pack will not be imbalanced by more than 5% in 142.7 years while using this circuit. For a 3 year period the maximum cell imbalance due to XR-8105 cell bias current will be < 0.11%.

3 Cell and 4 Cell Operation

The XR-8105 can work with 3 cell or 4 cell high stacks. Pin 11 is connected to VREF for 4 cell and to GND for 3 cell operation.

Startup

To initiate the XR-8105 proper operation, in the application circuit, a minimum of 5V voltage source is required to be temporarily applied between BATT+ and BATT- terminals. Without jump start both MOS switches will remain OFF preventing current flow to the load even though the battery may be fully charged. Thus the battery pack, upon assembly requires a brief connection to the charger or any 5V or greater value voltage source with minimum 1kΩ source resistance for the battery pack to be ready for proper operation.

THEORY OF OPERATION

Background

Li-Ion cells have a terminal voltage which ranges from 2.5V to 4.2V (different manufacturer's have slightly different voltages). The cells must be protected from exceeding these extremes on either end, which is a requirement different from earlier cell technologies. Meeting this requirement involves monitoring each cell in a cell pack. Because Li-Ion cells can be paralleled, any parallel cells can be monitored together. (e.g. a cell pack that is 4 cells in series will have 4 points to monitor. A pack that contains cells in a 3x3 matrix requires only 3 points to be monitored).

All current is ultimately returned to the bottom of the cell stack. Any cell input bias current results in causing the pack to become unbalanced. As an illustration, consider a 4 cell stack. The current removed from the node between cells 1 and 2 is experienced by only cells 1. The current removed from the node between cells 2 and cells 3 is experienced by cells 1 and cells 2. If the currents are the same, then cell 1 experiences twice the current flow of cell 2. This continues throughout the stack. The largest imbalanced will be between cell 1 and cell 4 where cell 4 conducts no bias currents and cell 1 conducts all 3 bias current, assuming that all 3 bias currents have the same polarity.

To minimize this effect, one of two possible methods can be employed. The first is sampling. Each cell can be sampled on a rotating basis, reducing the duty cycle on each cell so the effective average current is reduced. The

problem with this method can appear as two possible results: (1) A charge on an individual cell can be missed if it happens during a non monitor period or (2) if a change occurs in the charger output such that it reaches the full compliance voltage of the power supply between the monitoring cycles, it can cause the protection device to fail and leave you without protection. This will happen if the charger voltage is above the maximum voltage of the IC.

The second method is continuous measurement. The disadvantage of this is that there is a slightly higher system current drawn. The challenge is to minimize the bias currents for the measured inputs. The XR-8105 has a typical input bias current of 10mA. For today's capacity cells, this introduces not more that a 0.11% imbalance over a 3 year period (for 1.54AH battery), which is considered the shelf life by the cell manufacturer.

Operation

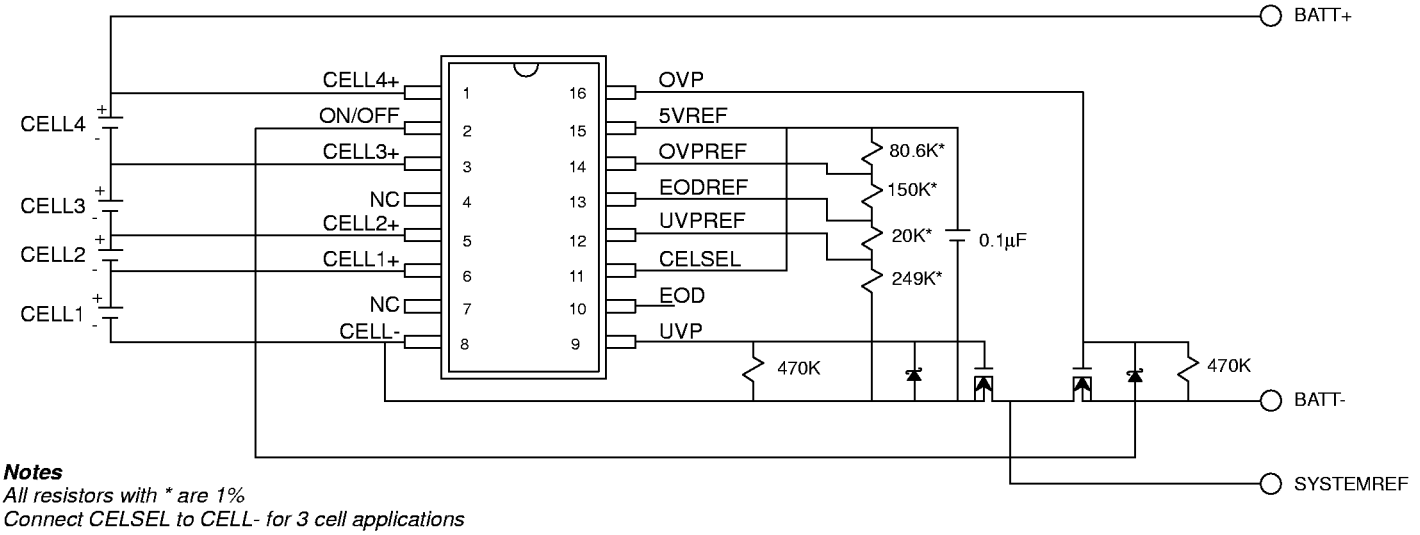
The EXAR XR-8105 monitors the voltage of 3 or 4 cell stacks with a differential input stage that isolates the voltage of each cell tap point. These differential voltages are compared to each of three reference voltages, which are externally set by the user based on both application and manufacturer's recommendations.

Two of these reference voltages: UVPREF and OVPREF are used to determine the state of two outputs that control external MOS switches via the UVP and OVP outputs respectively. The UVP output and MOS switch are used to block discharge current when any cell voltage reaches the UVPREF point. Charge current is still allowed via the body diode of the UVP MOS switch.

The UVP condition indicates that one of the cells has reached the UVP point, typically 2.5VDC. Any further drain on a cell that has reached this point can cause irreparable damage. Because of this, the GND point for all in pack circuitry is isolated by this MOS switch as well. Thus, when the UVP MOS switch is turned off, the system GND is lifted from the in-pack circuitry and all possible sources, of battery drain including XR-8105 supply current, are removed.

The reaction to an OVP condition is similar. If any cell in the peak reaches the OVPREF voltage (typically 4.2VDC), the OVP output turns off the OVP MOS switch, disconnecting the charge current path. Again, discharge current is allowed through the body diode of the OVP MOS switch. In this case, the in-pack electronics remain active.

One additional reference point and output exists. These are the pins used to detect and indicate an end of discharge voltage condition, or EOD. EOD is typically set at 2.7V. The EOD output is a logic level. A logic level "1" indicates an EOD condition, allowing a system to alert a user to shut down the host system in an orderly fashion prior to full power disconnect which occurs when the UVP threshold is reached.



Notes
*All resistors with * are 1%*
Connect CELSEL to CELL- for 3 cell applications

Figure 3. Application Schematic

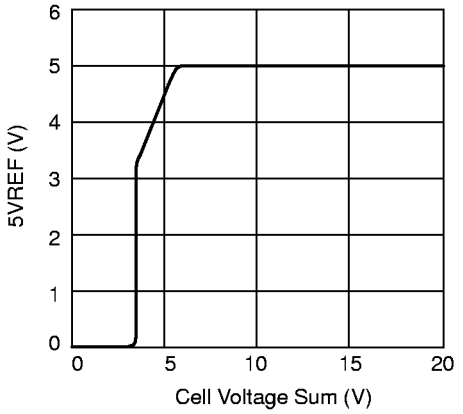


Figure 4. 5VREF Reference Voltage vs. Cell Voltage

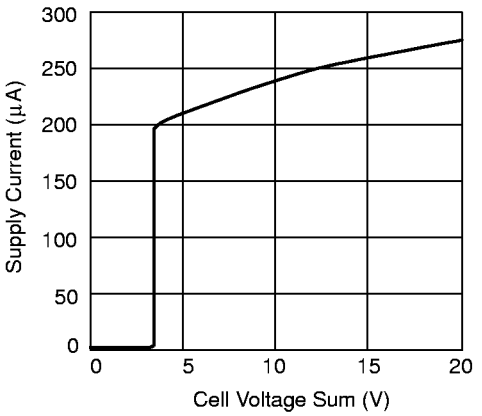


Figure 5. Supply Current vs. Cell Voltage Sum

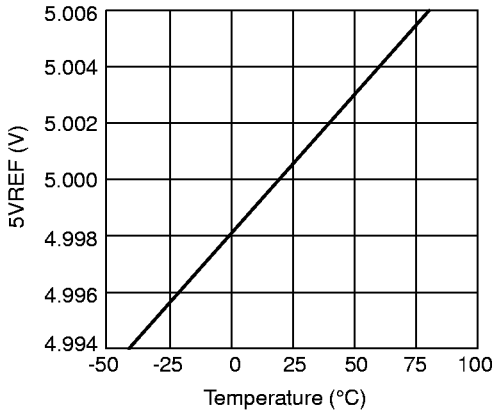


Figure 6. 5VREF Reference Voltage vs. Temperature

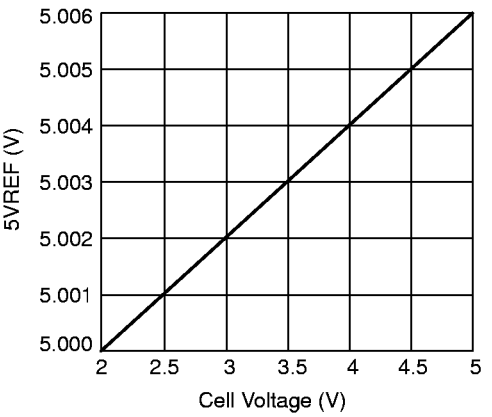


Figure 7. 5VREF Reference Voltage vs. Cell Voltage

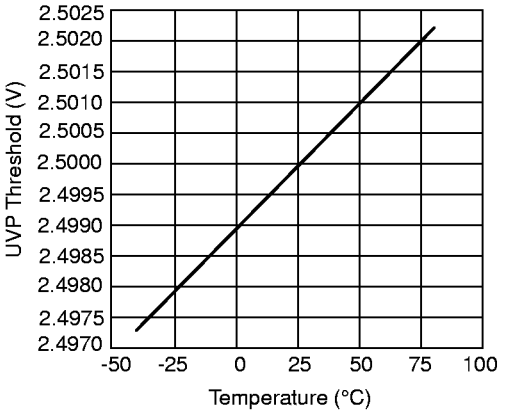


Figure 8. UVP Turn OFF Threshold vs. Temperature

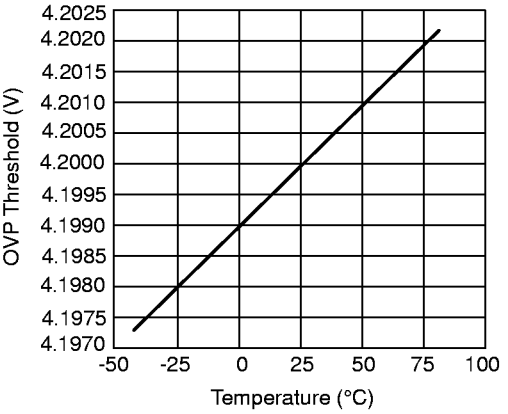


Figure 9. OVP Turn OFF Threshold vs. Temperature

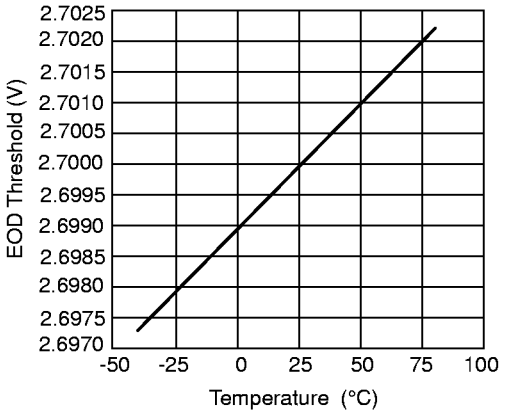


Figure 10. EOD Turn OFF Threshold vs. Temperature

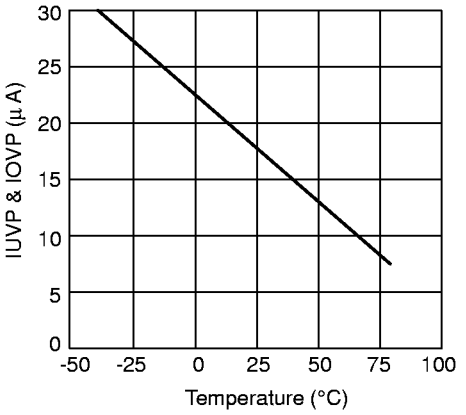
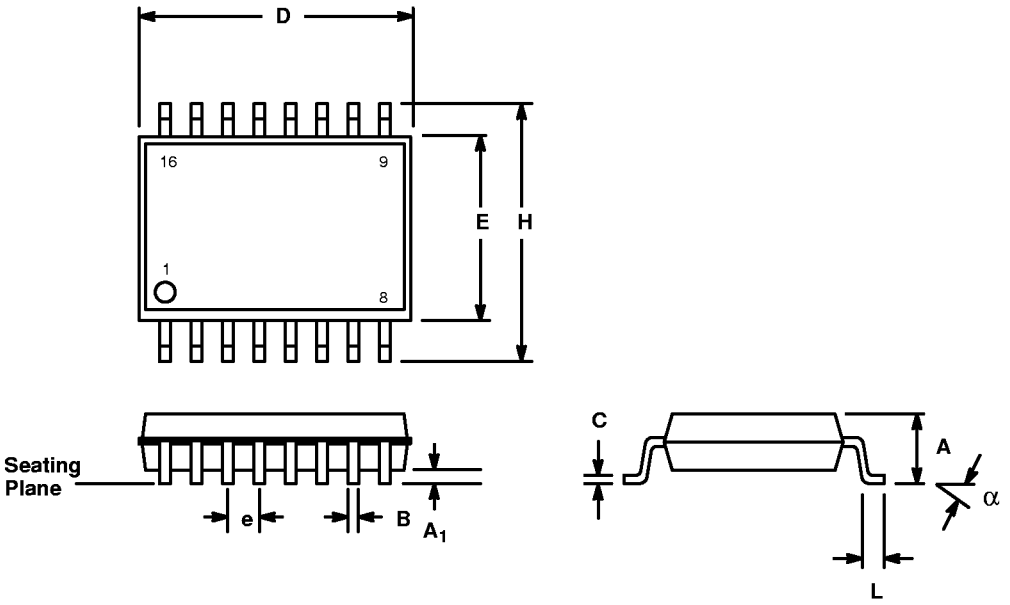


Figure 11. IUVP & IOVP vs. Temperature

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

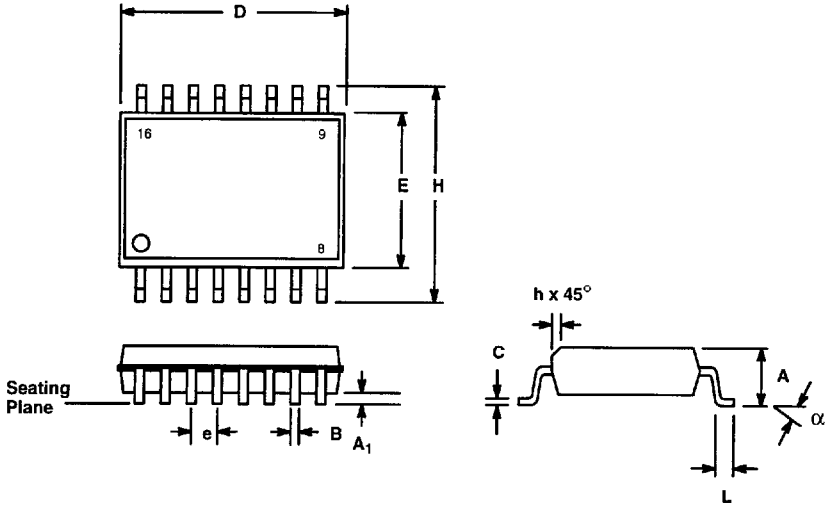
Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.46	2.64
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.482
C	0.0091	0.0125	0.231	0.318
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°