1.0 General Description

The AMIS-39101 is a robust high-side driver IC featuring eight independent high current output drive channels along with a number of integrated fault-protection circuits. This highly integrated product is designed for controlled delivery of power to a large variety of loads in industrial applications including motors, relays and LED arrays, among others. With all driver output channels in the conducting state, each channel can source up to 350mA of continuous current (resistive load). In cases where all output drivers are not active, higher output current per channel can be achieved provided that the thermal limits of the device are not exceeded. Furthermore, in order to minimize system cost each output driver has built-in fly-back diodes. The device withstands short-circuits to ground and supply, respectively. It is designed with an array of integrated protection features including over-temperature and over-current detection and shut down. The integrated charge pump requires only one external capacitor and provides for operation of the critical fault-protection circuitry even in case of low supply voltages. The device can be interfaced to a variety of microcontrollers via the serial peripheral interface (SPI) link, in turn allowing for monitoring and controlling the state of each of the output drivers individually. In this case, at the onset of a potential hazardous situation the drivers are switched off and the diagnostic state of the drivers can be extracted via the SPI interface. The device also features a power down mode for reduced power consumption and has high built-in electrostatic discharge (ESD) protection capability for robust operation.

2.0 Key Features

- Eight high-side output drivers
- Up to 830mA continuous current per driver pair (resistive load)
- Charge pump with one external capacitor
- SPI
- Short-circuit protection
- Diagnostic features
- Power-down mode
- Internal thermal shutdown
- 3.3V and 5V microcontroller compliant
- Excellent system ESD
- Automotive compliant
- SO28 package with low Rthja

3.0 Typical Applications

- Actuator control
- LED drivers
- Relays and solenoids
- Industrial process control
- Automotive load management

4.0 Ordering Information

Product Name	Package	Temperature Range
AMIS39101AGA	PSOP 300-28 (JEDEC MS-013)	-40°C…85°C

5.0 Block Diagram

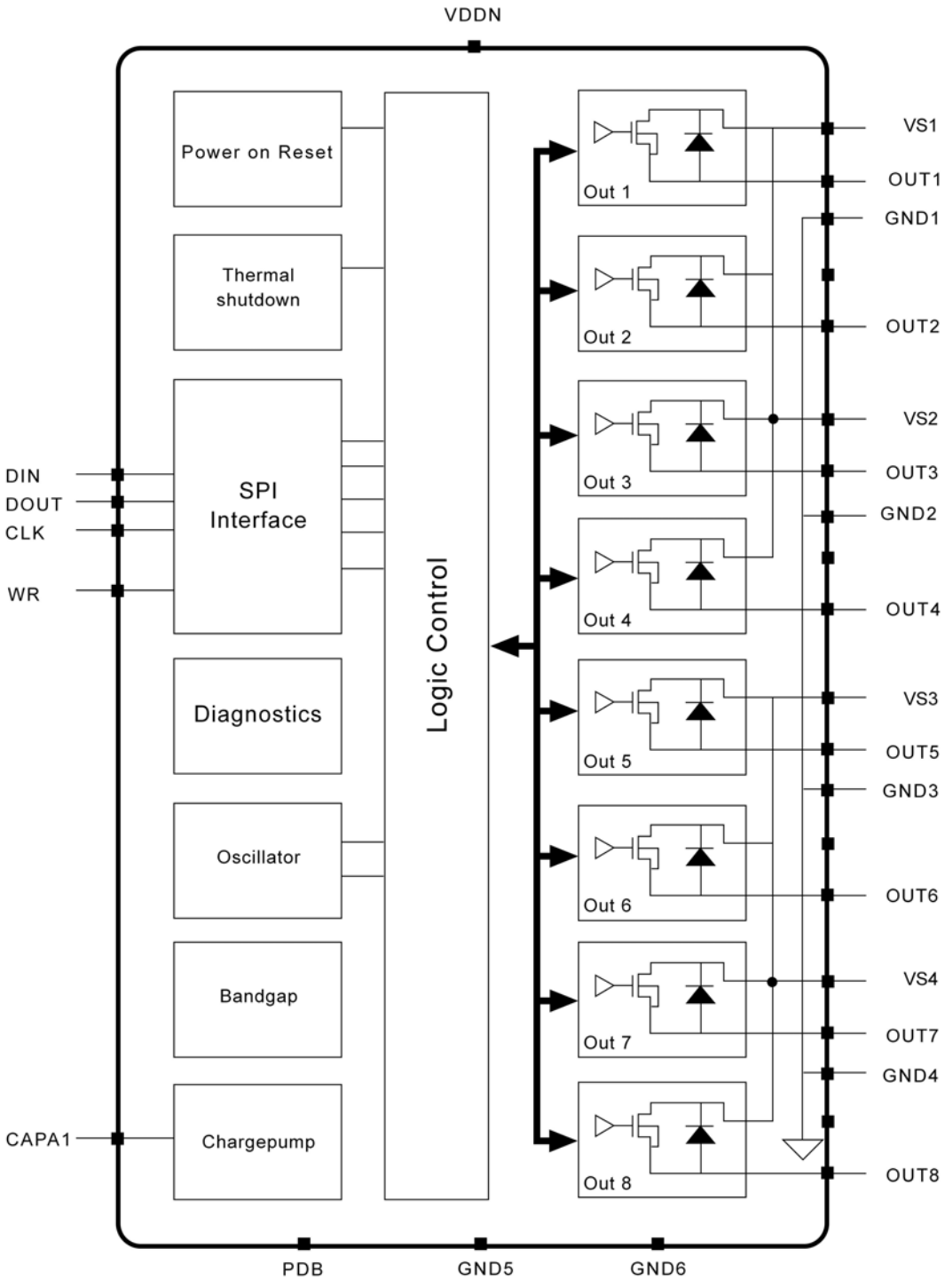


Figure 1: Block Diagram

6.0 Typical Application Diagram

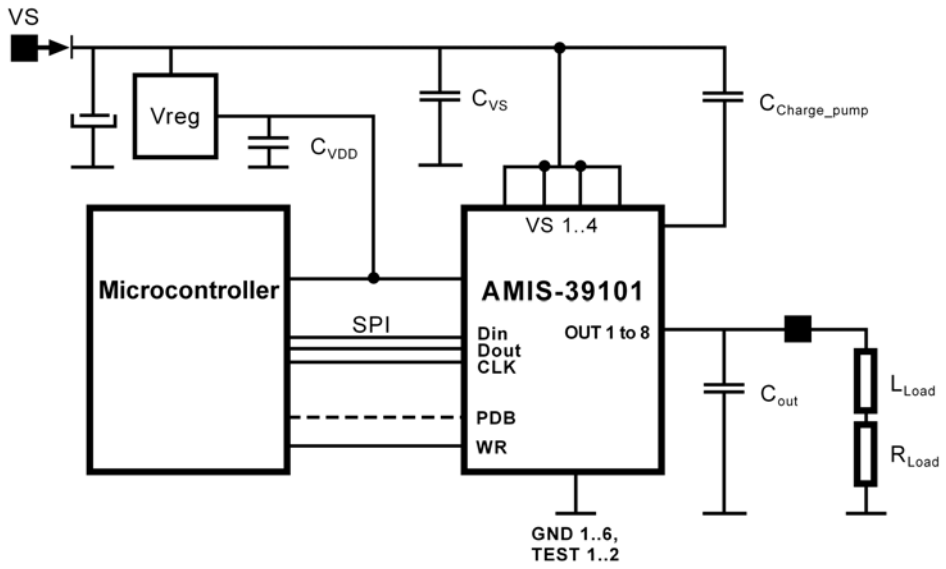


Figure 2: Typical Application Diagram

6.1 External Components

It is important to properly decouple the power supplies of the chip with external capacitors that have good high frequency properties.

The VS1, VS2, VS3, and VS4 pins are shorted on the PCB level. Also GND1, GND2, GND3, GND4, GND5, GND6, TEST, TEST1, and TEST2 are shorted on the PCB level.

Table 1: External Components

Component	Function	Min.	Value	Max.	Tol. [%]	Units
C_{VS}	Decoupling capacitor; X7R	100			± 20	nF
C_{charge_pump}	Charge pump capacitor(1)	0.47		47		nF
C_{out}(2)	EMC connector on connector	1				nF
C_{out}(2)	Decoupling capacitors; 50V	22			± 20	nF
C_{VDD}	Decoupling capacitors; 50V	22			± 20	nF
R_{Load}	Load resistance		65		± 10	Ω
L_{Load}	Load inductance at maximum current		300	350		mH

Notes:

(1) The capacitor must be placed close to the AMIS-39101 pins on the PCB.

(2) Both capacitors are optional and depend on the final application and board layout.

7.0 Pin Description

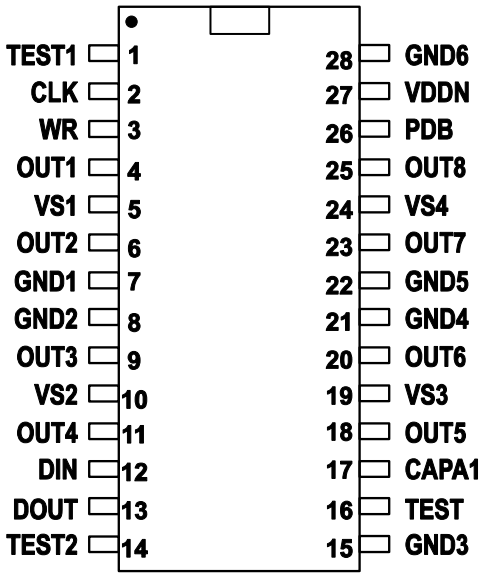


Figure 3: Pin Description of the AMIS-39101

Table 2: Pin Out

Pin	Name	Description
1	TEST1	Connect to GND
2	CLK	Schmitt trigger SPI CLK input
3	WR	Schmitt trigger SPI write enable input
4	OUT1	HS driver output
5	VS1	VS power supply
6	OUT2	HS driver output
7	GND1	Power ground and thermal dissipation path junction-to-PCB
8	GND2	Power ground and thermal dissipation path junction-to-PCB
9	OUT3	S driver output
10	VS2	VS power supply
11	OUT4	HS driver output
12	DIN	SPI input pin (Schmitt trigger or CMOS inverter)
13	DOUT	Digital three state output for SPI
14	TEST2	Connect to GND
15	GND3	Power ground and thermal dissipation path junction-to-PCB
16	TEST	Connect to GND
17	CAPA1	Charge pump capacitor pin
18	OUT5	HS driver output
19	VS3	VS power supply
20	OUT6	HS driver output
21	GND4	Power ground and thermal dissipation path junction-to-PCB
22	GND5	Power ground and thermal dissipation path junction-to-PCB
23	OUT7	HS driver output
24	VS4	VS power supply
25	OUT8	HS driver output
26	PDB	Schmitt trigger power-down input
27	VDDN	Digital supply
28	GND6	Power ground and thermal dissipation path junction-to-PCB

8.0 Electrical and Environmental Ratings

8.1 Absolute Maximum Ratings

Stress levels above those listed in this paragraph may cause immediate and permanent device failure. It is not recommended that more than one of these conditions be applied simultaneously.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VDDN	Power supply voltage	GND - 0.3	6	V
VS	VS power supply on pins VS1 to VS4, load dump, Pulse 5b 400ms	GND - 0.3	35	V
Iout_ON	Maximum output current OUTx pins(1) The HS driver is switched on	-3000	350	mA
Iout_OFF	Maximum output current OUTx pins(1) The HS driver is switched off	-350	350	mA
I_OUT_VS	Maximum output current VS1, 2, 3, 4 pins	-700	3750	mA
Vcapa1	DC voltage on pin CAPA1	0	VS+16.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	-0.3	VDDN+0.3	V
V_{ESD}	Pins that connect the application (pins VS1..4 and Out1..8)(2) All other pins(2)	-4 -2	+4 +2	kV kV
V_{ESD}	ESD according charged device model(3)	-750	+750	V
Tj	Junction temperature (T<100 hours)	-40	175	°C
Tmr	Ambient temperature under bias	-40	85	°C

Notes:

(1) The power dissipation of the chip must be limited not to exceed the maximum junction temperature Tj.
(2) According to HBM standard MIL-STD-883 method 3015.7.
(3) According to norm EOS/ESD-STM5.3.1-1999 robotic mode.

8.2 Thermal Characteristics

Table 4: Thermal Characteristics of the Package

Symbol	Description	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in power-SO28 package	In free air	145	K/W

Table 5: Thermal Characteristics of the AMIS-39101 on a PCB

PCB Design	Conductivity Top and Bottom Layer	Rthja (1)	Unit
Two layer (35um)	Copper planes according to Figure 4 + 25% copper for the remaining areas	24	K/W
Two layer (35um)	Copper planes according to Figure 4 + 0% copper for the remaining areas	53	K/W
Four layer JEDEC: EIA/JESD51-7	25% copper coverage	25	K/W
One layer JEDEC: EIA/JESD51-3	25% copper coverage	46	K/W

Note:

(1) These values are for general information purposes only, and will change based on each specific PCB design.

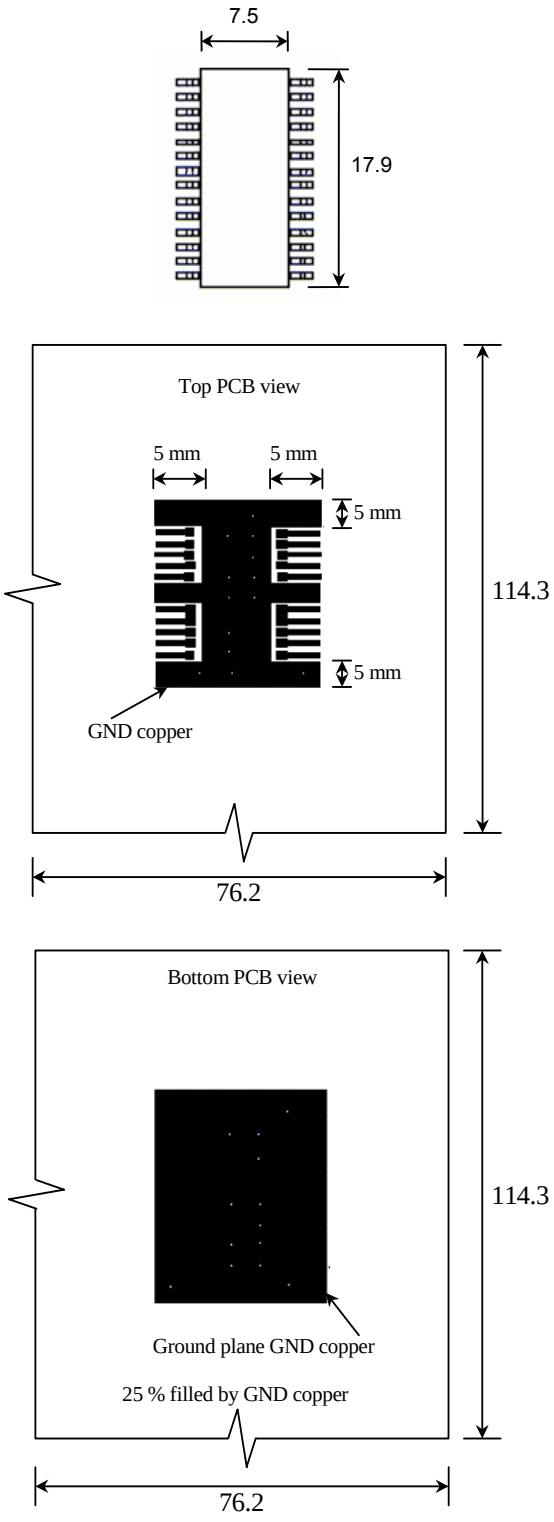


Figure 4: Layout Recommendation for Thermal Characteristics

8.3 Electrical Parameters

Operation outside the operating ranges for extended periods may affect device reliability. Total cumulative dwell time above the maximum operating rating for the power supply or temperature must be less than 100 hours.

The parameters below are independent from load type (see Section 8.4).

8.3.1. Operating Ranges

Table 6: Operating Ranges

Symbol	Description	Min.	Max.	Unit
VDDN	Digital power supply voltage	3.1	5.5	V
Vdig_in	Voltage on digital inputs CLK, PDB, WR, DIN	-0.3	VDDN	V
VS (1)	VS power supply on Pins VS1 to VS4	3.5	28	V
Tamb	Ambient temperature	-40	85	°C

Note:
(1) The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj of 130°C.

8.3.2. Electrical Characteristics

Table 7: Electrical Characteristics

Symbol	Description	Min.	Max.	Unit
I_VS_norm(1)	Consumption on VS without load currents In normal mode of operation PDB = high		3.5	mA
I_PDB_3.3(1)(2)	Sum of VS and VDDN consumption in power-down mode of operation PDB = low, VDDN 3.3V, VS = 24V, 23°C ambient CLK and WR are at VDDN voltage		25	µA
I_PDB_5(1)(2)	Sum of VS and VDDN consumption in power-down mode of operation PDB = low, VDDN 5V, VS = 24V, 23°C ambient CLK and WR are at VDDN voltage		40	µA
I_PDB_MAX_VS	VS consumption in power-down mode of operation PDB = low, VS = 28V		10	µA
I_VDDN_norm(1)	Consumption on VDDN In normal mode of operation PDB = high CLK is 500kHz, VDDN = 5.5V, VS = 28V		1.6	mA
R_on_1..8	On resistance of the output drivers 1 through 8 t VS= 24V (nominal VS power supply condition) t VS = 4.6V (worst case VS power supply condition)		 1 3	 Ω Ω
I_OUT_lim_x(1)	Internal over-current limitation of HS driver outputs	0.65	2	A
T_shortGND_HSdoff	The time from short of HS driver OUTx pin to GND and the driver deactivation; driver is Off Detection works from VS minimum of 7V VDDN minimum is 3V	5,4		µs
TSD_H (1)	High TSD threshold for junction temperature (temperature rising)	130	170	°C
TSD_HYST	TSD hysteresis for junction temperature	9	18	°C

Notes:
(1) The power dissipation of the chip must be limited not to exceed maximum junction temperature Tj.
(2) The cumulative operation time mentioned above may cause permanent device failure.

8.4 Load Specific Parameters

High-side driver parameters for specific loads are specified in following categories:

A. Parameters for inductive loads up to 350mH and $T_{ambient}$ up to 85°C
B. Parameters for inductive loads up to 300mH and $T_{ambient}$ up to 85°C
C. Parameters for resistive loads and $T_{ambient}$ up to 85°C

Table 8: Load Specific Characteristics

Symbol	Description	Min.	Max.	Unit
A. Inductive Load up to 350mH and $T_{ambient}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		240	mA
B. Inductive Load up to 300mH and $T_{ambient}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		275	mA
C. Resistive Load and $T_{ambient}$ up to 85°C				
I_OUT_ON_max.	Maximum output per HS driver, all eight drivers might be active simultaneously		350	mA
	Maximum output per one HS driver, only one can be active		650	mA
	Maximum output per HS driver, only two HS drivers from a different pair can be active simultaneously		500	mA
	Maximum output per one HS driver pair		830	mA

Note: The parameters above are not tested in production but are guaranteed by design. The overall current capability limitations need to be respected at all times.

The maximum current specified in Table 8 cannot always be obtained. The practically obtainable maximum drive current heavily depends on the thermal design of the application PCB (see Section 8.2).

The available power in the package is: (TSD_H - T_ambient) / Rthja

With TSD_H = 130°C and Rthja according to Table 5.

8.5 Charge Pump

The high-side drivers use floating NDMOS transistors as power devices**.** To provide the gate voltages for the NDMOS of the high-side drivers, a charge pump is integrated. The storage capacitor is an external one. The charge pump oscillator has typical frequency of 4MHz.

8.6 Diagnostics

8.6.1. Short Circuit Diagnostics

The diagnostic circuit in the AMIS-39101 monitors the actual output status at the pins of the device and stores the result in the diagnostic register which is then latched in the output register at the rising edge of the WR-pin. Each driver has its corresponding diagnostic bit DIAG_x. By comparing the actual output status (DIAG_x) with the requested driver status (CMD_x) you can diagnose the correct operation of the application according to Table 9.

8.6.2. Thermal Shutdown (TSD) Diagnostic

In case of TSD activation, all bits DIAG 1 to DIAG 8 in the SPI output register are set into the fault state and all drivers will be switched off (see Table 9).

The TSD error condition is active until it is reset by the next correct communication on SPI interface (i.e. number of clock pulses during WR=0 is divisible by 8), provided that the device has cooled down under the TSD trip point.

Table 9: OUT Diagnostics

Requested Driver Status	CMD_x	Actual Output Status	DIAG_x	Diagnosis
On	1	High	1	Normal state
On	1	Low	0	Short to ground or TSD(2)
Off	0	High	1	Short to VS or missing load(1) or TSD(2)
Off	0	Low	0	Normal state(1)

Notes:
(1) The correct diagnostic information is available after T_diagnostic_OFF time.
(2) All 8 diagnostic bits DIAG_x must be in the fault condition to conclude a TSD diagnostic.

8.6.3. Ground Loss

Due to its design, the AMIS-39101 is protected for withstanding module ground loss and driver output shorted to ground at the same time.

8.6.4. Power Loss

Table 10: Power Loss

VDDN	VS	Possible Case	Action
0	0	System stopped	Nothing
0	1	Start case or sleeping mode with missing VDDN	Eight switches in the off-state Power down consumption on VS
1	0	Missing VS supply VDDN normally present	Eight switches in the off-state Normal consumption on VDDN
1	1	System functional	Nominal functionality

8.7 SPI interface

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. The AMIS-39101 acts always as a slave and it can't initiate any transmission.

8.7.1. SPI Transfer Format and Pin Signals

The SPI block diagram and timing characteristics are shown in Figure 6 and Figure 7.

During an SPI transfer, data is simultaneously sent to and received from the device. A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DIN and DOUT). DOUT signal is the output from the AMIS-39101 to the external MCU and DIN signal is the input from the MCU to the AMIS-39101. The WR-pin selects the AMIS-39101 for communication and can also be used as a chip select (CS) in a multiple-slave system. The WR-pin is active low. If AMIS-39101 is not selected, DOUT is in high impedance state and it does not interfere with SPI bus activities. Since AMIS-39101 always shifts data out on the rising edge and samples the input data also on the rising edge of the CLK signal, the MCU SPI port must be configured to match this operation. SPI clock idles high between the transferred bytes.

The diagram in Figure 7 represents the SPI timing diagram for 8-bit communication.

Communication starts with a falling edge on the WR-pin which latches the status of the diagnostic register into the SPI output register. Subsequently, the CMD_x bits – representing the newly requested driver status – are shifted into the input register and simultaneously, the DIAG_x bits – representing the actual output status – are shifted out. The bits are shifted with x=1 first and ending with x=8. At the rising edge of the WR-pin, the data in the input register is latched into the command register and all drivers are simultaneously switching to the newly requested status. SPI communication is ended.

In case the SPI master does only support 16-bit communication, then the master must first send 8 clock pulses with dummy DIN data and ignoring the DOUT data. For the next 8 clock pulses the above description can be applied.

The required timing for serial to peripheral interface is shown in Table 11.

Table 11: Digital Characteristics

Symbol	Description	Min.	Max.	Unit
T_CLK	Maximum applied clock frequency on CLK input		500	kHz
T_DATA_ready	Time between falling edge on WR and first bit of data ready on DOUT output (driver going from HZ state to output of first diagnostic bit)		2	µs
T_CLK_first	First clock edge from falling edge on WR	3		µs
T_setup(1)	Setup time on DIN	20		ns
T_hold(1)	Hold time on DIN	20		ns
T_DATA_next	Time between rising edge on CLK and next bit ready on DOUT (capa on DOUT is 30pF max.)		100	ns
T_SPI_END	Time between last CLK edge and WR rising edge	1		µs
T_risefall	Rise and fall time of all applied signals (maximum loading capacitance is 30pF)	5	20	ns
T_WR	Time between two rising edge on WR (repetition of the same command)	300		µs

Note:
(1) Guaranteed by design

Normal mode verification:

- The *command* is the set of eight bits loaded via SPI, which drives the eight HS drivers on or off.
- The *command* is activated with rising edge on WR pin.

Table 12: Digital Characteristics

Symbol	Description	Min.	Max.	Unit
T_command_L_max.(1)	Minimum time between two opposite commands for inductive loads and maximum HS driver current of 275mA	1		s
T_command_R(1)	Minimum time between two opposite commands for resistive loads and maximum HS driver current of 350mA	2		ms
T_PDB_recov	The time between the rising edge on the PDB input and 90 percent of VS-1V on all HS driver outputs. (all drivers are activated, pure resistive load 35mA on all outputs)		1	ms

Note:
(1) Guaranteed by design

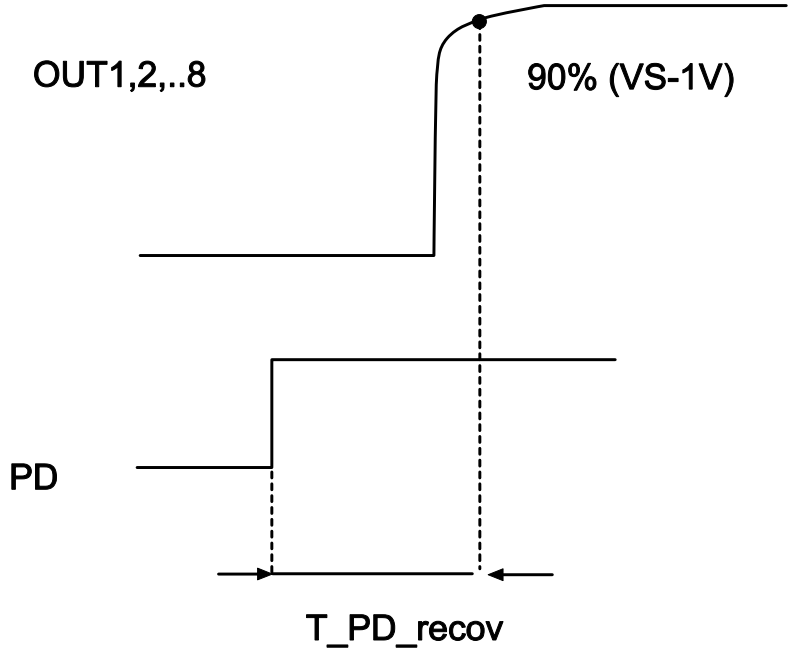


Figure 5: Timing for Power-down Recovery

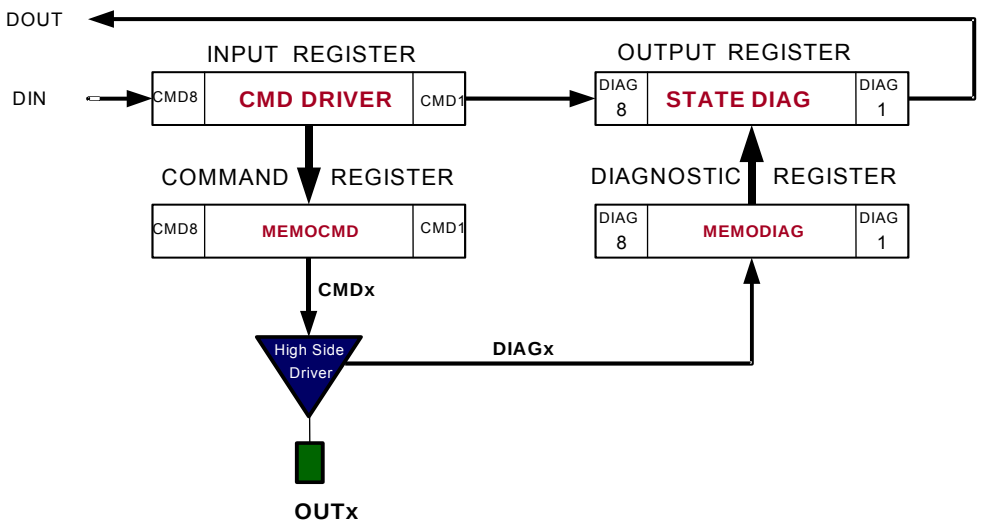


Figure 6: SPI Block Diagram

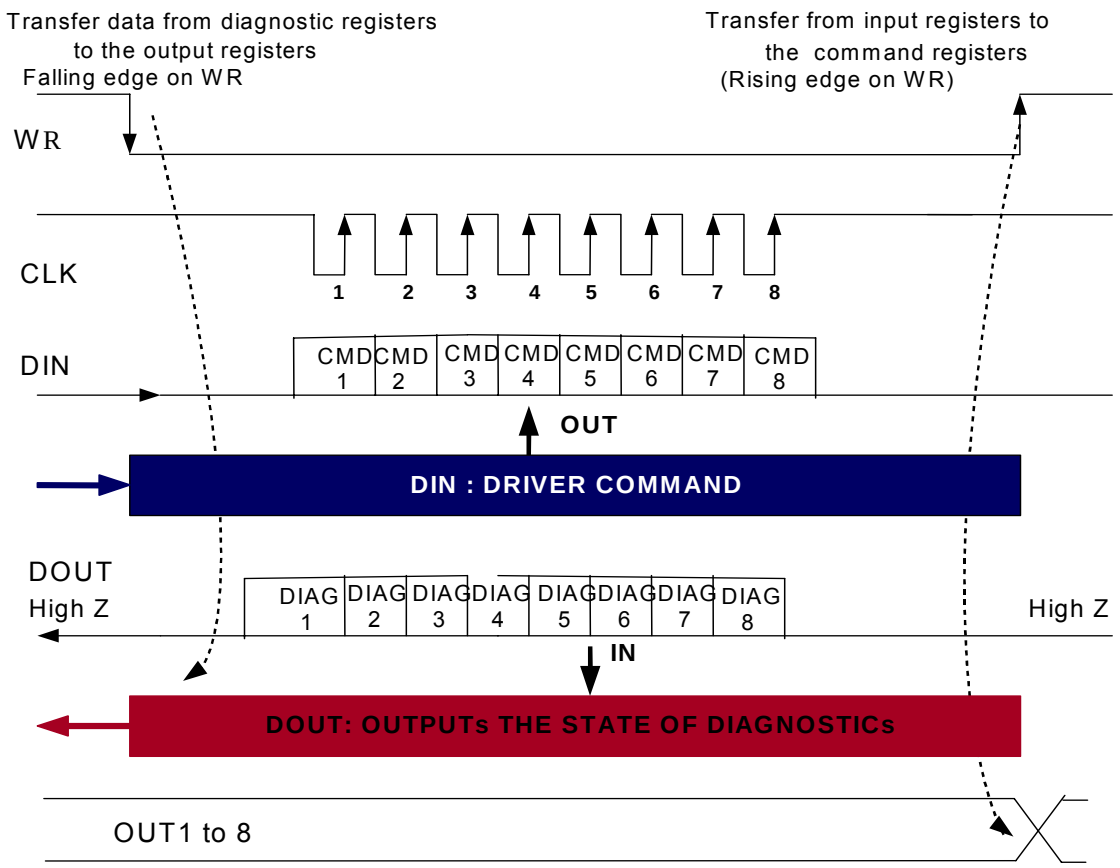
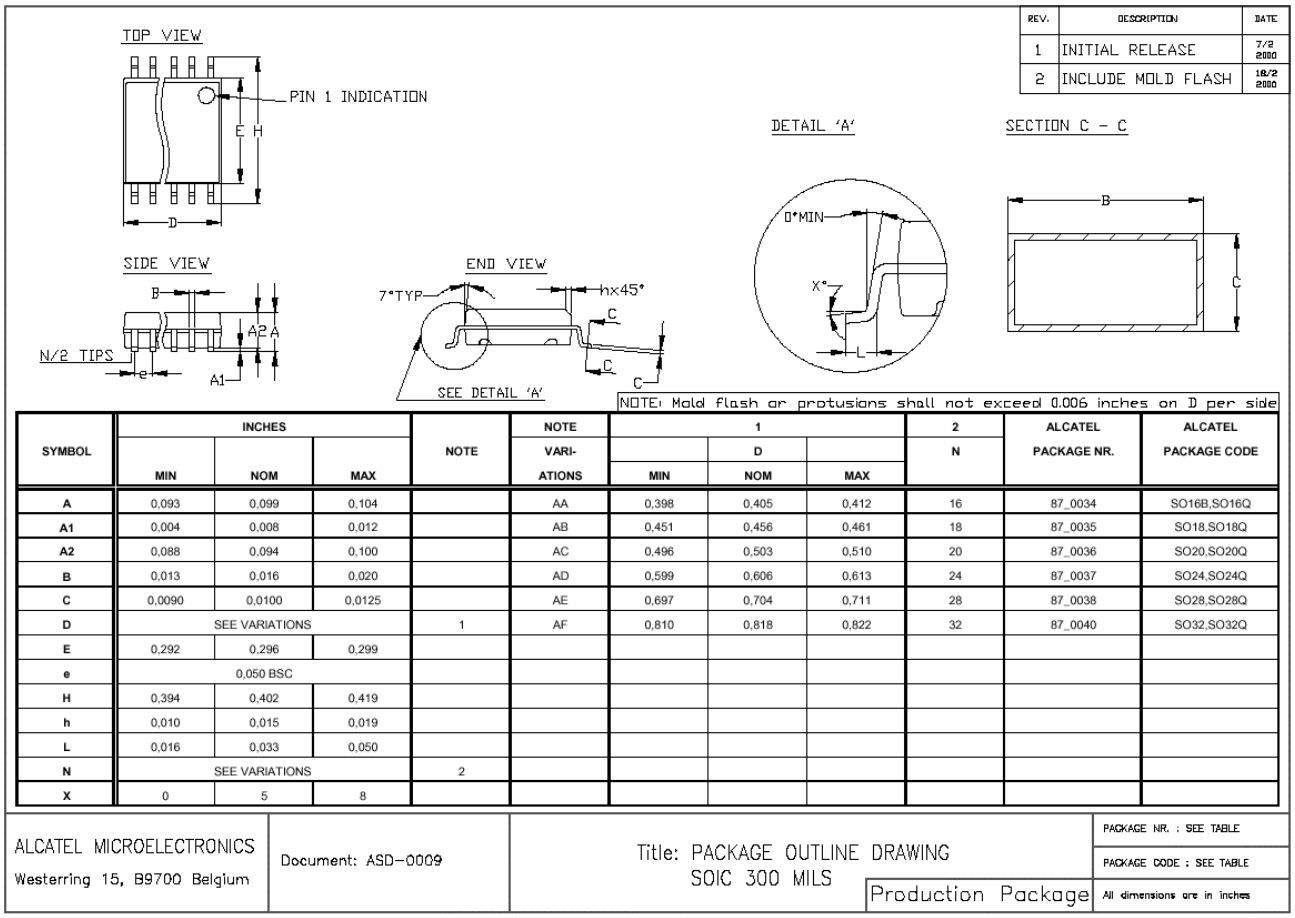


Figure 7: Timing Diagram

9.0 Assembly and Delivery



REV.	DESCRIPTION	DATE
1	INITIAL RELEASE	7/2 2000
2	INCLUDE MOLD FLASH	10/2 2000

SYMBOL	INCHES MIN	INCHES NOM	INCHES MAX	NOTE	NOTE VARI-ATIONS	1 D MIN	1 D NOM	1 D MAX	2 N	ALCATEL PACKAGE NR.	ALCATEL PACKAGE CODE
A	0,093	0,099	0,104		AA	0,398	0,405	0,412	16	87_0034	SO16B,SO16Q
A1	0,004	0,008	0,012		AB	0,451	0,456	0,461	18	87_0035	SO18,SO18Q
A2	0,088	0,094	0,100		AC	0,496	0,503	0,510	20	87_0036	SO20,SO20Q
B	0,013	0,016	0,020		AD	0,599	0,606	0,613	24	87_0037	SO24,SO24Q
C	0,0090	0,0100	0,0125		AE	0,697	0,704	0,711	28	87_0038	SO28,SO28Q
D	SEE VARIATIONS			1	AF	0,810	0,818	0,822	32	87_0040	SO32,SO32Q
E	0,292	0,296	0,299								
e	0,050 BSC										
H	0,394	0,402	0,419								
h	0,010	0,015	0,019								
L	0,016	0,033	0,050								
N	SEE VARIATIONS			2							
X	0	5	8								

Figure 8: Package Outline Drawing

For detailed mechanical data, please refer to the AMIS Packaging Handbook; (http://www.amis.com/tech_resources/packaging/index.html), specification number 16505.

10.0 Quality and Reliability

A quality system with certification against TS16949 is maintained.

An AEC-Q100 compatible product qualification is performed. Monitoring of production is performed according to the dedicated AMIS specifications for assembly and wafer fabrication.

All products are tested using a production test program. Lot conformance to specification in volume production is guaranteed by means of following quality conformance tests:

Table 13: Qualification

QC Test	Conditions	AQL Level	Inspection Level
Electrical functional and parametric	To product data sheet	0.04	II
External visual (mechanical)	Physical damage to body or leads (e.g. bent leads) Dimensions affecting PCB manufacturability (e.g. coplanarity)	0.15	II
External visual (cosmetic)	Correctness of marking All other cosmetic defects	0.65	II

Each production lot will be accompanied with a Certificate of Conformance.

11.0 Revision History

Table 14: Revision History

Revision	Date	Description
0.1	Various	Initial document

12.0 Company or Product Inquiries

For more information about AMI Semiconductor's products or services visit our Web site at http://www.amis.com.