Very High Accuracy, Low Noise, Sample-and-Hold Amplifier

Designed for High Resolution Data Acquisition Applications

Introduction

The SHA2410 is a high performance hybrid sample-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time of 2.5 µs to ±0.0015%, very low aperture jitter of 200 ps, and low feedthrough of 100 dB make it suitable for use with fast 16-bit A/D converters that digitize signals up to 50 kHz. Accepting a bipolar ±5 volt input, the SHA2410 has very low noise, 20 µV RMS, making it an ideal choice for applications requiring 100 dB dynamic range, such as professional audio and nuclear research. In most other open-loop sample-and-hold amplifiers, the linearity is limited by the hold switch performance. The SHA2410 incorporates a unique pedestal compensation circuit to reduce the effects of the hold switch to ±0.003% maximum.

The SHA2410 also features a low droop rate of 0.3 µV/µs, making it particularly well suited for slower high resolution systems. In the hold mode, the SHA2410 will hold an input signal to ±0.0015% of full scale for 500 µs.

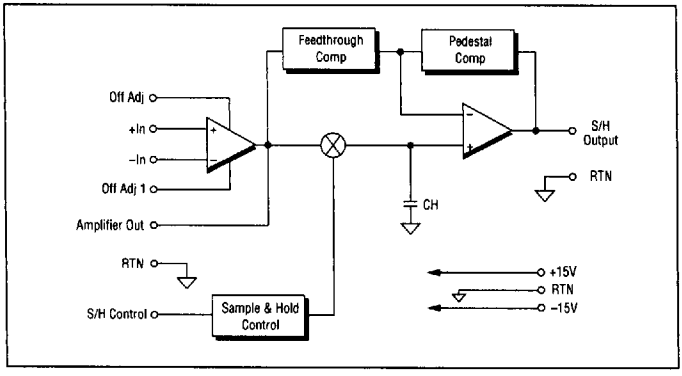
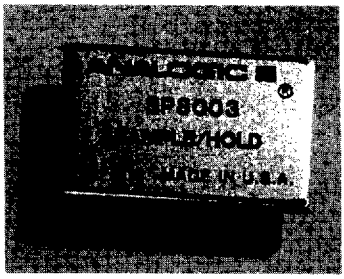


Figure 1. SHA2410 Simplified Block Diagram.



Features

- ❑ Fast Acquisition (2.5 µs)
- ❑ Low Aperture Uncertainty (200 ps RMS)
- ❑ Low Noise (20 µV RMS)
- ❑ Low Feedthrough (–100 dB at 25 kHz)
- ❑ Excellent Linearity (±0.0015%)
- ❑ Low Input Capacitance (5 pF)
- ❑ Low Droop Rate (0.3 µV/µs)
- ❑ Ease-of-Use
- ❑ 14-Pin Hybrid Package

Applications

- ❑ Wideband Data Acquisition Systems
- ❑ Professional Audio
- ❑ Telecommunications
- ❑ Automatic Test Equipment
- ❑ Industrial Process Control
- ❑ Nuclear Research

4

SHA2410/SP8003

Specifications[1]

ANALOG INPUT

Input Range
±10V [4], ±5V Min. [2]

Input Bias Current
1500 nA Max.

Input Capacitance
5 pF

Input Impedance
10 kΩ

CONTROL INPUT

Logic "0" (Sample)
–0.5V Min., 0.8V Max.

Logic "1" (Hold)
2.5V Min., +5.5V Max.

Required Rise Time
10 ns Max. for Min. Aperture Time

DYNAMIC CHARACTERISTICS

Acquisition Time, Non-Inverting
2.5 µs Max. to ±0.0015% of 10V Input Step

Inverting
2.5 µs Max. to ±0.0015% of 10V Input Step

Sample-to-Hold Transient Settling Time
500 ns Max. to ±0.0015%

Output Slew Rate
10V/µs

Pedestal
±10 mV Max.

Aperture Delay
25 ns

Aperture Uncertainty
200 ps (RMS)

Full Power Bandwidth
150 kHz

Small Signal Bandwidth
2 MHz

Droop Rate
0.02 µV/µs Typ., 0.3 µV/µs Max.

Feedthrough —10 Vp-p at 500 kHz
–100 dB

TRANSFER CHARACTERISTICS

Gain
+1 ±0.005% Typ., ±0.01% Max.

Nonlinearity
±0.0015% Typ., ±0.003% Max.

Offset Error
±5 mV (Adjustable to zero)

Noise (Sample Mode) DC to 1 MHz
20 µV (RMS) Max.

Noise (Hold Mode) DC to 1 MHz
35 µV (RMS) Max.

Output Voltage
±5V Min., ±10V Min.[4]

Maximum Load
2 kΩ Min. || 100 pF Max.

Dielectric Absorption
±0.005% of Voltage Change

STABILITY (0°C TO 70°C)

Offset Drift
50 µV/°C Max.

Droop Rate
Doubles every 10°C

Warm-Up Time
1 minute

POWER REQUIREMENTS [3]

±15V Supplies
14.5V Min., 15.5V Max.

+15V Current Drain
15 mA Typ., 18 mA Max.

–15V Current Drain
15 mA Typ., 18 mA Max.

Power Consumption
450 mW Typ., 540 mW Max.

Power Supply Rejection Ratio
100 µV/% Max.

ENVIRONMENTAL & MECHANICAL

Temperature Range Rated Performance
0° to 70°C

Storage
–25°C to 85°C

Relative Humidity
0 to 85% non-condensing up to 70°C

Dimensions
0.8" x 0.5" x 0.2" (14-pin DIP)
(20.32 mm x 12.7 mm x 5.08 mm)

NOTES:

1. All specifications guaranteed at 25°C and ±15V supplies unless otherwise noted.
2. Absolute maximum input range without damage is ±15V.
3. It is possible to use power supplies from ±12V to ±18V. Consult factory.
4. For ±10V requirements, specify model number SP8003.
5. For a discussion of how to determine the overall throughput rate for the S/H and A/D converter, refer to page 156 of the Analogic Data Conversion Systems Digest.
6. The derivation of this formula is shown on page 154 of the *Analogic Data Conversion Systems Digest.*

Specifications subject to change without notice.

System Considerations

Sample-and-hold amplifiers are often used to sample many channels at the same instant in time, such as in seismic data acquisition, and to reduce the time uncertainty (and resultant amplitude error) when digitizing fast time-varying signals. Practical systems have inherent finite sampling apertures; however, the SHA2410 minimizes this time to an aperture uncertainty of 200 ps. Figure 2 illustrates the typical timing of the SHA2410 [5]. If a system uses an A/D converter without a sample-and-hold, the time uncertainty is the conversion time of the A/D converter, which is several orders of magnitude longer than the S/H's aperture uncertainty.

A sample-and-hold is required for a particular A/D conversion application if the input signal is changing fast enough so that the input to the A/D converter changes by more than one LSB during the conversion time. For a sinusoidal signal, the calculation [6] is straightforward:

$$FMax = \frac{LSB}{(\text{Full Scale Range})\ (2\pi)\ (\text{A/D Conversion Time})}$$

FMax represents the maximum allowable input frequency.

For example, with a 16-bit A/D converter that has a conversion time of 17 µs and a 20V full scale range, the maximum signal input frequency without a sample-and-hold would be:

$$FMax = \frac{20V/(2^{16})}{(20V)\ (2\pi)\ (17\ \mu s)} = 0.143\ Hz$$

Based on this analysis it is clear that all 16-bit applications would require a sample-and-hold.

By using the SHA2410 sample-and-hold the maximum signal frequency increases dramatically. In applications that use a sample-and-hold, the S/H aperture uncertainty replaces the A/D conversion time in the previous equation:

$$FMax = \frac{20V/(2^{16})}{(20V)\ (2\pi)\ (200\ ps)} = 12.1\ MHz$$

Bypass Capacitor

Two 6.8 µF tantalum bypass capacitors should be installed close to the SHA2410, between +15V and analog ground and between –15V and analog ground.

Adjustments

The SHA2410 allows the input offset error to be externally nulled to zero by connecting a 100 kΩ potentiometer across Pins 14 and 13 as shown in Figure 5. To adjust the offset voltage, place the SHA2410 in the sample mode, short Pins 1 and 6, and set the offset potentiometer such that the output of the S/H is 0V.

The gain of the SHA2410 is typically within ±0.0015% of the nominal ±5V output. This small gain error of the sample-and-hold can be compensated via the gain adjustment potentiometer on the A/D converter following the SHA2410.

Principles of Operation

As shown in Figure 1, the SHA2410 sample-and-hold amplifier uses an open-loop configuration. The advantage to the open-loop topology is that it achieves a faster acquisition time at a lower cost than other configurations. In Figure 1, it can also be seen that the SHA2410 includes a pedestal compensation circuit, which compensates for the nonlinearity of the switches and amplifiers. Additionally, a feed-through compensation circuit has been added so that true 16-bit performance can be achieved in dynamic systems.

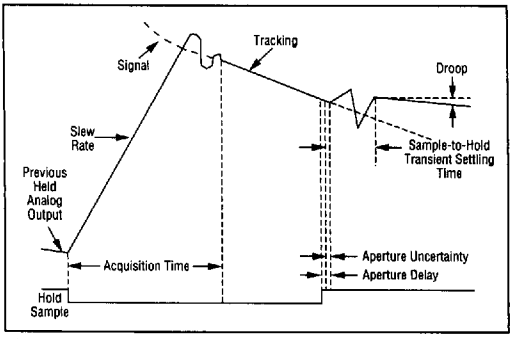


Figure 2. SHA2410 Timing Diagram.

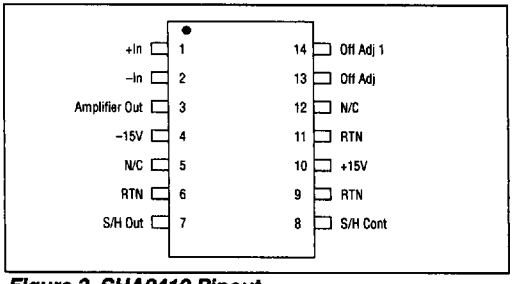


Figure 3. SHA2410 Pinout.

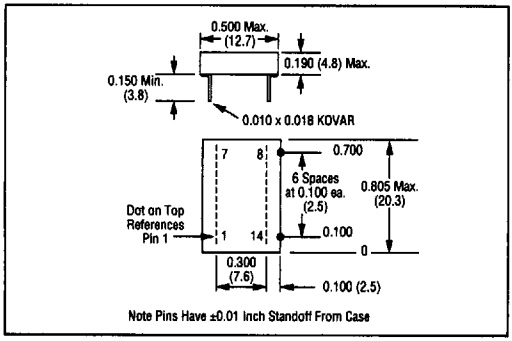


Figure 4. SHA2410 Mechanical Outline.

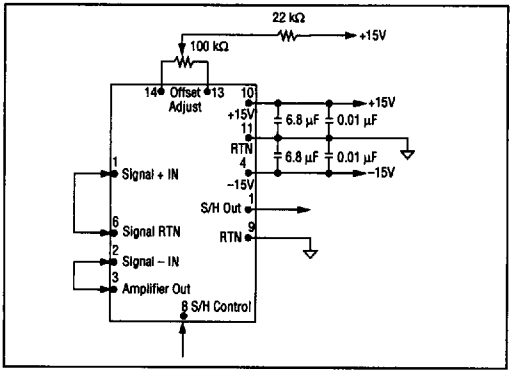


Figure 5. Offset Adjustment.

Applications

The SHA2410 can be used with any user-defined feedback network to provide any desired gain in the sample mode. As shown in Figure 1, the input amplifier is uncommitted to provide the utmost applications versatility. The most common application of the SHA2410 will utilize the connection diagrammed in Figure 6A. In this mode of operation, the SHA2410 will operate as a unity-gain non-inverting amplifier.

The input amplifier has a very high open-loop gain to ensure that gain nonlinearity will be minimized in applications where a gain other than one is utilized. The SHA2410 in a non-inverting gain configuration, as diagrammed in Figure 6B, has a transfer function of 1 + R2/R1 in the sample mode. In the inverting configuration, diagrammed in Figure 6C, the transfer function of the SHA2410 is equal to –R2/R1 when sampling. In the inverting and non-inverting configurations where external resistors are used to set the desired gain, care must be taken to select the appropriate resistor type. Both the initial gain accuracy and gain drift over temperature are functions of the type and matching characteristics of the resistors.

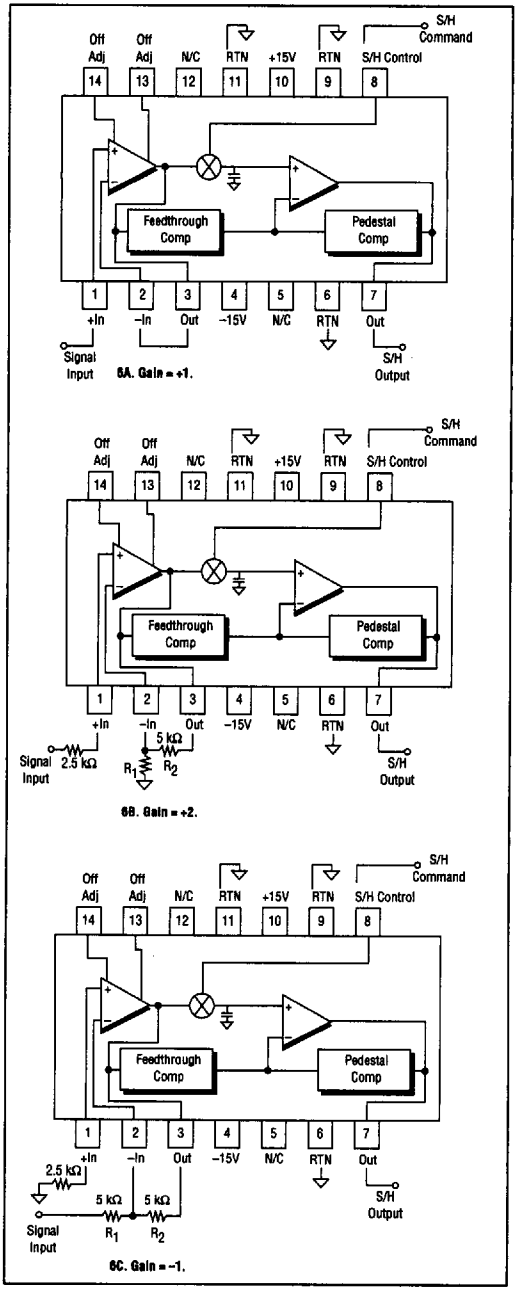


Figure 6. SHA2410 Connection Diagram.

Ordering Guide

High Speed S/H Amplifier 14-Pin DIP	
SHA2410	±5V Input
SP8003	±10V Input