NEL

MD-01-4-43-75-482
May 8, 2002
Preliminary

MC740-430E
47-Gb/s 4:1 Multiplexer

The MC740-430E is an engineering sample of 47-Gb/s signal generator. It consists of a 4:1 multiplexer (MUX), D-type flipflop (D-FF), and clock distribution unit based on 0.1-μm InP-HEMT devices. Four-parallel data inputs are multiplexed to 47-Gb/s data by using 47- and 11.75-GHz clock signals. At the output stage, the D-FF regenerates the muliplexed data with the 47-GHz clock signal and offers symmetrical eye openings. The MC740-430E has SCFL (Source Coupled FET Logic) I/O and can be directly connected to a pulse pattern generator.

FEATURES

Operating range: 38 to 47 Gb/s (min.) (note)
Signal regeneration with full-rate clock signal
Large output amplitude: SCFL I/O (V_{OHD} = 0V, V_{OLD} = -0.9V, typ.)
Single power supply voltage: DC -6 V

(note) 50-Gb/s operation is optional.

APPLICATIONS

Parallel-to-serial converters, Test equipments

FUNCTION DIAGRAM

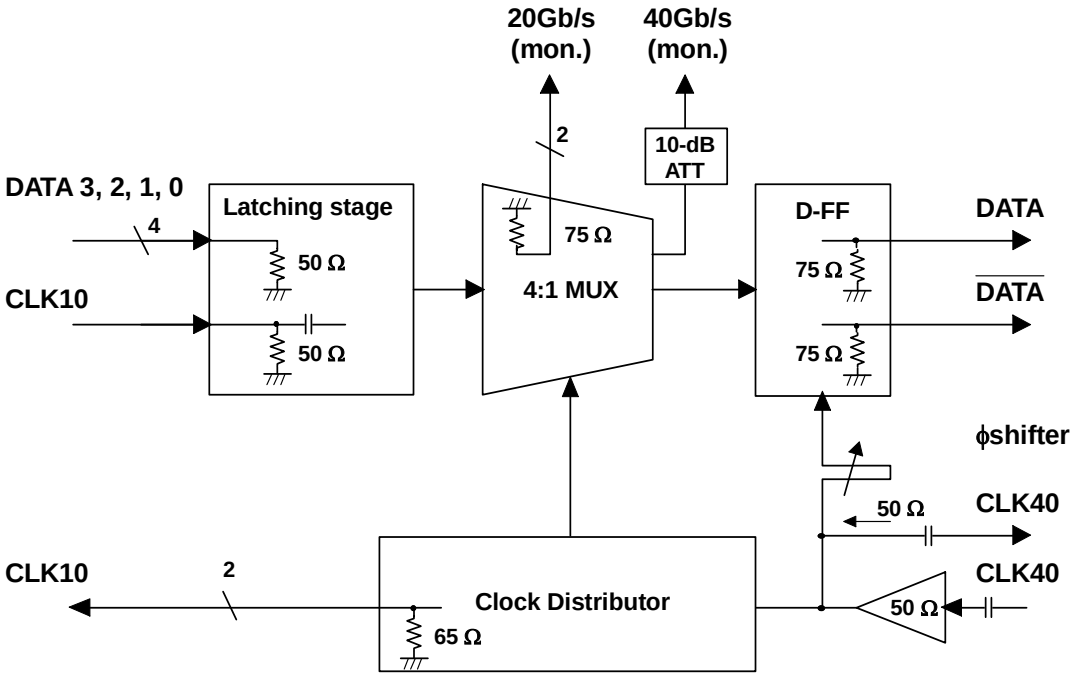
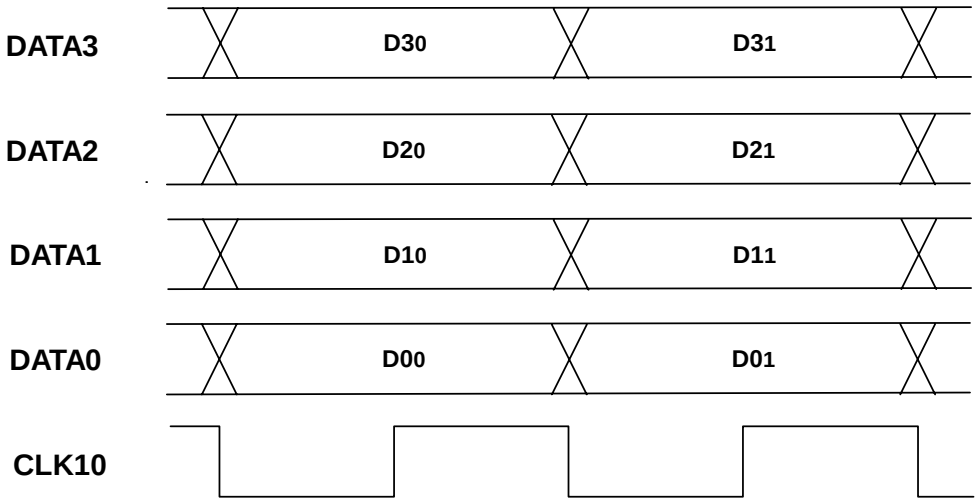


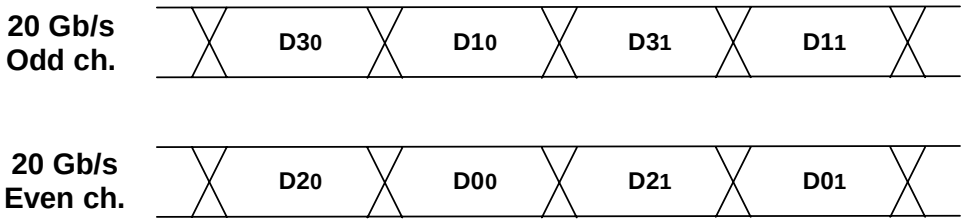
Fig. 1. Function diagram.

TIMING CHARTS

(1) Data and Clock Input Signals



(2) Multiplexed 20 Gb/s Data Output Signals (Monitor)



(3) Multiplexed 40 Gb/s Data Output Signals

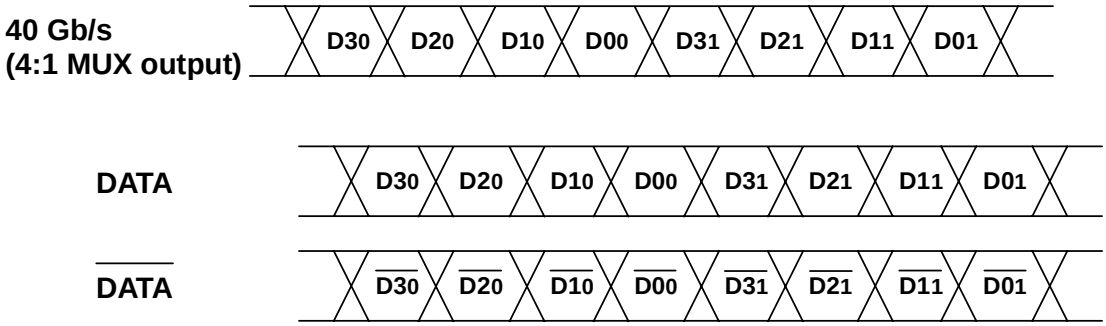


Fig. 2. Timing charts.

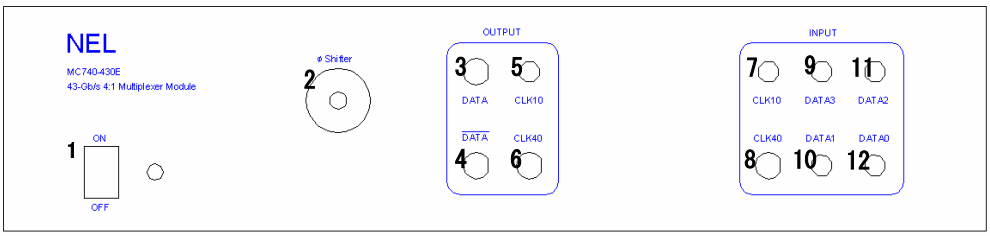
CONNECTION TABLE

No.	NAME	FUNCTION	TERM-INAL	No.	NAME	FUNCTION	TERM-INAL
1	Front Switch	Front Switch	-	13	20Gb/s Even	20G Monitor (Even ch., DATA2 and 0)	K(f) (2)
2	ϕshifter	Clock Phase Shifter for D-FF	-	14	20Gb/s Odd	20G Monitor (Odd ch., DATA3 and 1)	K(f) (2)
3	DATA	Data Output	V(f) (1)	15	CLK10	1/4 Clock Output	SMA(f)
4	/DATA	Data Output (complement)	V(f) (1)	16	40Gb/s	40G Monitor (4:1 MUX Output)	V(f) (1)
5	CLK10	1/4 Clock Output	SMA(f)	17	PWR	Power Supply (-6.0 V)	-
6	CLK40	Clock Output	V(f) (1)	18	GND	Ground (0.0 V)	-
7	CLK10	1/4 Clock Input	SMA(f)	19	Main Switch	Main Switch	-
8	CLK40	Clock Input	V(f) (1)				
9	DATA3	Data Input 3	SMA(f)				
10	DATA1	Data Input 1	SMA(f)				
11	DATA2	Data Input 2	SMA(f)				
12	DATA0	Data Input 0	SMA(f)				

notes) (1) V: Anritsu panel adaptor V232
(2) K: Anritsu panel adaptor K232B

CONNECTION DIAGRAM

FRONT PANEL



REAR PANEL

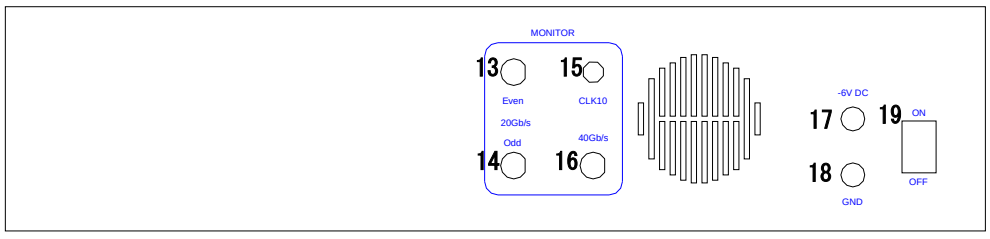


Fig. 3. Front and rear panels.

Case dimension (without connectors)
height: 95 mm
width: 370 mm
depth: 235 mm

ABSOLUTE MAXIMUM RATINGS

GENERAL

SYMBOL	PARAMETER	Ratings
V_{PWR}	Power Supply Voltage	TBD
Tstor	Storage Temperature	TBD

DATA and CLOCK INPUT SIGNALS

SYMBOL	PARAMETER	Ratings
DATA3 to 0	Applied Voltage at DATA3 to 0	-1.9 to 0 V
V_{ICLK40}	Applied Voltage at CLK40	-1.6 to +1.6 V (DC), 1.6 Vpp (AC)
V_{ICLK10}	Applied Voltage at CLK10	-1.6 to +1.6 V (DC), 1.6 Vpp (AC)

DATA and CLOCK OUTPUT SIGNALS

SYMBOL	PARAMETER	Ratings
$V_{DATA, /DATA}$	Applied Voltage at DATA, /DATA	TBD
V_{OC40}	Applied Voltage at CLK40	-1.2 to 1.2 V (DC), No RF Input
V_{OC10}	Applied Voltage at CLK10	-1.75 to +0.2 V

MONITOR OUTPUT SIGNALS

SYMBOL	PARAMETER	Conditions
40Gb/s	40-Gb/s Monitor Output Interface	TBD
20Gb/s (odd, even)	20-Gb/s Monitor Output Interface	-1.75 to +0.2 V
CLK10	10-GHz Clock Output Interface	-1.75 to +0.2 V

RECOMMENDED OPERATING CONDITIONS

GENERAL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{PWR} (note1)	Power Supply Voltage		-6.0		V
Ta (note2)	Operating Temperature	20	-	30	℃

(note1)
NEL recommends a DC power supply with an output current capacity of 10 A and an output voltage ripple less than 10 mV rms.
(note2)
The MC740-430E should be protected from condensation.

DATA and CLOCK INPUT SIGNALS

SYMBOL	PARAMETER	Conditions
DATA3 to 0	Data Input Interface	DC coupling (see DC and AC characteristics)
CLK40	40-GHz Clock Input Interface (with an internal DC blocking capacitor)	AC coupling (see AC characteristics)
CLK10	10-GHz Clock Input Interface	AC or DC coupling (see AC characteristics)

DATA and CLOCK OUTPUT SIGNALS

SYMBOL	PARAMETER	Conditions
DATA, /DATA	Data Output Interface	DC coupling, Terminate with 50 Ω to GND
CLK40	40-GHz Clock Output Interface (with an internal DC blocking capacitor)	AC coupling, Terminate with 50 Ω
CLK10	10-GHz Clock Output Interface	AC or DC coupling, Terminate with 50 Ω

MONITOR OUTPUT SIGNALS

SYMBOL	PARAMETER	Conditions
40Gb/s	40-Gb/s Monitor Output Interface (with an internal 10-dB attenuator)	DC coupling, Terminate with 50 Ω to GND
20 Gb/s (odd, even)	20-Gb/s Monitor Output Interface	DC coupling, Terminate with 50 Ω to GND
CLK10	10-GHz Clock Output Interface	AC or DC coupling, Terminate with 50 Ω

DC CHARACTERISTICS

(VPWR = -6.0 V, GND = 0.0V, Ta = 25℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VIH	Data Input Voltage, High (DATA3 to 0)	-0.2	0.0		V
VIL	Data Input Voltage, Low (DATA3 to 0)		-0.9	-0.8	V
VOHD	Data Output Voltage, High (DATA, /DATA)	TBD	0.0		V
VOLD	Data Output Voltage, Low (DATA, /DATA)		-0.9	TBD	V
IPWR	Power Supply Current		7.0	TBD	A
Pd	Power Dissipation		42	TBD	W

AC CHARACTERISTICS

(VPWR = -6.0 V, GND = 0.0V, Ta = 25℃)

DATA and CLOCK INPUT SIGNALS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
fMIN	Minimum Clock Frequency for CLK40			38	GHz
fMAX	Maximum Clock Frequency for CLK40	47 (note)			GHz
Skew	Maximum Skew Among Four Data and CLK10 Inputs	10 (TBD)			pspp
CI40	Clock Input Amplitude for CLK40	0.6 (TBD)	0.9	1.2	Vpp
CI10	Clock Input Amplitude for CLK10	0.7	0.9		Vpp
Vcenter	Center Voltage of CLK40 and 10	-0.5	0.0	0.5	V

(note) 50-Gb/s operation is optional.

DATA and CLOCK OUTPUT SIGNALS

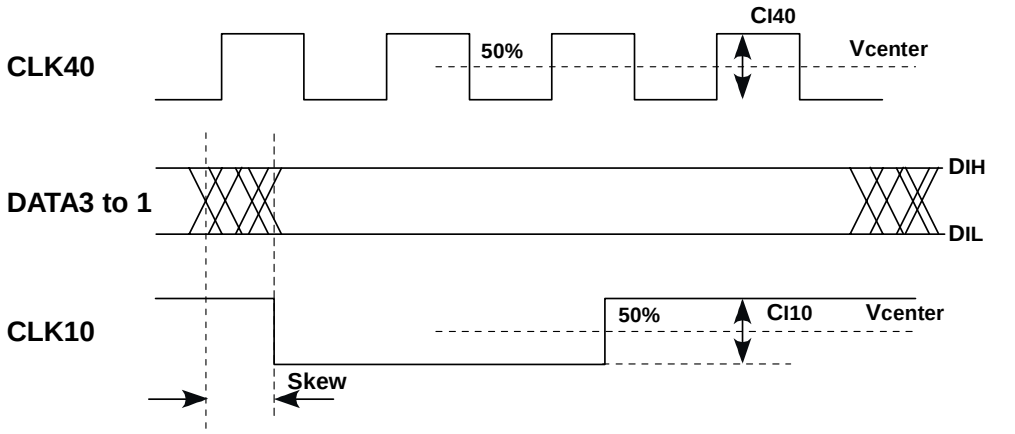
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VampD	Output Voltage Amplitude (DATA, /DATA)	TBD	0.9		Vpp
tr	Output Rise Time (DATA, /DATA)		10	TBD	ps
tf	Output Fall Time (DATA, /DATA)		10	TBD	ps
CO40	Output Voltage Amplitude of CLK40	0.5 (TBD)	0.7		Vpp
CO10	Output Voltage Amplitude of CLK10	0.5 (TBD)	0.7		Vpp
VOHC10	Output Voltage, High (CLK10)	TBD	-0.2		V
VOLC10	Output Voltage, Low (CLK10)		-0.9	TBD	V

MONITOR OUTPUT SIGNALS

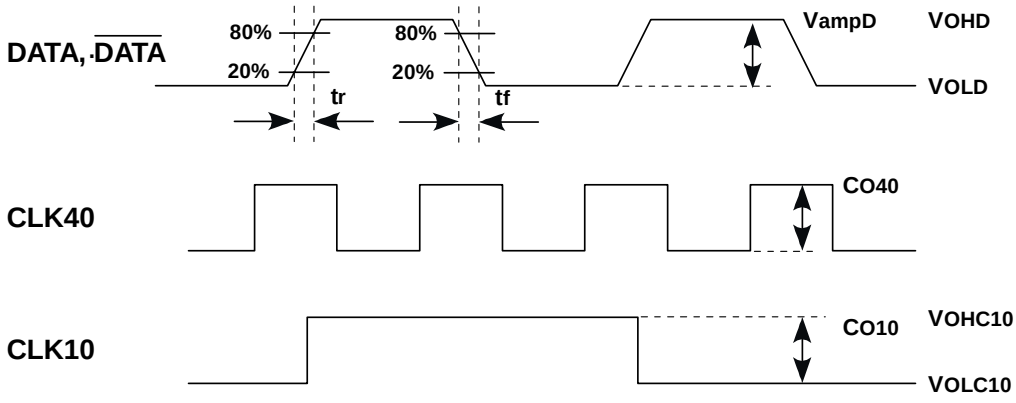
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{ampM40}	Output Voltage Amplitude of 4:1 MUX (with an internal 10-dB attenuator)	-	0.3		Vpp
V_{ampM20}	Output Voltage Amplitude of 20 Gb/s Data, (Odd, Even)	-	0.9		Vpp
C_{M10}	Output Voltage Amplitude of CLK10	0.5 (TBD)	0.7		Vpp
V_{OHM10}	Output Voltage, High (CLK10)	TBD	-0.2		V
V_{OLM10}	Output Voltage, Low (CLK10)		-0.9	TBD	V

DEFINITIONS of SYMBOLS

(1) Data and Clock Input Signals



(2) Data and Clock Output Signals



(3) Monitor Output Signals

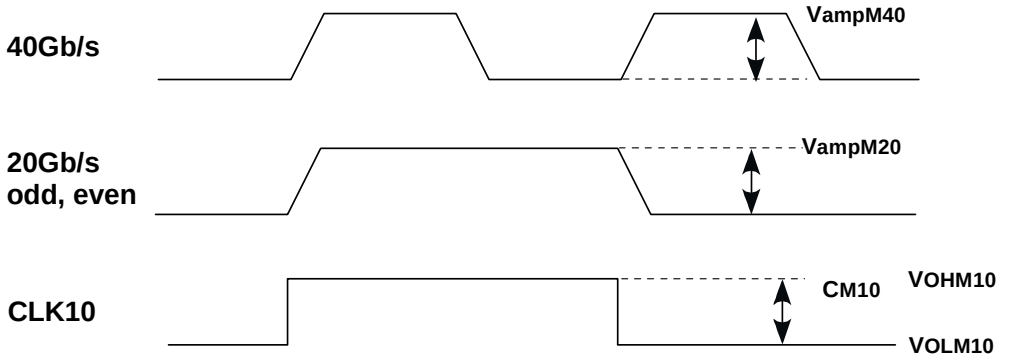
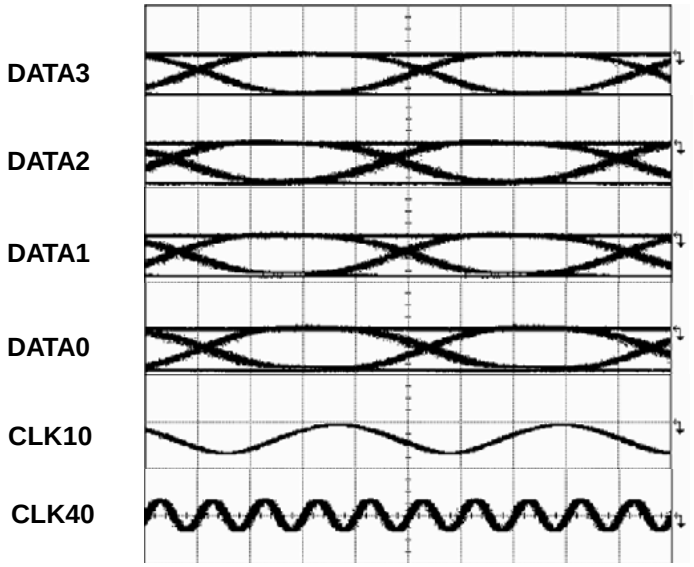


Fig. 4. Definitions of symbols.

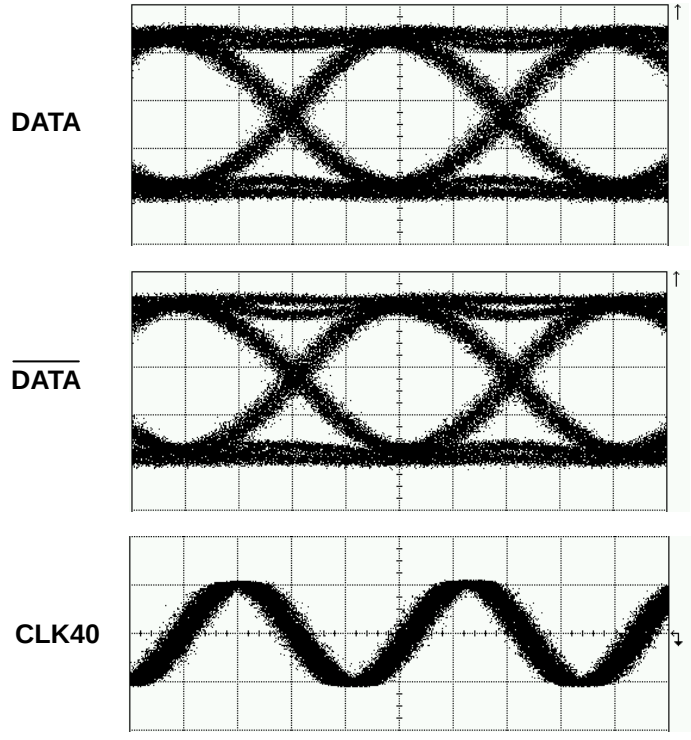
EXAMPLE WAVEFORMS (47-Gb/s OUTPUT)

INPUT SIGNALS



1 V/div, 20 ps/div

OUTPUT SIGNALS



300 mV/div, 5 ps/div

Fig. 5. Example input and output waveforms (47-Gb/s operation).

Measurement conditions
Ta = 25℃, VPWR = -6.0 V
DATA3 to 0: 11.75-Gb/s (2^{23}-1) pseudo-random binary sequence
Sampling Oscilloscope:
Agilent digital communication analyzer (86100A) and plug-in module (83484A)
Cable: SUHNER SUCOFLEX102 (30 cm)

OPERATION

CAUTION

The MC740-430E is very sensitive to electrostatic discharge (ESD). ESD preventive measures must be employed at customer's working desk. Before operating the MC740-430E, please read the handling precautions on page 14.
Before connecting any cables to the input and output terminals, short the center and outer conductors of the cable together.
Mechanical shock can damage or destroy the MC740-430E. Please handle carefully.
Do not remove the warranty seals and/or open the cover.

Turn-on procedure

Connect a DC power supply, signal sources (a pulse pattern generator, PPG, and a synthesizer), an oscilloscope, and a device under test (see the sample implementation, Fig. 9). Here, outputs from the equipments should be turned-off.
If customer connects an AC coupled circuit to the DATA and/or /DATA output terminals, terminate the terminals with 50-ohm resistors via a bias-tee (see Fig. 9).
Output terminals unused should be terminated with 50-ohm resistors.

Power supply sequence is shown in table 1.

Table 1 Turn-On Procedure

Turn-on sequence	Procedure
Step 1	Make sure the output voltage of the DC power supply has been set to be - (minus) 6 V. The DC -6 V on.
Step 2	Main switch (rear panel) on. A current of 1 A is observed at the DC power supply. Wait until the current becomes stable (approximately 10 sec).
Step 3	Front switch on. A current of 7 A is observed at the DC power supply. Wait until the current becomes stable (approximately 10 sec).
Step 4	RF input on.

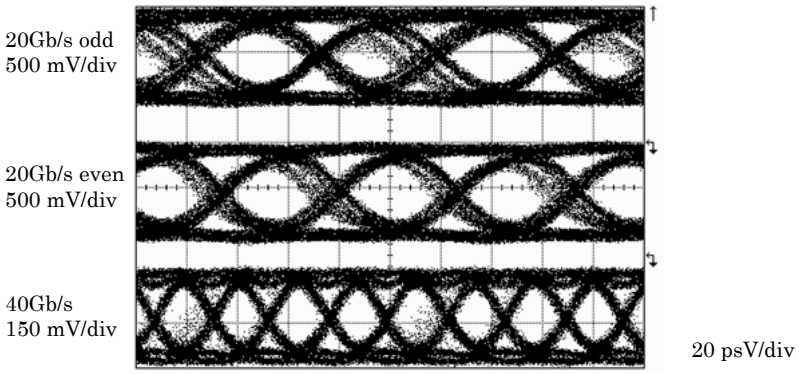
Delay adjustment

To operate the MC740-430E normally, the following delay adjustments are needed (refer to the function diagram, Fig. 1, and sample implementation, Fig. 9).

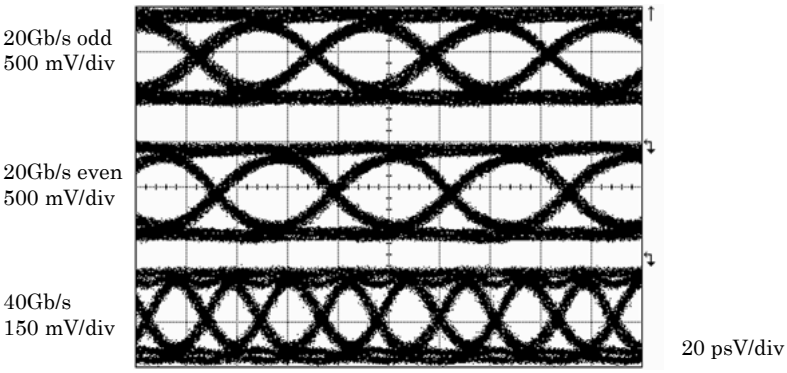
(1) CLK10 output: Adjust the timing between the input data (after latching) and the internal clock at the 4:1 MUX.
(2) Clock delay for the DFF ("ϕshifter" on front panel): Adjust the timing between the output signal from the 4:1 MUX and the clock signal for the DFF.

Step 1 CLK10 output

Insert a phase shifter between CLK10 output terminal and the PPG. Phase shift range of the phase shifter should be 100 ps_{pp}.
Observe the 20 Gb/s monitor outputs by using the oscilloscope. If the CLK10 delay is not optimum, the monitor outputs will be similar to Fig. 6(a). Adjust the CLK10 delay until the monitor output becomes clear (see Fig. 6(b)). When the 20G monitor outputs become clear, the 40G monitor output automatically becomes clear.



(a) with an unsuitable delay



(b) after delay adjustment

Fig. 6. 20G and 40G monitor output waveforms.

Informally, similar adjustment could be done by shifting the delay of CLK10 input (clock delay time from PPG). The output timing from the latching stage, or input data timing for the 4:1 MUX, can be controlled by CLK10 input as shown in Fig. 7. However, this method cannot be applicable for all situations because the clock phase margin of the latching stage is smaller than 360 degree.

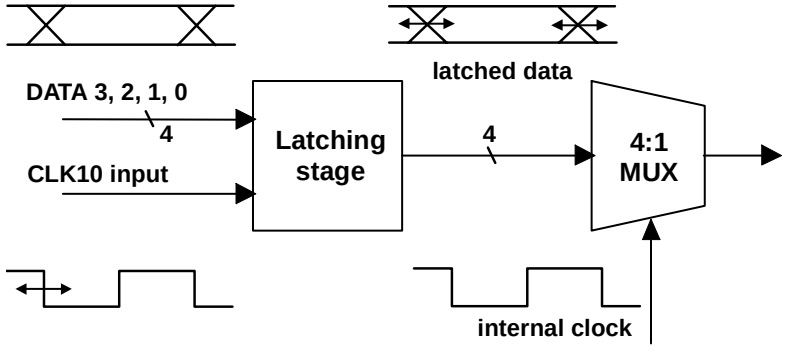
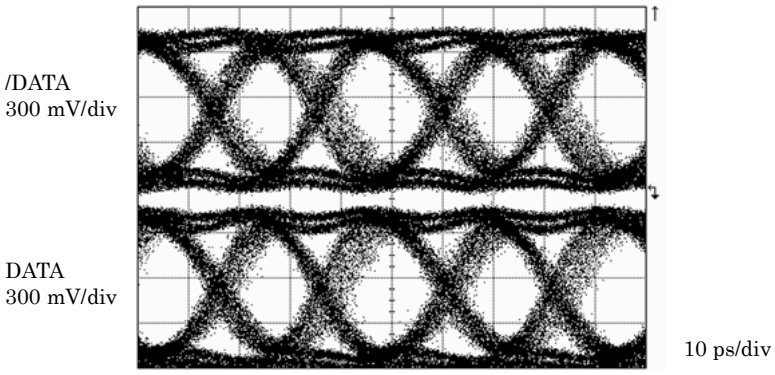


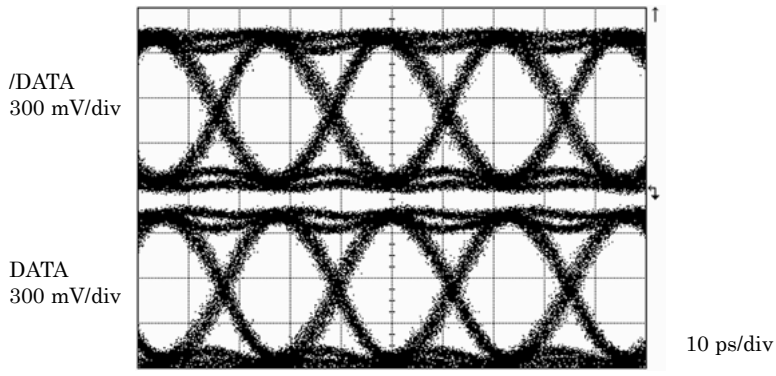
Fig. 7. Delay adjustment by CLK10 input.

Step 2 Clock delay for DFF

If the CLK10 delay is not optimum, the monitor output will be similar to Fig. 8(a). Adjust the clock delay for DFF by using "ϕshifter" dial with monitoring the DFF output signals.



(a) with an unsuitable delay



(b) after delay adjustment at "ϕshifter"

Fig. 8. DFF output waveforms.

Turn-off procedure

Turn-off sequence is shown in Table. 2.

Table 2 Turn-off sequence

Turn-off sequence	Procedure
Step 1	RF inputs off.
Step 2	Front switch off.
Step 3	Main switch (rear panel) off.
Step 4	DC -6 V off.

SAMPLE IMPLEMENTATION

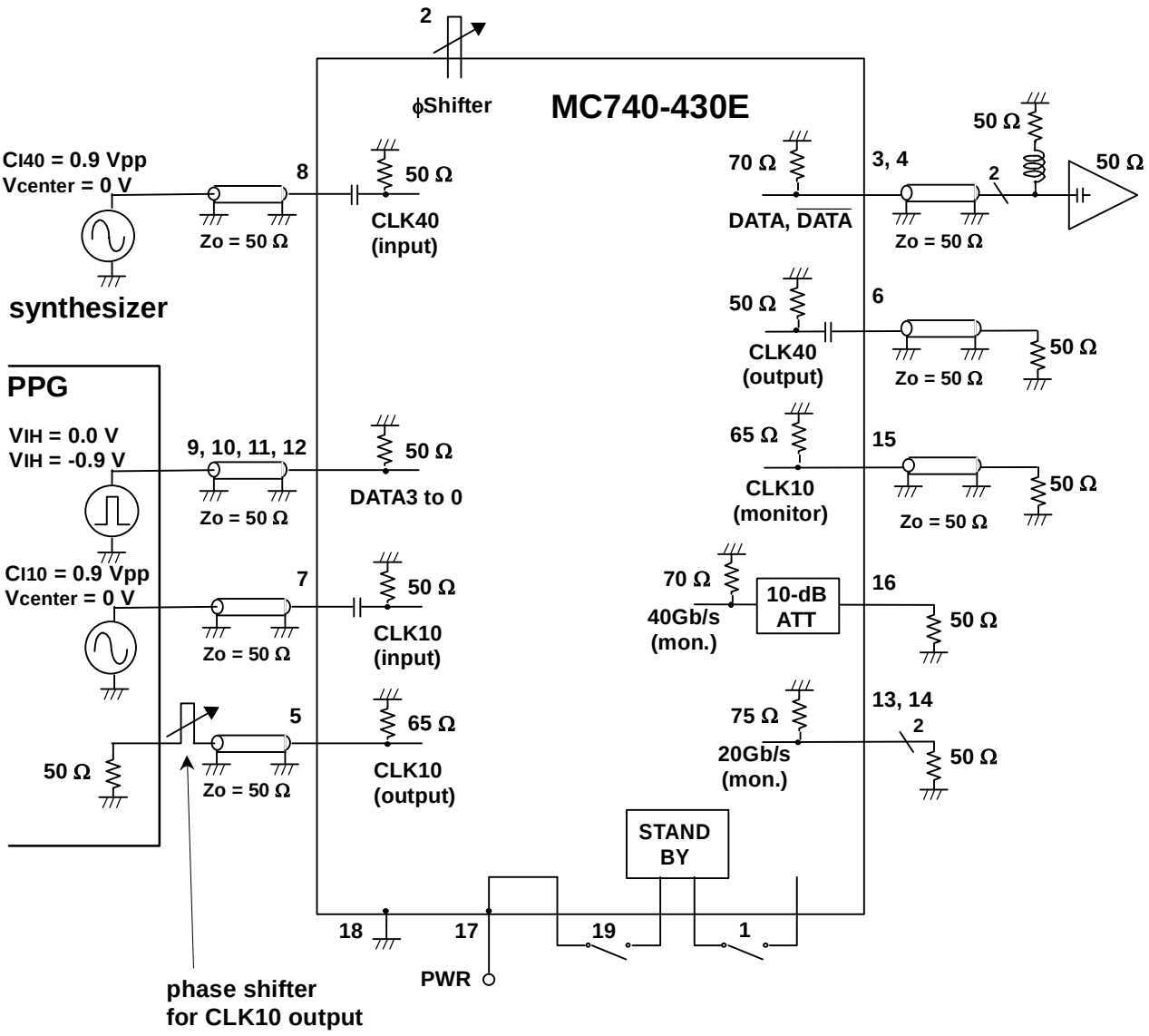


Fig. 9. Sample implementation.

Notes: Each number corresponds to a connector or a dial shown in the connection diagram on page 3.
Power supply sequence is shown on pages 10 -12.

HANDLING PRECAUTIONS

BEFORE OPERATING THE INP HEMT/GaAs MESFET/Si-Bipolar IC MODULES, PLEASE READ THIS HANDLING INSTRUCTION TO PREVENT DAMAGE FROM ELECTRIC SURGES SUCH AS POWER LINE LEAK AND ELECTROSTATIC DISCHARGE.

1. Determine the standard GND on the working desk. The Standard GND should be connected to the highest quality GND in the room.

   Connect commonly all of GND terminals of all the equipment to the standard GND on the working desk. The working desk should be conductive and should be connected to the standard GND.

   Connection cables are preferred to be as short as possible and as thick as possible.

2. Put on a conductive wrist–strap connected to the standard GND on the desk through a 1-Mohm resistor.

3. Confirm that the voltages of all surrounding materials including human body which touch the modules are less than 0.2 V. Please measure these voltages using an oscilloscope (Do not use DC and AC voltmeters).

4. Make sure that there is no abnormal spike on the power supply voltage.

5. Ground all soldering iron tips. Leak voltage should be less than 0.2 V.

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

4. To make a design, the products shall be used within the assured ranges with respect to maximum ratings, voltage, and radiation. NTT Electronics Corp. shall not take any responsibility for damage caused by neglecting the assured values or improper usage.

5. Though NTT Electronics Corp. makes every effort to improve quality and reliability, there is a risk that failure or malfunction may occur in semiconductors. It is therefore necessary that the purchasers should take responsibility for making a design that allows the products to operate safely on equipment and systems without any direct threat to the human body and/or property, should such failures or malfunction occur.

6. NTT Electronics Corp.'s semiconductor device products are designed to be used with multimedia networks communication equipment and related measuring equipment. They have not been developed for such equipment that may affect people's lives. Those who intend to use the products for special purposes that may affect human life as a result of failure or malfunction in the equipment using the products or that require extremely high reliability (e.g. life support, aircraft and space rockets, control in nuclear power facilities, submarine relays, control of operations, etc.) shall contact NTT Electronics Corp. before using the products. NTT Electronics Corp. shall not assume any liability for damage that may occur during operation of the products without prior consultation.

7. This products is controlled under the 'Foreign Exchange and Foreign Trade Law'. In the case of exporting this product, it is requested that you take necessary procedures to obtain prior approval from the Japanese Minister of Economy, Trade and Industry.

8. Some of the products use GaAs (gallium arsenide). GaAs powder and vapor are dangerous for humans. Do not break, cut, crush or chemically destroy the products. To dispose of the products, follow the relevant regulations and laws; do not mix with general industrial waste and domestic garbage.

9. Any questions should be directed to the Sales Department of NTT Electronics Corp.

NTT Electronics Corporation reserves the right to make change in designs, specifications and other information at any time without prior notice. These products or technologies are subject to Japanese strategic restrictions.