MP7506, MP7507

T-51-11

CMOS 8 AND 16 CHANNEL ANALOG MULTIPLEXERS

FEATURES

- DTL/TTL/CMOS Direct Interface
- Power Dissipation: 1.5mW
- R_{ON}: 300Ω
- Break-Before-Make Switching
- Replaces DG506/DG507

GENERAL DESCRIPTION

The MP7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The MP7507 is identical to the MP7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

ABSOLUTE MAXIMUM RATINGS

(T_A=+25°C unless otherwise noted.)

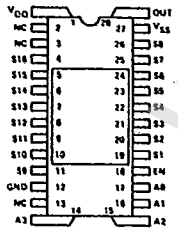
V_{DD} to GND ..... +17V
V_{SS} to GND ..... -17V
V Between Any Switch Terminals 25V
Switch Current (I_S, Continuous) 20mA
Switch Current (I_S, Surge)
1mS duration, 10% duty cycle 35mA
Digital Input Voltage Range ..... V_{DD} to GND
Power Dissipation (Package)*
28 Pin Ceramic DIP** 1000mW
28 Pin Plastic DIP*** 1200mW
Operating Temperature
Plastic ..... 0°C to +70°C
Ceramic (J, K versions) ..... -25°C to +85°C
Ceramic (S, T versions) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C

CAUTION:

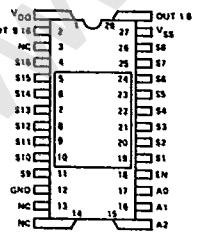
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be set at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

PIN CONFIGURATION (Top View)

MP7506

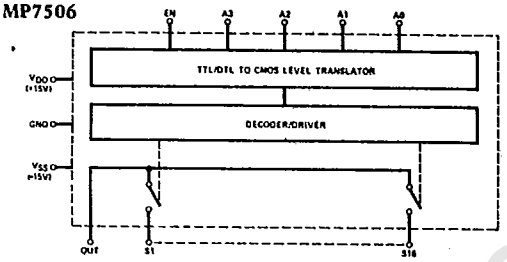


MP7507

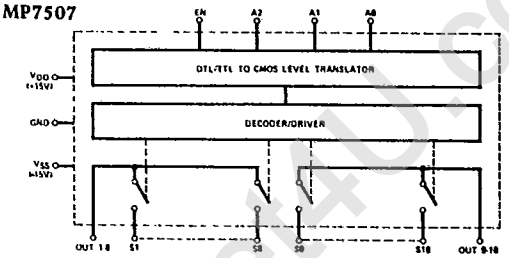


FUNCTIONAL DIAGRAMS

MP7506



MP7507



TRUTH TABLES

MP7506

A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

MP7507

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

* Device mounted with all leads soldered or welded to PC board
** Derate 10mW/°C above +50°C
*** Derate 12mW/°C above +50°C

See Section 7 for Ordering Information

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SPECIFICATIONS V_{DD} = +15V, V_{SS} = −15V unless otherwise noted.

PARAMETER Note 1		VERSION Note 2	SWITCH CONDITION	25°C TYP	Over Specified Temp. Range MIN	Over Specified Temp. Range MAX	UNITS	TEST CONDITIONS
ANALOG SWITCH								
R_{ON}		J, K	ON	450		550	Ω	V_S = −10 V to +10 V, I_S = 1 mA
		S, T	ON	400		500		
R_{ON} vs. V_S		All	ON	15			%	
R_{ON} vs Temperature		All	ON	0.5			%/°C	V_S = 0 V, I_S = 1 mA
ΔR_{ON} Between Switches		All	ON	4			%	
R_{ON} vs. Temperature Between Switches		All	ON	0.05			%/°C	
I_S		J, K	OFF	5		50	nA	V_S = −10 V, V_{OUT} = +10 V and V_S = +10 V, V_{OUT} = −10 V "Enable" Low
		S, T	OFF	1		50	nA	
I_{OUT}	MP7506	J, K	OFF	20		500	nA	
		S, T	OFF	10		500	nA	
	MP7507	J, K	OFF	10		250	nA	
		S, T	OFF	5		250	nA	
$I_{OUT} - I_S$	MP7506	J, K	ON	20		500	nA	V_S = 0
		S, T	ON	10		500	nA	
	MP7507	J, K	ON	10		250	nA	
		S, T	ON	5		250	nA	
DIGITAL CONTROL								
V_{INL}						0.8	V	Note 3
V_{INH}		J, S			3.0		V	
		K, T			2.4		V	
I_{INL} or I_{INH}		All		10		30	µA	
C_{IN}		All		3			pF	
DYNAMIC CHARACTERISTICS Note 4								
$t_{transition}$		J, S		700			ns	V_{IN}: 0 to 3.0 V
		K, T		1000			ns	
t_{open}		All		100			ns	
$t_{on(En)}$		J, S		0.8			µs	V_{EN}: 0 to 3.0 V
		K, T		1.5			µs	
$t_{off(En)}$		J, S		0.8			µs	
		K, T		1			µs	
"OFF" Isolation		All					dB	V_{EN} = 0, R_L = 200 Ω, C_L = 3.0 pF, V_S = 3.0 VRMS, f = 500 kHz
C_S		All	OFF	5			pF	
C_{OUT}	MP7506	All	OFF	40			pF	
	MP7507	All	OFF	20			pF	
C_{S-OUT}		All	OFF	0.5			pF	
C_{SS} Between Any Two Switches		All	OFF	0.5			pF	
POWER SUPPLY								
I_{DD}		J, K	OFF	1			mA	All Digital Inputs Low
		S, T	OFF	1		2	mA	
I_{SS}		J, K	OFF	1			mA	
		S, T	OFF	1		2	mA	
I_{DD}		J, K	ON	1			mA	All Digital Inputs High
		S, T	ON	1		2	mA	
I_{SS}		J, K	ON	1			mA	
		S, T	ON	1		2	mA	

NOTES:
1. Specifications subject to change without notice.
2. JN, KN versions specified for 0°C to +75°C; JD, KD versions for −25°C to +85°C; and SD, TD versions for −55°C to +125°C.
3. A pullup resistor, typically 1-2 kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.
4. AC parameters are sample tested to ensure conformance to specifications.