MX23L6412

SEQUENTIAL 64M-BIT MASK ROM

FEATURES

- Bit organization
  - 4M x 16 (word mode only)
  - 256 words/page
  - Total 16K pages
- Sequential access at 200ns cycle time in a page
- Asynchronous chip enable input (ALEH, ALEL)
- Access time
  - Read latency time: 950ns
  - Read cycle time: 200ns
  - RD access time: 150ns
- Current
  - Operating:25mA(max.)
  - Address input:2mA(max.)
  - Standby:20uA(max.)
- Supply voltage
  - 3.0V~3.6V
- Package
  - 32 pin TSOP

ORDER INFORMATION

Part No.	Read Cycle Time	Package
MX23L6412TC-20	200ns	32 pin TSOP

GENERAL DESCRIPTION

The product is a 64M bits (4M x 16) mask ROM composed of 16K pages, and each consists of 256 words memory cell array. This mask ROM has a 16 bit address input / data output bus (AD0~AD15), two address latch enable pins (high : ALEH, low : ALEL), a read strobe ($\overline{RD}$).

There are 3 modes, Stand-by mode, Active mode, and Address input mode. Stand-by mode is a non-operating state, and has the smallest current dissipation. Active mode is an operating state, and data output is possible. Address input mode is a state of address input.

Address input is through AD bus when ALEL is high. The high and low 16 bit addresses are latched at ALEH'sand ALEL falling edges. As for high 16 bit address, A0~A6 are through 7 bit address register, A7~A15 are not used internally. As for low 16 bit address, A1~A8 are through 8 bit address counter, A9~A15 are through 7 bit address register, and A0 are not used internally. High address input must be done before low address input, and both address inputs are needed for page change or address change in a same page. After address inputs, $\overline{CE}$ goes high at ALEH falling edge and $\overline{RD}$ doesn't toggle, the ROM is in stand-by mode.

After ROM turned into Active mode from Address input mode, it takes tL time to read. In a page, sequential read access is possible at tCYC cycle time. Sequential read operation (increment of internal address counter) is done at every falling edge of RD. At the end of a page, internal address counter raps around to the beginning of the page.

PIN CONFIGURATION

32 TSOP

PIN DESCRIPTION

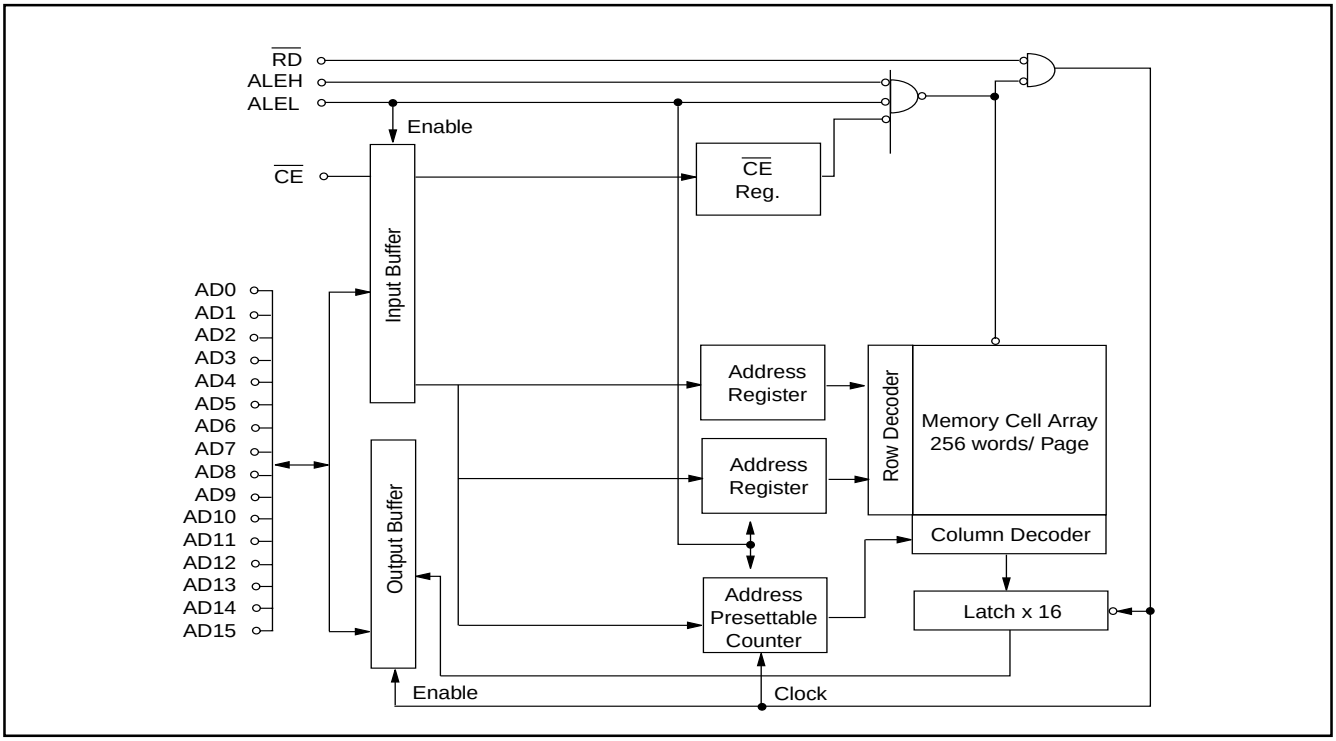
Symbol	Pin Function
AD0~AD15	Address Input / Data Output
ALEH	Address Latch Enable High
ALEL	Address Latch Enable Low
$\overline{CE}$	Chip Enable Input
$\overline{RD}$	Read Strobe Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

TRUTH TABLE

Mode	Operation	$\overline{CE}$	ALEH	ALEL	$\overline{RD}$	AD Bus
Address Input	High address input	L	H	H	X	Address input
Address Input	Low address input	X	L	H	X	Address input
Active	Internally active	X	L	L	H	Floating
Active	Data read	X	L	L	L	Data output
Stand-by	Stand-by *	X	H-->L	L	X	Floating

Note: Please see "standby mode" timing diagram.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.5V to 4.6V
Ambient Operating Temperature	Topr	0° C to 70° C
Storage Temperature	Tstg	-55° C to 125° C

DC CHARACTERISTICS (Ta = 0° C~70° C, VCC = 3.3V±10%)

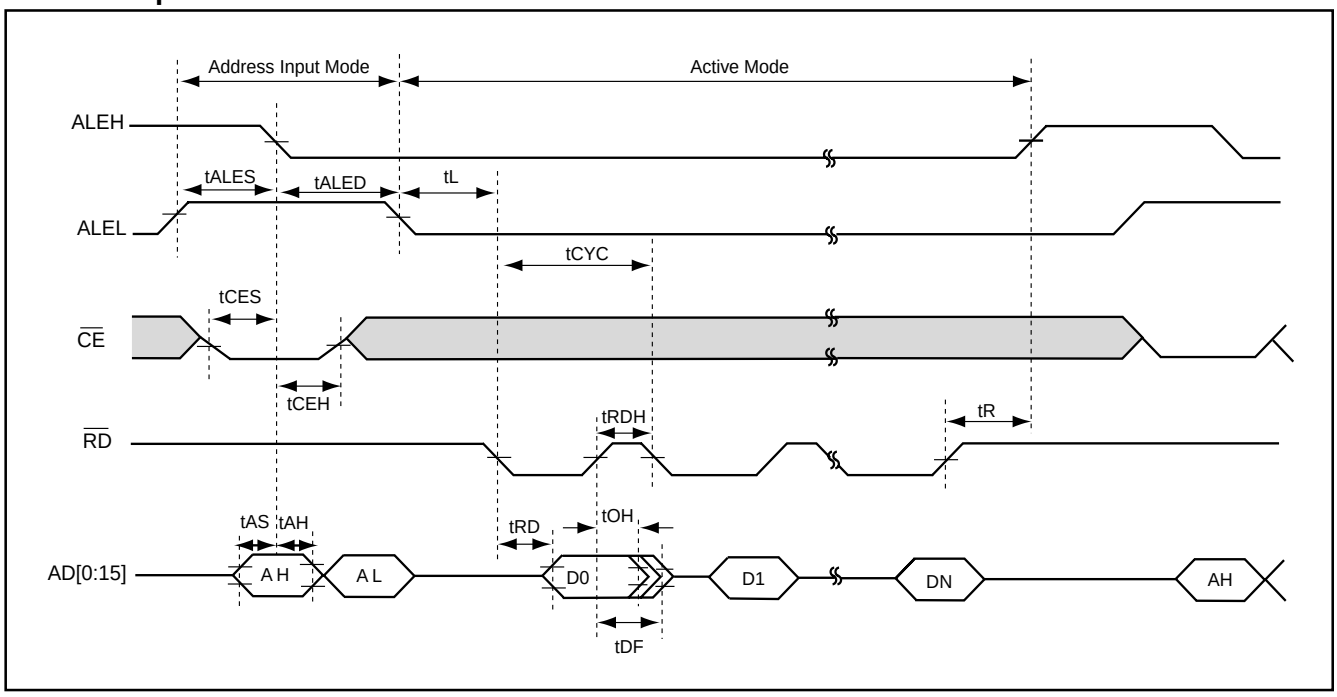
Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.0V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 2mA
Input High Voltage	VIH	2.0V	VCC+0.5V	
Input Low Voltage	VIL	-0.5V	0.8V	
Input Leakage Current	ILI	-10uA	10uA	VIN = 0V to 3.6V
Output Leakage Current	ILO	-10uA	10uA	VOUT = 0V to 3.6V
Operating Current	ICC1	-	25mA	Cycle = 200ns, VIN = VIH or VIL, active mode
Address Input Current	ICC2	-	2mA	Cycle = 100ns, VIN = VIH or VIL, address input mode
Standby Current (CMOS)	ISTB	-	20uA	Cycle = 200ns, VIN = VCC±0.3V or 0V±0.3V,stand-by mode
Input Capacitance	CIN	-	12pF	Ta = 25° C, f = 5MHz, VIN = 0V
Output Capacitance	COUT	-	12pF	Ta = 25° C, f = 5MHz, VOUT = 0V

AC CHARACTERISTICS (Ta = 0° C~70° C, VCC = 3.3V±10%)

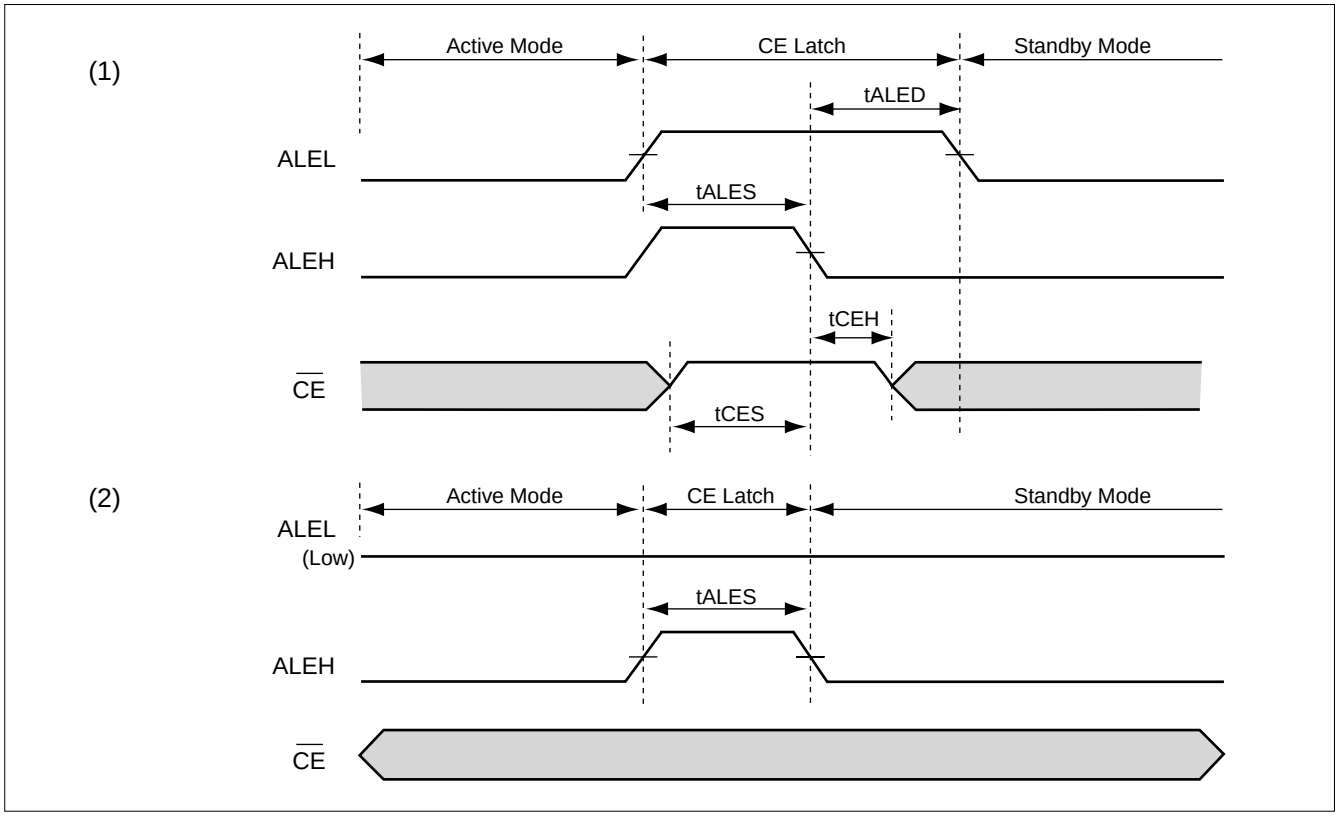
Item	Symbol	MIN.	MAX.	Conditions
ALEL Setup Time	tALES	70ns		
ALE Delay Time	tALED	70ns		
Address Setup Time	tAS	30ns		
Address Hold Time	tAH	0		
Read Latency Time	tL	950ns		
Read Cycle Time	tCYC	200ns		
CE Setup Time	tCES	50ns		
CE Hold Time	tCEH	0ns		
RD Access Time	tRD		150ns	
RD High Time	tRDH	50ns		
Output Hold Time	tOH	0		
Output Float Time	tDF		40ns	
Release Time	tR	0		

TIMING DIAGRAM

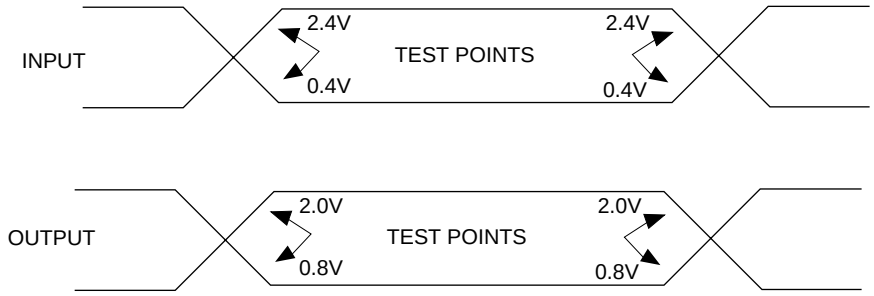
Address Input Mode and Active Mode



Standby Mode



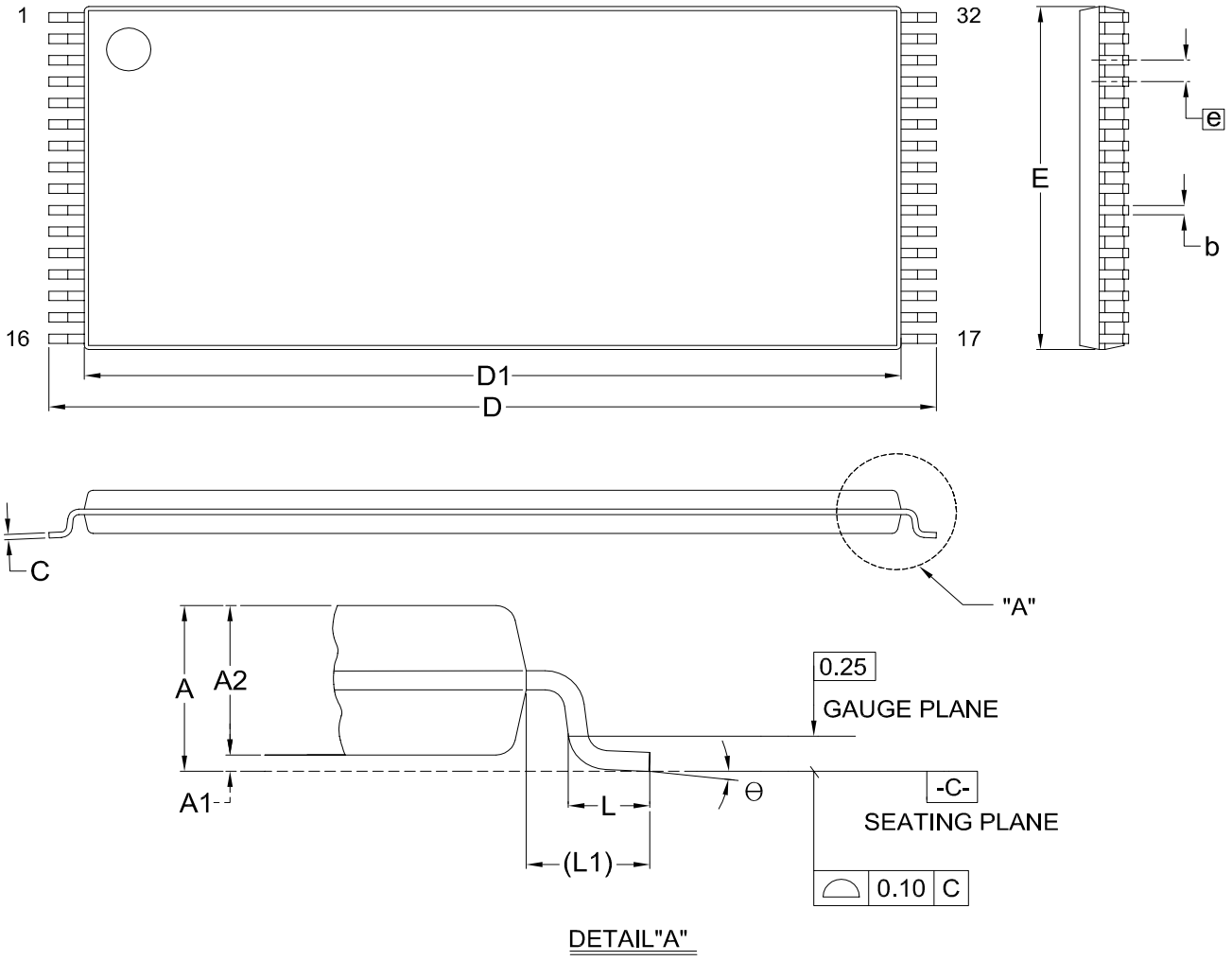
AC Test Conditions



* Input Rise and Fall Times : <10ns
* Output Load : 1TTL+100pF (without active current loading)

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 32L (8X20mm)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.1	To revise the $\overline{CE}$ setup time tCES as 50ns(min.) instead of 30ns	P3	JUL/26/1999
1.2	Modify Access time--Read latency time:1000ns--->950	P1,3	OCT/13/2000
	Add Package Information	P5	
1.3	Change Standby Current:500uA(max.)--->20uA(max.)	P1,3	AUG/17/2001
1.4	Add Standby Mode Timing Diagram	P2,4	FEB/20/2002
1.5	To modify Package Information	P6	MAR/11/2003

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