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| STRUCTURE | Silicon Monolithic Integrated Circuit |
| PRODUCT NAME | γ -correction IC for TFT-LCD Panel |
| TYPE | BD8139EFV |
| FEATURES | <ul style="list-style-type: none"> • Built-in 10ch γ-correction + Vcom outputs • I²C Bus Interface Control (Built-in Auto Read) |

○ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| PARAMETER | SYMBOL | LIMITS | UNIT |
|-----------------------------|--------|----------|------|
| Power Supply Voltage 1 | DVCC | 7 | V |
| Power Supply Voltage 2 | VCC | 20 | V |
| REFIN Voltage | REF | 20 | V |
| Amplifier Drive Current | Io | 50*1 | mA |
| Junction Temperature | Tjmax | 150 | °C |
| Power Dissipation | Pd | 1600*2 | mW |
| Operating Temperature Range | Topr | -30~+85 | °C |
| Storage Temperature Range | Tstg | -55~+150 | °C |

*1 Do not however exceed Pd, AS0 and Tjmax=150°C.

*2 Pd decreased at 12.8mW/°C for temperatures above Ta=25°C, mounted on 70×70×1.6mm Glass-epoxy PCB.

○OPERATING CONDITION (Ta=25°C)

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|--------------------------------|--------|-----|-----|------|
| Power Supply Voltage 1 | DVCC | 2.3 | 4.0 | V |
| Power Supply Voltage 2 | VCC | 6 | 18 | V |
| REFIN Voltage | REF | 6 | 18 | V |
| Amplifier Drive Current | Io | - | 40 | mA |
| I ² C Bus Frequency | fCLK | - | 400 | KHZ |
| OSC Frequency | fosc | 10 | 200 | KHz |

*The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

*This product is not designed for normal operation within a radio active environment.

*Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

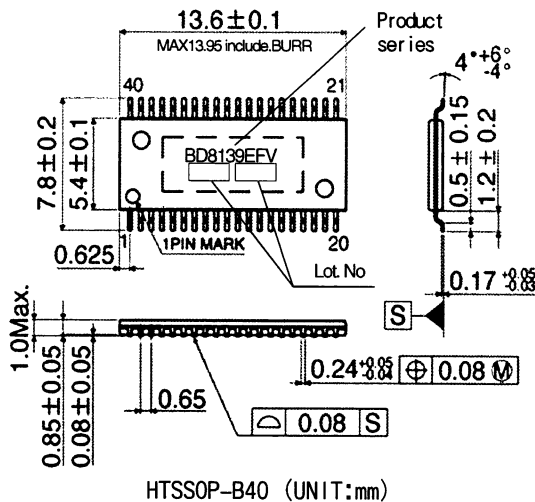
If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS (Unless otherwise specified VCC=15V, DVCC=3.3V, Ta=25°C)

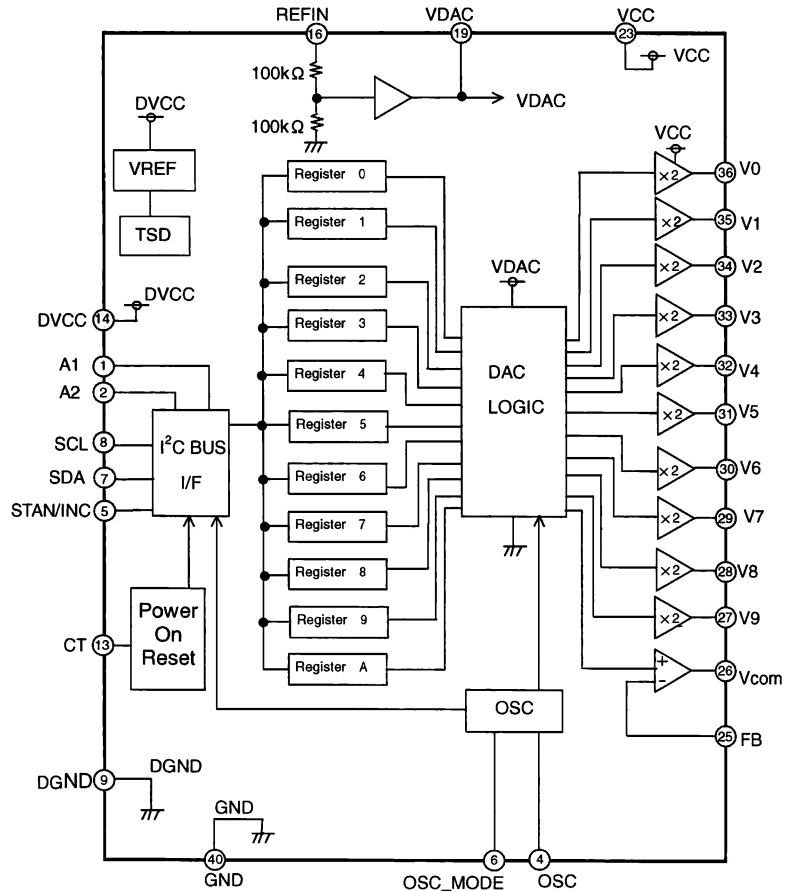
| PARAMETER | SYMBOL | LIMIT | | | UNIT | CONDITIONS |
|----------------------------|------------------|----------|---------|------|------|--|
| | | MIN | TYP | MAX | | |
| 【 REF IN 】 | | | | | | |
| Sink Current | I _{REF} | 25 | 50 | 75 | μA | REF=10V |
| 【 γ-CORRECTION AMP】 | | | | | | |
| Drive Current | I _o | 150 | 300 | - | mA | DAC=3V, OUTx=0V |
| Load Regulation | ΔV | - | 5 | 20 | mV | I _o =+10mA ~ -10mA, OUTx=6V |
| Output Voltage High | VOH | VCC-0.16 | VCC-0.1 | - | V | I _o =-5mA |
| Output Voltage Low | VOL | - | 0.1 | 0.16 | V | I _o =5mA |
| 【 COMMON AMP】 | | | | | | |
| Input Bias Current | I _b | - | 0 | 1 | μA | VFB=6V |
| Drive Current | I _o | 150 | 300 | - | mA | DAC=3V, OUTx=0V |
| Load Regulation | ΔV | - | 5 | 20 | mV | I _o =+10mA ~ -10mA, OUTx=3V |
| Input Voltage Range | VFB | 0 | - | VDAC | V | R _o =100KΩ, C _o =100pF |
| Output Voltage high | VOH | VCC-0.16 | VCC-0.1 | - | V | I _o =-5mA |
| Output voltage Low | VOL | - | 0.1 | 0.16 | V | I _o =5mA |
| 【 DAC】 | | | | | | |
| Resolution Coding | Res | - | 10 | - | Bit | |
| Non-Linear Error | LE | -2 | - | 2 | LSB | Range of 00A ~ 3F5 error with ideal straight |
| Differential Error | DLE | -2 | - | 2 | LSB | Range of 00A ~ 3F5 error with ideal amount of Increase in 1LSB |
| 【 OSC】 | | | | | | |
| Frequency | fosc | - | 210 | - | KHz | Internal oscillator mode |
| 【 CONTROL SIGNAL】 | | | | | | |
| Sink Current | I _{ctl} | - | 16 | 25 | μA | |
| SDA output voltage Low | VSDA | - | - | 0.4 | V | I _{SDA} =3.0mA |
| Input leakage Current | I _{Li} | -10 | - | 10 | μA | 0.4V~0.9DVCC |
| Threshold Voltage | V _{TH} | 0.7 | - | 2.6 | V | DVCC=3.3V |
| Reset Time | trst | - | 45 | - | μs | CCT=1000pF |
| 【 WHOLE DEVICE】 | | | | | | |
| Circuit Current | I _{cc} | - | 18 | - | mA | All outputs = 5V |

*This product is not designed for protection against radioactive rays.

○PHYSICAL DIMENSIONS • MARKING



○BLOCK DIAGRAM



※Refer to the Technical Note about the details of the application.

○PIN No, Pin Name, Function

| PIN No | PIN NAME | Function | PIN No | PIN NAME | Function |
|--------|----------|--|--------|----------|-----------------------------|
| 1 | A1 | Slave/Slave address set① Autoread/word address set① for EEPROM | 21 | NC | — |
| 2 | A2 | Slave/Slave address set② Autoread/word address set② for EEPROM | 22 | NC | — |
| 3 | NC | — | 23 | VCC | POWER SUPPLY |
| 4 | OSC | SYNCHRONIZED CLOCK INPUT | 24 | NC | — |
| 5 | STAN/INC | INPUT MODE SWITCH FOR I ² C | 25 | FB | COM negative feedback INPUT |
| 6 | OSC_MODE | OSC MODE SWITCH (INTERNAL/EXTERNAL) | 26 | VCOM | COM OUTPUT |
| 7 | SDA | DATA SIGNAL INPUT FOR I ² C | 27 | V9 | GAMMA 9 output |
| 8 | SCL | CLOCK SIGNAL INPUT FOR I ² C | 28 | V8 | GAMMA 8 output |
| 9 | DGND | GROUND | 29 | V7 | GAMMA 7 output |
| 10 | DACGND | GROUND FOR DAC | 30 | V6 | GAMMA 6 output |
| 11 | NC | — | 31 | V5 | GAMMA 5 output |
| 12 | NC | — | 32 | V4 | GAMMA 4 output |
| 13 | CT | CAPACITOR CONNECTION FOR POWER ON RESET | 33 | V3 | GAMMA 3 output |
| 14 | DVCC | DIGITAL POWER SUPPLY | 34 | V2 | GAMMA 2 output |
| 15 | NC | — | 35 | V1 | GAMMA 1 output |
| 16 | REF1N | DAC REFERENCE INPUT | 36 | V0 | GAMMA 0 output |
| 17 | NC | — | 37 | NC | — |
| 18 | NC | — | 38 | NC | — |
| 19 | VDAC | DAC VOLTAGE OUTPUT | 39 | NC | — |
| 20 | NC | — | 40 | GND | GROUND |

● Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a setting of heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

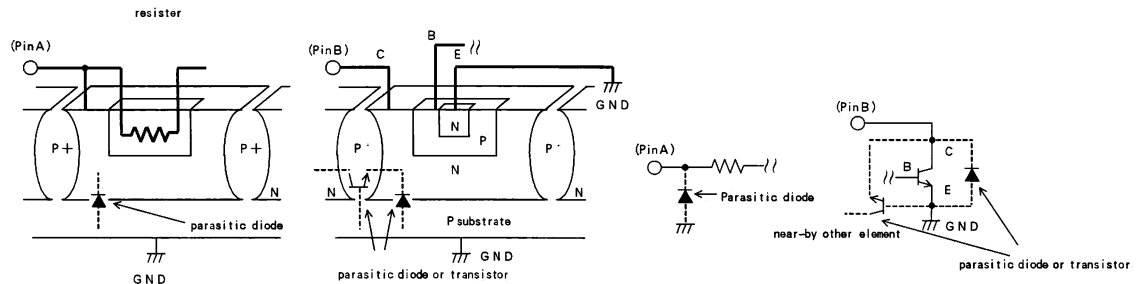
6) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

7) Regarding input pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins. (see the chart below)

The formation of parasitic NPN transistors according to the relationships of different IC pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input and out



8) Thermal shutdown circuit (TSD)

This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature Tj will trigger the thermal shutdown circuit to turn off all output power elements. The circuit will automatically reset once the chip's temperature Tj drops. Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the circuit.

9) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

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